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Study on the recovery of NBTI of ultra-deep sub-micro MOSFETs*

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Taking the actual operating condition of complementary metal oxide semiconductor (CMOS) circuit into account, conventional direct current (DC) stress study on negative bias temperature instability (NBTI) neglects the detrapping of oxide positive charges and the recovery of interface states under the 'low' state of p-channel metal oxide semiconductor field effect transistors (MOSFETs) inverter operation. In this paper we have studied the degradation and recovery of NBTI under alternating stress, and presented a possible recovery mechanism. The three stages of recovery mechanism under positive bias are fast recovery, slow recovery and recovery saturation.

Keywords: NBTI, recovery, interface states, oxide positive charges
PACC: 7340Q, 7300, 7220J

1. Introduction

With the rapid development of very large scale integration (VLSI), the device dimensions have been reduced continuously. Among the reliability problems of ultra-deep sub-micro devices, negative bias temperature instability (NBTI) is getting worse, and turns into one of the most dominant degradation mechanisms and receives broad attention from the entire semiconductor industry.[1−3]

NBTI is an effect occurring in PMOSFETs under negative gate bias stress and high temperatures. It leads to the increase of threshold voltage $V_{\rm th}$ and 'off' current $I_{\rm off}$ and the degradation of drain current $I_{\rm d}$ and transconductance $G_{\rm m}$. In conventional NBTI study, the devices are stressed by constant negative gate bias at high temperatures with the source and the drain grounded. However, in the actual complementary metal-oxide semiconductor (CMOS) circuits, the gate bias of PMOSFETs is switching between high and low voltages. The direct current (DC) stress neglects the recovery of interface states and the detrapping of oxide positive charges in CMOS circuits. Therefore, DC stress overestimates the degradation and underestimates the lifetime of the device.[4] The degradation of NBTI under alternating stress has been studied recently. However, there are contradictions among recovery mechanisms. In this paper we study the degradation and recovery of NBTI in the 0.1μm PMOSFETs, and present a possible mechanism which interprets the recovery.

2. Devices and experiments

The PMOSFETs used here are of surface channel. They were manufactured using a 90 nm process technology with lightly doped drain (LDD) structure and shallow trench isolation (STI) scheme. All the devices were 0.1 μm in length, 10 μm in width and the oxide thickness was 1.4 nm. The gate oxides of all devices were annealed in N_2O atmosphere after thermal growth. An Agilent B1500A high-precision semiconductor parameter analyser was used to conduct the tests. Figure 1 is the schematic diagram of NBTI under alternating stress. The devices were stressed under NBTI stress conditions of $V_{\rm g} = V_{\rm stress}$, and $V_{\rm d} = V_{\rm s} = 0$ at elevated temperatures. $V_{\rm stress}$ was alternated between negative and positive gate bias in our experiments. Stress was interrupted at regular intervals so that device parameters were measured. For all tests, the threshold voltage was determined from

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$I_d - V_g$ curve using the maximum slope current method with a drain voltage of -0.05V. As the threshold voltage V_{th} is one of the most important parameters and it degrades more quickly than other parameters, this paper makes a point on the study of V_{th} degradation and analyses the mechanism.

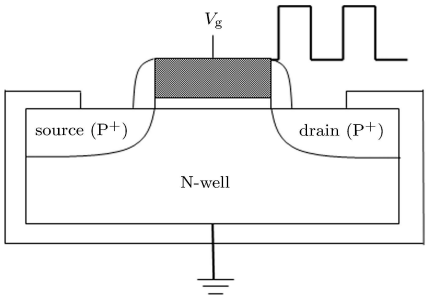


Fig.1. Schematic of NBTI under alternating stress.

3. Results and discussion

Figures 2 and 3 show the output and transfer characteristics of 0.1μm PMOSFETs respectively. From the figures, we can see that the drain current reaches 10^{-3} Aμm^{-2} in magnitude and the threshold voltage is about -0.2V. All these show the natural performance of the 0.1 μm PMOSFETs and testing results are credible on these devices under different bias and temperature (BT) stresses. Under conventional DC bias stress, NBTI is studied at 120 °C. The relationship between ΔV_{th} (the difference between the initial V_{th} and the V_{th} tested at the stress intervals) and stress time shows a perfect linearity in the log-log scale as shown in Fig.4. Its slope 0.28 is identical with the result of conventional study.[5] The increase of V_{th} demonstrates that additional positive charges are produced. The expression of V_{th} is given by

$$V_{th} \propto -\frac{qN_f}{C_{ox}} - \frac{qN_{it}(\phi_s)}{C_{ox}}, \qquad (1)$$

where N_f is the density of fixed positive charges, and N_{it} is the density of interface states which depends on the surface potential ϕ_s. The shift of V_{th} can be caused by the increase of fixed positive charges and interface states, and it will lead to the final failure of the devices. However, DC stress has neglected the actual operating conditions of CMOS circuits: gate bias is switching between high and low voltages. Different phenomena must be generated in the process of alternating stress. Figure 5 shows the degradations of NBTI under DC and alternating stresses. As can be seen clearly, the degradation in the first stress cycle under alternating gate bias is consistent with that of the DC stress. When gate bias turns positive, V_{th} starts to recover. The final degradation will be smaller than that under DC condition due to the recovery. It is clear that the recovery of V_{th} caused by positive bias plays an important role in the effect of NBTI. Figure 6 shows the NBTI effect under alternating stress. A whole cycle takes 3000s, including 1000s for stress time and 2000s for recovery time. It can be seen clearly that ΔV_{th} increases continuously during the negative bias stress period of 1000s as expected. When reversing gate bias to the opposite polarity (positive), a reduction of ΔV_{th} is observed. ΔV_{th} falls down quickly to point A, and then the falling rate becomes smaller down to point B. After point B, the shift of ΔV_{th} is so small that ΔV_{th} can be considered constant and the recovery tends to be 'saturation'. Suppose the last ΔV_{th} of each negative bias stress cycle to be ΔV_{th}^0. We plot the two recovery cycles with the values of $\Delta V_{th}/\Delta V_{th}^0$ in the same time range, just like Fig.7. Each recovery cycle can be divided into three stages corresponding to those of Fig.6. The three stages are named as 'fast recovery', 'slow recovery' and 'recovery saturation'; and they are caused by different recovery mechanisms.

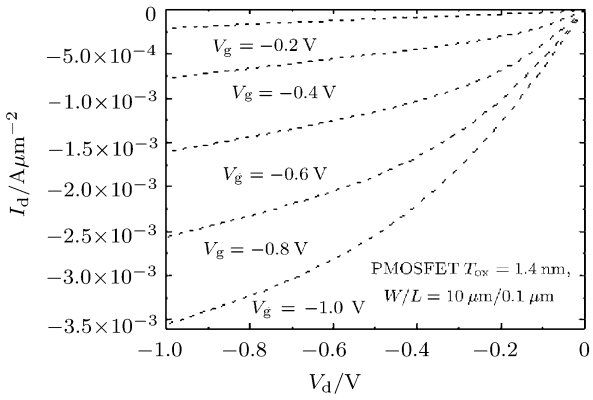


Fig.2. Output characteristics of 0.1μm PMOSFETs.

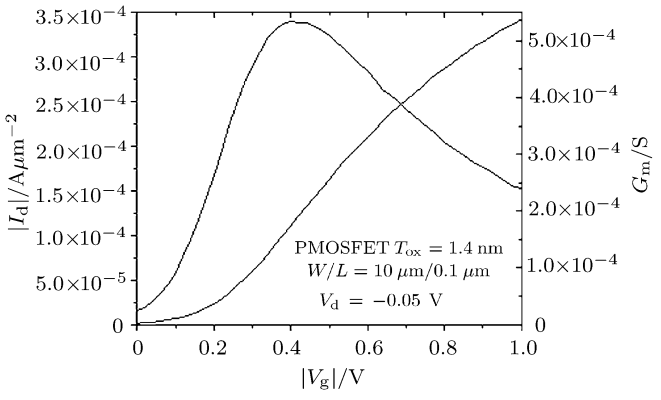


Fig.3. Transfer characteristics of 0.1μm PMOSFETs.

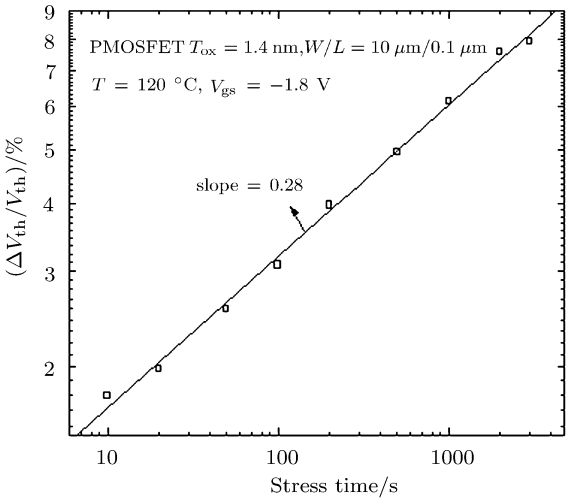


Fig.4. Shift of V_{th} under DC condition with $V_{gs} = -1.8$V at 120°.

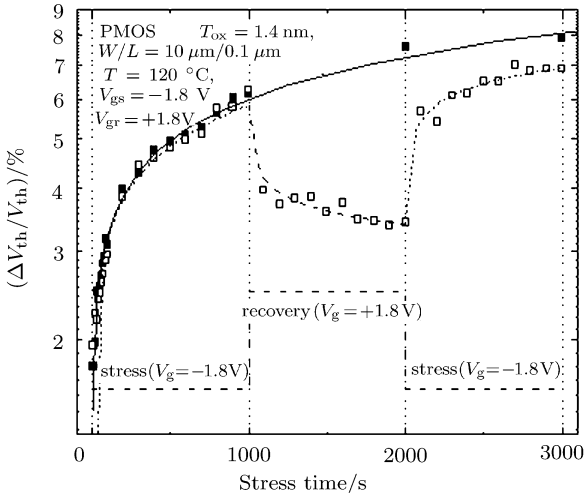


Fig.5. Variations of V_{th} under DC and dynamic stressing-recovery-stressing NBTI.

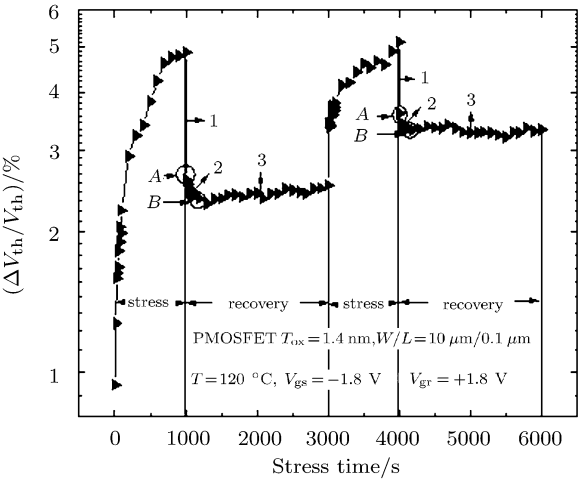


Fig.6. Degradation of ΔV_{th} under dynamic stressing-recovery-stressing conditions with $V_{gs} = -1.8$V and $V_{gr} = +1.8$V at 120°.

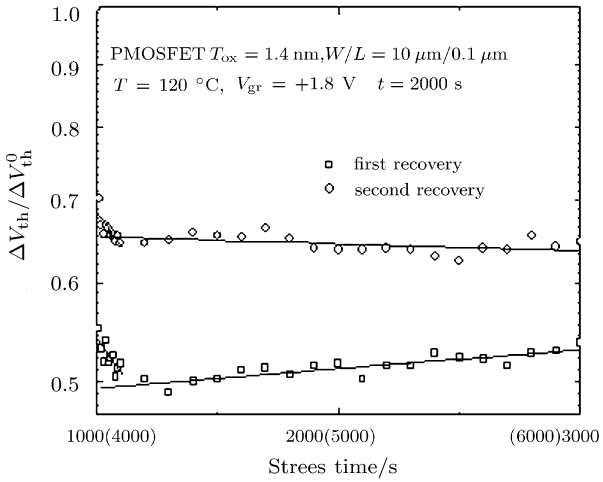


Fig.7. Two recovery curves plotted in the same time scales. The first recovery time ranges from 1000 to 3000s, and the second from 4000 to 6000s.

The NBTI degradation is generally thought to be related to the breaking of SiH bond.[6,7] Stressed by a constant negative gate bias, the energy band of n-substrate rises, and the holes (h^+) are accumulated at the channel region. The hydrogen (H) absorbed in the technological process is present at the interface of Si/SiO_2 in the form of SiH. With the interaction of holes in the inversion layer, SiH bonds are weakened and, at elevated temperatures and under the effect of electric field, the dissociations of H atoms occur with the corresponding generation of interface states (Si dangling bond).[8] Under the inversion condition, H atoms become H^+ ions or protons, being the only stable charge state of H at the interface.[6,9] Some H^+ ions move in the direction towards polySi under the effects of electric field and concentration gradient. Some of these H^+ ions are trapped in the oxide layer to produce fixed positive charges. Meanwhile, at the interface, some H^+ ions continue to react with $Si_3 \equiv SiH$. The SiH complex is polarized such that the Si atom holds more positive charge and the H atom holds more negative charge.[9] Therefore, the positively charged H^+ will react directly with SiH to generate more interface states and H_2 molecules which move to polySi due to the concentration gradient. Some time later, there will be H^+ ions and H_2 molecules lost in the polySi [10] in the process. At the same time of this process, some holes are injected into and trapped by oxide layer. The whole process of negative bias stress is shown in Fig.8. All the related reactions in the stress process are as follows:

$$Si_3 \equiv SiH + h^+ \rightarrow Si_3 \equiv Si \bullet + H^+, \qquad (2)$$

$$\mathrm{Si_3 \equiv SiH + H^+ \rightarrow Si_3 \equiv Si \bullet + H_2}, \quad (3)$$

$$\mathrm{H^+ \xrightarrow{traping} SiO_2}, \quad (4)$$

$$\mathrm{h^+ \xrightarrow{traping} SiO_2}. \quad (5)$$

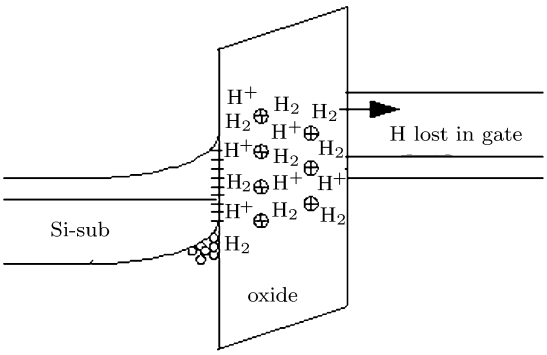


Fig.8. Schematic of the process of NBTI stress. ⊗ holes trapped in oxide layer, ○ holes in the inversion layer.

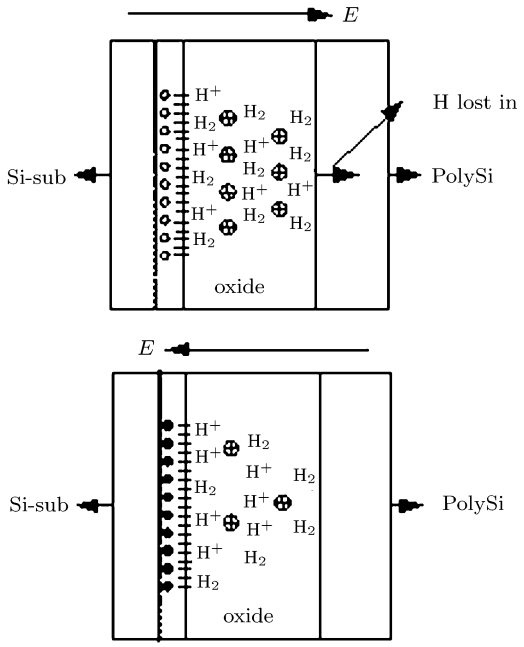


Fig.9. Schematics of the process of stressing and recovery of NBTI. ⊗ holes trapped in oxide layer, ○ holes in the inversion layer, • electrons in the accumulation layer.

After the negative stress in the period of 1000s, positive stress is applied to the gate electrode. As shown in Fig.6, the recovery can be divided into three stages. Figure 9 shows the changes in $Si/SiO_2/polySi$ under stress and recovery conditions. The 1.4nm thick oxide layer is only several atoms thick. Therefore, the fixed positive charges trapped in the oxide layer are not stable and the H^+ ions can get released by quickly detrapping[11] and the holes are also released and turn towards the channel area.[12] Meanwhile, those H^+ ions near the interface turn back to the interface. Under the accumulation condition, the H^+ ion picks up an electron and then reacts with the Si dangling bond to form a Si-H bond, namely, passivating an interface state. All these lead to a fast falling of ΔV_{th} at first seconds. That is the first stage 'fast recovery'. After the detrapping of H^+ ions and holes, there only H^+ effect is left in the recovery process. For smaller concentration of H_2 molecules due to the cease from producing H_2 molecules, some H_2 molecules begin to move back to the interface. With the help of electrons, the H^+ ions from the decomposing of H_2 molecules can assist the passivation of interface states. The falling rate of ΔV_{th} becomes smaller for several reasons. The first is that a lot of hydrogen (including H^+ ions and H_2 molecules) have been lost in polySi and there are still some hydrogen moving into polySi even under positive bias. The second is that it needs time for hydrogen to move back to the interface. This is the second stage 'slow recovery'. The last stage is the 'recovery saturation', in which the amount of hydrogen moving back is limited, and ΔV_{th} becomes stable. All the related reactions in the process of recovery are given as follows:

$$\mathrm{H^+ \xrightarrow{det\ raping} SiO_2}, \quad (6)$$

$$\mathrm{h^+ \xrightarrow{det\ raping} SiO_2}, \quad (7)$$

$$\mathrm{H_2 + 2e^- \rightarrow 2H^+}, \quad (8)$$

$$\mathrm{Si_3 \equiv Si \bullet + H^+ + e^- \rightarrow Si_3 \equiv SiH}. \quad (9)$$

Two negative bias stress cycles are plotted in the same time scale in Fig.10. The first stress time cycle ranges from 0 to 1000 s and the second actual time lies between 3000 and 4000 s. For an incomplete recovery, there exists the 'recovery saturation', and the starting point of degradation of the second cycle is higher than that of the first. However, after the stress time of 1000 s, ΔV_{th} of the second cycle is only a little higher than the first. From Fig.10, we can also see clearly that the degradation rate in the second cycle is much smaller than in the first. The reason is that in the recovery cycle, the amount of interface states and oxide charges decreases, so the distribution of hydrogen changes. There are much fewer SiH bonds which cause NBTI, and the recovery portion in the second cycle is smaller too, as shown in Fig.7.

In Fig.11, ΔV_{th} degradations in the two recovery cycles at different recovery temperatures are plotted

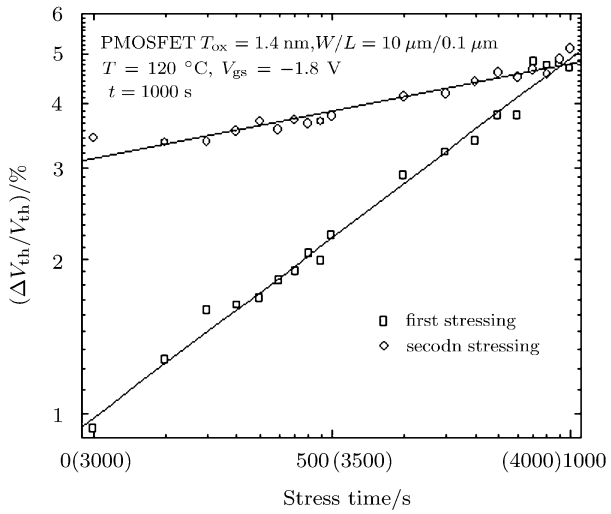


Fig.10. Two stressing processes plotted in the same time scale. The first stressing time ranges from 0 to 1000s, and the second one from 3000 to 4000s.

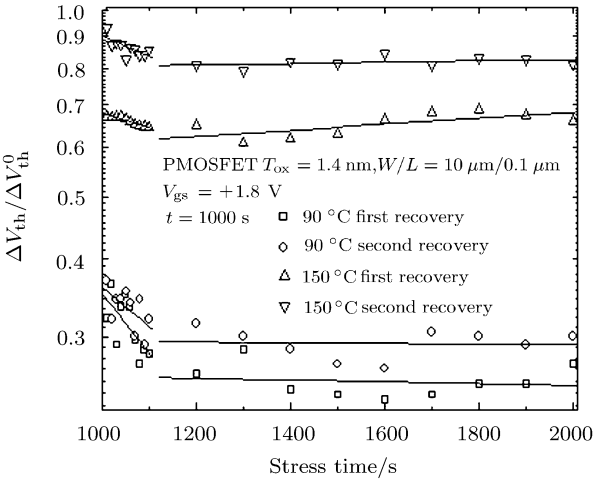


Fig.11. Different recoveries with the values of $\Delta V_{\rm th}/\Delta V_{\rm th}^0$ plotted in the same time scale at different temperatures.

with the values of $\Delta V_{\rm th}/\Delta V_{\rm th}^0$ in the same time scale. Recoveries are different at different temperatures. The recovery becomes smaller when temperature becomes higher, and the second cycle has a smaller recovery than the first. The higher the temperature, the larger the energy of H^+ and h, and the fewer of them are trapped, resulting in more hydrogen lost in polySi. Therefore, recovery becomes smaller.

4. Conclusions

The degradation and recovery of NBTI are observed in 0.1μm PMOSFET. NBTI recovery occurs in three stages. The first stage is called 'fast recovery'. Positive charges trapped in the oxide layer get released quickly under positive gate bias. Meanwhile, H^+ ions located near the interface move back to passivate interface states. Both the reasons lead to the quick fall of NBTI degradation. The second stage is named 'slow recovery', which is only due to the effect of H^+ ions. After some times, the recovery of NBTI tends to be balanced, which is the third stage 'recovery saturation'. With in this mechanism, temperature can affect NBTI drastically. When the temperature gets higher, the recovery portion of NBTI becomes smaller. And with increasing number of cycles, the recovery of NBTI also becomes smaller.

Acknowledgment

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