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Hot-carrier degradation for 90 nm gate length LDD-NMOSFET with ultra-thin gate oxide under low gate voltage stress*

Chen Hai-Feng(陈海峰)†, Hao Yue(郝 跃), Ma Xiao-Hua(马晓华), Li Kang(李 康), and Ni Jin-Yu(倪金玉)

School of Microelectronics, Xidian University, Xi'an 710071, *China*

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The hot-carrier degradation for 90 nm gate length lightly-doped drain (LDD) NMOSFET with ultra-thin (1.4 nm) gate oxide under the low gate voltage (LGV) (at $V_g = V_{th}$, where V_{th} is the threshold voltage) stress has been investigated. It is found that the drain current decreases and the threshold voltage increases after the LGV ($V_g = V_{th}$) stress. The results are opposite to the degradation phenomena of conventional NMOSFET for the case of this stress. By analysing the gate-induced drain leakage (GIDL) current before and after stresses, it is confirmed that under the LGV stress in ultra-short gate LDD-NMOSFET with ultra-thin gate oxide, the hot holes are trapped at interface in the LDD region and cannot shorten the channel to mask the influence of interface states as those in conventional NMOSFET do, which leads to the different degradation phenomena from those of the conventional NMOS devices. This paper also discusses the degradation in the 90 nm gate length LDD-NMOSFET with 1.4 nm gate oxide under the LGV stress at $V_g = V_{th}$ with various drain biases. Experimental results show that the degradation slopes (n) range from 0.21 to 0.41. The value of n is less than that of conventional MOSFET ($0.5 - 0.6$) and also that of the long gate length LDD MOSFET (~ 0.8).

Keywords: threshold voltage, lightly doped drain, gate-induced drain leakage current, hot hole
PACC: 7340Q, 7340, 7360H

1. Introduction

Lightly doped drain (LDD) MOSFETs have become the standard devices in integrated circuits. As the feature size of device shrinks sharply, the electric field in the device is stronger than before, so the carriers can easily gain higher energy to become hot carriers (HCs), resulting in the degradation of the device.[1] In LDD-MOSFETs, the distribution of the lateral fields is changed. The maximal lateral field occurs in the LDD region, which makes the damage region move away from the corner of drain in conventional device to the LDD region. This change in damage region induces many degradation phenomena and the mechanism of LDD-MOSFET different from those of the conventional MOSFET. Therefore, an all-sided investigation of the HC degradation in LDD-MOSFETs is specially necessary.

However, the study of HC degradation in LDD device is mainly focused on damage under the middle gate voltage stress ($V_g = 0.5V_d$) and high gate voltage stress ($V_g = V_d$) at present.[2,3] Under these stresses hot electrons have received more attention. But the study on the low gate voltage (LGV) stress ($V_g = V_{th}$), in which hot holes can be created,[4] attains less attention. As the downscaling of gate oxide continues, positive charge formed near interface will become increasingly important.[5] So the study on the HC degradation under the LGV ($V_g = V_{th}$) stress is helpful to understanding the mechanism of the damage created by hot holes in the ultra-short gate length LDD MOSFET with ultra-thin gate oxide. Meanwhile, such a study also reveals the real damage in device in that the real device operates in a low gate voltage.

In this paper are studied the HC degradation and the mechanism of damage created by hot holes in the ultra-short gate length and ultra-thin gate oxide LDD-NMOSFET under the LGV stress at $V_g = V_{th}$ with various fixed values of V_d. Because on the analysis of the change in electronic characteristic of device, the degradations of V_{th}, the maximal transconductance

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†E-mail: heellor@163.com

($G_{\rm mmax}$), the drain linear current ($I_{\rm dlin}$) and the drain saturation current ($I_{\rm dsat}$) are presented and the physical mechanism of damage is discussed in detail.

2. Devices and experiments

The devices used in this paper are LDD-NMOSFETs, fabricated in a standard 90 nm CMOS technology. The LDD NMOSFET is a surface device with an N^+ poly-Si gate. The gate oxide thickness ($T_{\rm ox}$) of the device is 1.4 nm with decoupled-plasma-nitridation (DPN) processing. The devices have a gate length of $L_{\rm g}$ = 90 nm, width of W = 2 μm and the effective channel of $L_{\rm eff}$ = 75 nm. For these devices, $V_{\rm th}$ = 0.28 V. Figure 1 shows the cross section of the device.

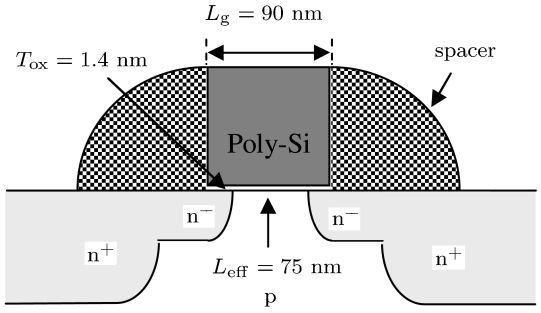


Fig.1. Cross section of the LDD-NMOSFET used in this paper.

The samples were stressed using the LGV stress at $V_{\rm g} = V_{\rm th}$ and various fixed values of $V_{\rm d}$ (2.1, 2.2, 2.3, 2.4, and 2.5 V). During the stress, the source and substrate were grounded ($V_{\rm s} = V_{\rm sub}$ = 0 V). $I_{\rm g} - V_{\rm g}$ and $I_{\rm d} - V_{\rm d}$ characteristics were measured before and after stresses. In selected time intervals (i.e. 50, 100, 200, 300, 400 and 500s), the electrical parameters of device $V_{\rm th}$, transconductance ($G_{\rm m}$), $I_{\rm dlin}$ and $I_{\rm dsat}$ are monitored. To assist in analysing the features of damage resulting from hot holes at the interface in the LDD region, the GIDL currents before and after stresses were measured at $V_{\rm d}$=1.2V by sweeping $V_{\rm g}$ from 0 to −2.0 V. All the stresses and measurements were performed under light-tight and electrically-shielded condition at room temperature, using an HP4156B precision semiconductor parameter analyser.

In addition, SILVACO software was applied to simulating the lateral field under the stress condition in the device.

3. Results and discussion

Figure 2 shows $G_{\rm m} - V_{\rm g}$ and $I_{\rm d} - V_{\rm g}$ curves before and after LGV stresses at $V_{\rm g} = V_{\rm th}$ and various fixed values of $V_{\rm d}$. It can be seen that the $G_{\rm mmax}$ and $I_{\rm d}$ decrease with increasing stress time varying from 50 to 500 s. It can also be seen that the reductions in $G_{\rm mmax}$ and in $I_{\rm d}$ are enhanced with increasing $V_{\rm d}$ after the LGV stress. During the first 50s stress, the rate of the degradation is the fastest. Afterwards, it becomes slower. Figure 3 shows $I_{\rm d} - V_{\rm d}$ characteristics before and after the LGV stresses. As the stress continues, $I_{\rm d}$ curves shift downwards. In the conventional NMOSFETs, the trapped holes and interface states exist under the LGV ($V_{\rm g} = V_{\rm th}$) stress. The holes trapping on the corner of the drain shorten the effective channel and thus they enhance $I_{\rm d}$, while the interface states reduce $I_{\rm d}$ due to mobility degradation. However, the effect of holes clearly dominates and it masks the influence of interface state on $I_{\rm d}$.[4] Therefore, a net $I_{\rm d}$ increase is observed after the LGV stress. But this phenomenon is not in agreement with that of our experiments.

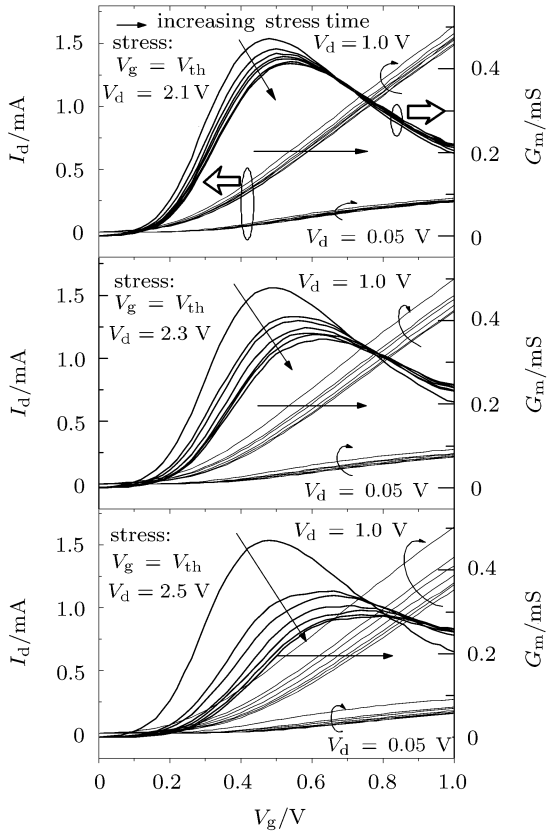


Fig.2. $I_{\rm d} - V_{\rm g}$ and $G_{\rm m} - V_{\rm g}$ before and after LGV stresses at $V_{\rm g} = V_{\rm th}$ with various fixed values of $V_{\rm d}$. Stress time ranges from 50 to 500 s (i.e. 50, 100, 200, 300, 400 and 500 s). $V_{\rm g} = V_{\rm th}$ = 0.28 V.

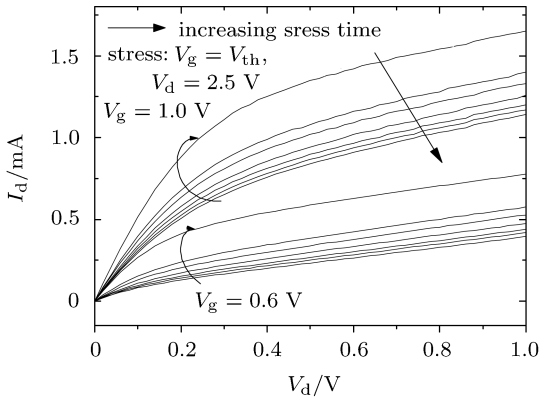


Fig.3. $I_d - V_d$ characteristics before and after the LGV stresses. Stress time from 50 to 500 s (i.e. 50, 100, 200, 300, 400 and 500 s). $V_g = V_{th} = 0.28$ V.

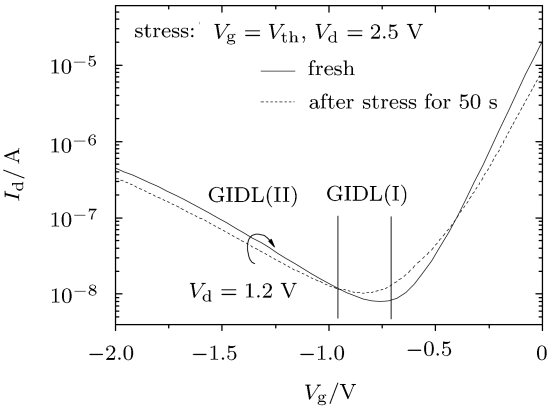


Fig.4. GIDL current before and after LGV stresses for 50 s. $V_{th} = 0.28$ V.

In order to understand this disagreement, the damage under the LGV($V_g = V_{th}$) stress in LDD device must be known. Because the GIDL current is very sensitive to the trapped charge and the interface states at the interface in the gate-to-LDD region, we investigate the damage through the analysis of GIDL current before and after stresses. For NMOSFETs, all the interface states become neutral at high values of V_{dg}, thus only the oxide trapped charges affect the GIDL current.[6] But at low values of V_{dg}, interface states alter the GIDL current by introducing a trap-assisted leakage component.[7] In Fig.4, the GIDL current increases at the low values of V_{dg} (GIDL(I) region), which indicates that interface states generated during the LGV stress which assists in band-to-band tunnelling. Meanwhile, GIDL current decreases at the high values of V_{dg} (GIDL(II) region). This fact gives the evidence that the holes are trapped in the oxide during the LGV stress. These trapped holes at the interface depress energy band bending of Si at interface in the gate-to-LDD region. As a result, the electron tunnelling length from valance band to conductance band becomes longer and the GIDL current decreases. From the above analysis, it is concluded that hot holes are injected into interface and generate interface states under the LGV ($V_g = V_{th}$) stress.

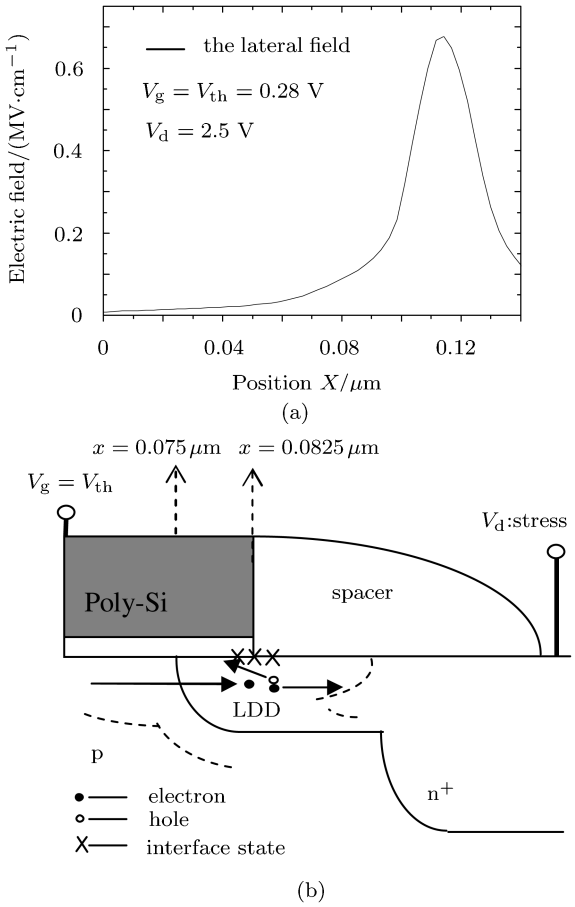


Fig.5. LDD-NMOSFET ($T_{ox} = 1.4$ nm, $L_g = 90$ nm, $L_{eff} = 75$ nm) (a) Distribution of the lateral field along channel simulated with SILVACO under LGV stress condition. (b).Illustration of LDD-NMOSFET. The hot holes are created by impact-ionization under LGV stress condition. They are injected into oxides and create additional degradation.

Although the trapped holes exist, I_d in on-state decreases (Fig.2 and Fig.3). This case differs from that of conventional device. The decrease in I_d can be explained as follows. In the ultra-short gate and ultra-thin gate oxide LDD-NMOSFETs the maximal lateral field occurs in the LDD region under the LGV ($V_g = V_{th}$) stress. Figure 5(a) shows the distribution of the lateral fields along the channel of the device. During stressing, the impact-ionization induced by energetic electrons from the channel does not occur on the corner of drain, but around the maximal lateral

field in the LDD region as shown in Fig.5(b). The hot holes generated in the impact-ionization process are injected into the oxide in the field direction by the strong lateral field. In this way, a lot of trapped holes and interface states are formed at the interface around the gate-to–LDD region. These trapped holes, however, are located in the LDD region and they cannot expand the drain to the channel. So they cannot mask the influence of interface states on $I_{\rm d}$. Moreover, these trapped holes do increase the resistance of the LDD region with interface states, which results in an decrease in the drain current after stress(shown in Fig.2 and Fig.3). In addition, part of these hot holes create some traps in the oxide when they directly pass through the ultra-thin gate oxide even though the energy is not high enough to surmount the gate oxide barrier. So these traps and interface states enhance the gate current $I_{\rm g}$, as shown in Fig.6.

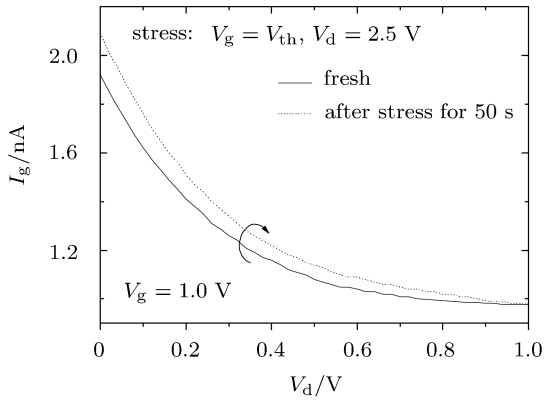


Fig.6. $I_{\rm g} - V_{\rm d}$ before and after the LGV stresses for 50 s. $V_{\rm th}$=0.28V.

Figure 7 shows the degradations of $V_{\rm th}$ and $G_{\rm mmax}$ as functions of stress time. The shift of $V_{\rm th}$ is positive, while that of $G_{\rm mmax}$ is negative. For conventional NMOSFET, the $V_{\rm th}$ shifts negatively after LGV ($V_{\rm g} = V_{\rm th}$) stress.[4] In LDD-NMOSFETs, $I_{\rm d}$ decreases after the LGV stress. Therefore, $V_{\rm g}$ becomes larger when $I_{\rm d} = 0.1$ μA $\times(W/L)$. In other words, the $V_{\rm th}$ becomes large ($V_{\rm th}$ is defined as V_g when $I_{\rm d} = 0.1$ μA$\times(W/L)$ with $V_{\rm d} = 0.05$ V). Under the LGV ($V_{\rm g} = V_{\rm th}$) stress, the $V_{\rm th}$ and $G_{\rm mmax}$ degradations increase with drain bias $V_{\rm d}$, but are less sensitive to $V_{\rm d}$ than at lower values of $V_{\rm d}$ as indicated by smaller slope under high values of $V_{\rm d}$ of Fig.7. It can be seen that the degradation of $V_{\rm th}$ is obviously larger than that of $G_{\rm mmax}$.

Figure 8 shows the degradations of $I_{\rm dlin}$ (measured at $V_{\rm g} = 1$ V, and $V_{\rm d} = 0.1$ V, and $I_{\rm dsat}$ (measured at $V_{\rm g} = 1$ V, and $V_{\rm dsat} = V_{\rm d} - V_{\rm th} = 0.82$ V) as functions of stress time in $I_{\rm d} - V_{\rm d}$ characteristics. The $I_{\rm dlin}$ degradation is larger than the $I_{\rm dsat}$ degradation, and the $V_{\rm th}$ and $G_{\rm mmax}$ degenerate with increasing stress time. It can be seen from Fig.6 and Fig.7 that the degradations of these four kinds of electronic parameters are still consistent with those from the conventional degradation model of $\Delta = Kt^n$ in Ref.[8], where n is the degradation slope. In Figs.7 and 8, the n of $V_{\rm th}$ is about $0.31 - 0.41$, the n of $G_{\rm mmax}$ is between 0.24 and 0.36, and n values of $I_{\rm dlin}$ and $I_{\rm dsat}$ are $0.26 - 0.39$. The above values of n are smaller than either the values ($0.5 - 0.6$ in Ref.[8]) of conventional long-channel device or the value (~ 0.8 in Ref.[3]) of long-channel LDD device with thick gate oxide.

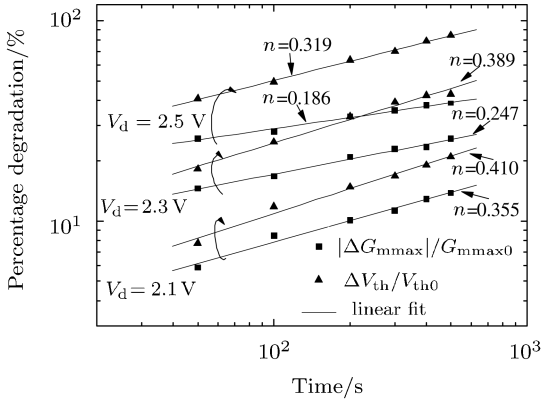


Fig.7. The degradations of $V_{\rm th}$ and $G_{\rm mmax}$ as functions of stress time under the LGV stress at $V_{\rm g} = V_{\rm th}$ with various fixed values of $V_{\rm d}$.

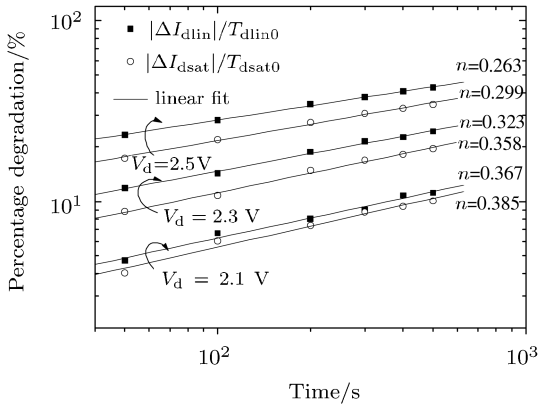


Fig.8. The degradations of $I_{\rm dlin}$ and $I_{\rm dsat}$ as functions of stress time under LGV stress at $V_{\rm g} = V_{\rm th} = 0.28$ V with various fixed drain biases $V_{\rm d}$. The degradations of $V_{\rm th}$, $G_{\rm mmax}$, $I_{\rm dlin}$ and $I_{\rm dsat}$ as functions of $1/V_{\rm d}$ under the LGV stress at $V_{\rm g} = V_{\rm th}$.

Figure 9 shows the degradations of $V_{\rm th}$, $G_{\rm mmax}$, $I_{\rm dlin}$, $I_{\rm dsat}$ as functions of $1/V_{\rm d}$ after the 50 s LGV stress at $V_{\rm g} = V_{\rm th} = 0.28$ V with various fixed values

of $V_{\rm d}$ (2.1, 2.2, 2.3, 2.4, and 2.5 V). The degradations exhibit two parts depending on drain bias $V_{\rm d}$. The degradations in the $1/V_{\rm d}$ $(0.417 - 0.476)$ region vary linearly with $1/V_{\rm d}$, and the slopes in this region are apparently larger than those of the $1/V_{\rm d}$ $(0.40-0.417)$. Because $\Delta = A{\rm e}^{B/V_{\rm d}}$,[9] where B reflects the rate of degradation. It is seen that the rate of degradation before the drain bias $V_{\rm d} = 2.4$ V $(1/V_{\rm d} = 0.417)$ is larger than that after $V_{\rm d} = 2.4$ V in Fig.9. The results are consistent with the results shown in Fig.7 and Fig.8 that the n becomes small as drain bias $V_{\rm d}$ increases in the LGV $(V_{\rm g} = V_{\rm th})$ stress setting. It can also be seen that the comparison of degradations among $V_{\rm th}$, $G_{\rm mmax}$, $I_{\rm dlin}$ and $I_{\rm dsat}$ shows $\Delta V_{\rm th}/V_{\rm th0} > |\Delta G_{\rm mmax}|/G_{\rm mmax0} > |\Delta I_{\rm dlin}|/I_{\rm dlin0} > |\Delta I_{\rm dsat}|/I_{\rm dsat0}$.

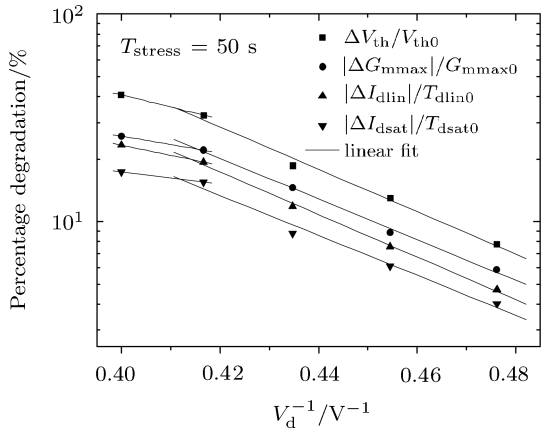


Fig.9. The degradations of $V_{\rm th}$ $G_{\rm mmax}$ $I_{\rm dlin}$ and $I_{\rm dsat}$ as functions of $1/V_{\rm d}$ under the LGV stress at $V_{\rm g} = V_{\rm th}$.

Based on the above discussion, it is concluded that the degradation of the ultra-short gate length LDD NMOSFET with ultra-thin gate oxide under LGV stress accords with the conventional device degradation model. But if we define the 10% degradation as the criterion of the ultra-short channel and ultra-thin gate oxide LDD device's failure, the $V_{\rm th}$ degradation should be the optimal choice to describe the degradation of device because it is the largest among the four kinds of the degradation parameters above in device.

4. Conclusion

The degradation of the 90 nm gate length LDD NMOSFET with ultra-thin gate oxide under the LGV stress $(V_{\rm g} = V_{\rm th})$ has been investigated. It is found that the drain current decreases and the $V_{\rm th}$ shift is positive after the LGV$(V_{\rm g} = V_{\rm th})$ stress. The results differ from the degradations of conventional NMOSFET under the LGV$(V_{\rm g} = V_{\rm th})$ stress that the drain current increases and the $V_{\rm th}$ shift is negative.

We take advantage of characteristics of the GIDL current to analyze the damage generated during the stress. It is confirmed that the degradation of the drain current is still attributed to the hot holes in ultra-short gate length and ultra-thin gate oxide LDD-NMOSFETs. However, these holes are trapped at the interface of gate-to-LDD overlap region in LDD due to the maximal lateral field located in the LDD. Then these trapped holes cannot shorten the channel to mask the influence of interface states on $I_{\rm d}$. Furthermore, they increase the resistance of LDD region with interface states so that the decrease in $I_{\rm d}$ and increase in $V_{\rm th}$ are displayed. In addition, this paper discusses the degradations of $V_{\rm th}$, $G_{\rm mmax}$, $I_{\rm dlin}$ and $I_{\rm dsat}$ in the 90 nm gate length LDD-NMOSFET with 1.4 nm gate oxide under the LGV stress at $V_{\rm g} = V_{\rm th}$ with various drain biases. The $V_{\rm th}$ degradation is the largest among the degradations of the four parameters. Furthermore, the degradation slopes (n) of these four kinds of degradation parameters range from 0.21 to 0.41. The value of n is less than that of conventional device and also that of the long gate length LDD device.

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