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# Corner effects in double-gate/gate-all-around MOSFETs*

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Two kinds of corner effects existing in double-gate (DG) and gate-all-around (GAA) MOSFETs have been investigated by three-dimensional (3D) and two-dimensional (2D) simulations. It is found that the corner effect caused by conterminous gates, which is usually deemed to deteriorate the transistor performance, does not always play a negative role in GAA transistors. It can suppress the leakage current of transistors with low channel doping, though it will enhance the leakage current at high channel doping. The study of another kind of corner effect, which exists in the corner at the bottom of the silicon pillar of DG/GAA vertical MOSFETs, indicates that the D-top structure with drain on the top of the device pillar of vertical transistor shows great advantage due to lower leakage current and better DIBL (drain induced barrier lowering) effect immunity than the S-top structure with source on the top of the device pillar. Therefore the D-top structure is more suitable when the requirement in leakage current and short channel character is critical.

**Keywords:** GAA, DG, DIBL, S-top, D-top, corner effect

**PACC:** 7280C, 7340R, 7360J

## 1. Introduction

Double-gate and gate-all-around (also called surrounding gate) MOSFETs are promising architectures for transistors under 50 nm, for they can extend the scalability of CMOS technology due to inherent short-channel effect (SCE) immunity and provide almost ideal subthreshold slope and high current drive,[1−4] which makes them suitable for high-density, low-voltage and low-power memory and conventional CMOS applications.

However, there are two kinds of corner effects in DG and GAA MOSFETs that may influence their performance. The first kind of corner effect exists in gate-all-around transistors, as shown in Fig.1(a).

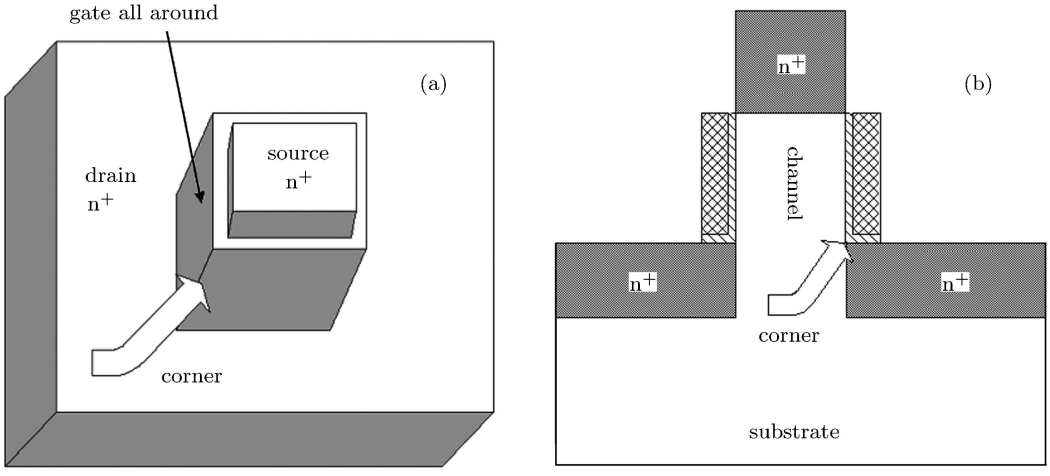



**Fig.1.** Schematic diagram of the two kinds of corner effects in GAA/BG transistors: (a) corner effect caused by conterminous gate in GAA MOSFET, (b) corner effect that exists at the corner of the bottom of the silicon pillar of DG/GAA vertical MOSFET.

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Though the GAA transistor has high driving current and better controllability of channel since the width of gates are increased, the four corners formed by the conterminous gates may affect the electric field and surface potential in the corner region of the channel, like in the grooved-gate MOSFET.[5,6] In certain triple-gate MOSFETs, this corner effect is known to result in lower threshold voltage and a larger leakage current.[7,8] In this paper, this kind of corner effect is further investigated and it is found that for GAA vertical transistor with gate length of 50 nm, this corner effect is not always negative for the performance of the transistor.

The other kind of corner effect is shown in Fig.1(b), at the bottom of the silicon pillar of DG/GAA vertical MOSFETs, near the source (in D-top structure) or the drain (in S-top structure). The influence of this kind of corner has also been studied in this paper for the first time and is analysed to give some guidelines for making choice of structures of vertical MOSFETs.

## 2. Simulation and analysis

### 2.1. Corner effect caused by conterminous gate

The corner effect caused by conterminous gates is studied in this section. The 2D cross-section view of the simulated GAA and DG transistors between the source and drain is shown in Fig.2.

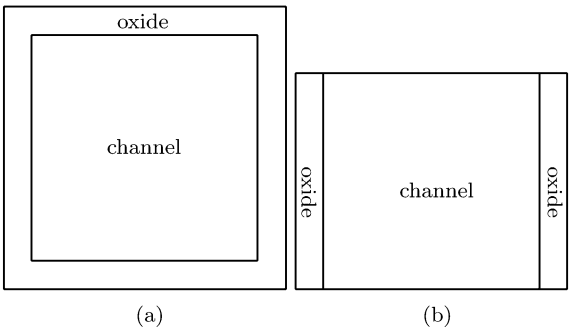



**Fig.2.** Cross sections of the GAA and DG transistors in the middle of the gate: (a) GAA transistor. (b) DG transistor.

Either section of the channel is assumed to be a square with four equal sides of 30 nm. The gate length is 50 nm and the gate oxide thickness is 1.5 nm. A midgap metal gate ($\Phi_{\rm M} = 4.6$ V) is used for $V_{\rm th}$ control. 3D device simulations have been performed using the DESSIS device simulator of ISE. Considering the quantization effect in the MOSFETs, the density gradient model,[9] which can describe both 2D and 3D quantization effect, is adopted. In order to include quantization effect in simulation, an additional potential parameter $\Lambda$ is introduced to the classical density formula for modification, as shown in Eq.(1):

$$n = N_{\rm c} \exp\left(\frac{E_{\rm F_n} - E_{\rm c} - \Lambda}{kT}\right), \tag{1}$$

where $n$ is the electron density, $T$ the carrier temperature, $k$ the Boltzmann constant, $N_{\rm c}$ the conduction band density of states, $E_{\rm c}$ the conduction band energy, and $E_{\rm F_n}$ the electron Fermi energy. In the density gradient model we used, the parameter $\Lambda$ is given as

$$\begin{aligned}\Lambda = & -\frac{\gamma h^2}{12m}\left\{\nabla^2 \log n + \frac{1}{2}(\nabla \log n)^2\right\} \\ = & -\frac{\gamma h^2}{6m}\frac{\nabla^2\sqrt{n}}{\sqrt{n}},\end{aligned} \tag{2}$$

where $\hbar = h/(2\pi)$ is the reduced Planck constant, $m$ is the density of state mass, and $\gamma$ is a fitting factor.

Figure 3 shows the off-state current ($I_{\rm off}$) and the on-state current ($I_{\rm on}$) of GAA and DG transistors for various channel doping. It can be seen that $I_{\rm on}$ of GAA transistor is higher than that of DG transistor in all simulated cases due to the significantly increased channel width, no matter whether the channel doping is low or high.

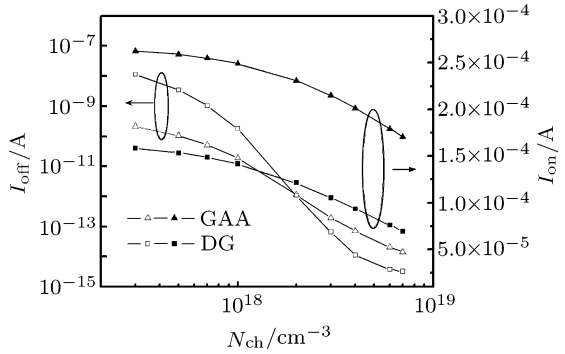



**Fig.3.** $I_{\rm on}$ and $I_{\rm off}$ of GAA and DG transistor for various channel doping. For low channel doping, GAA transistor has lower $I_{\rm off}$ than DG transistor, though GAA transistor has higher $I_{\rm off}$ than DG transistor when channel doping is high.

However, $I_{\rm off}$ of GAA transistor is not always higher than that of DG transistor. For low channel doping, GAA transistor has lower $I_{\rm off}$ than DG transistor, though GAA transistor with high channel doping has higher $I_{\rm off}$ than DG transistor. To clarify the physical

mechanism of the different relative results of $I_{\rm off}$ for high and low channel doping, the electron distribution along one side of the 2D cross section of channel in the middle of the gate of GAA transistor (as shown in Fig.2(a)) is shown in Fig.4. Figure 4(a) shows the electron distribution for channel doping of $5.0\times10^{17}\,{\rm cm}^{-3}$, which is typical for low channel doping. It can be seen that when the gate voltage is zero, the electron density in the corner region is $2.6\times10^{11}\,{\rm cm}^{-3}$, i.e., 44% lower than that in the middle of the channel surface, which is $4.7\times10^{11}\,{\rm cm}^{-3}$. This can explain the reduced leakage current in the device. In contrast, for channel doping of $4.0\times10^{18}\,{\rm cm}^{-3}$, which is typical for high channel doping, when the gate voltage is zero, the electron density in the corner, which is $4.4\times10^{10}\,{\rm cm}^{-3}$, is higher than that in the middle of the surface, which is $1.8\times10^{9}\,{\rm cm}^{-3}$, as shown in Fig.4(b).

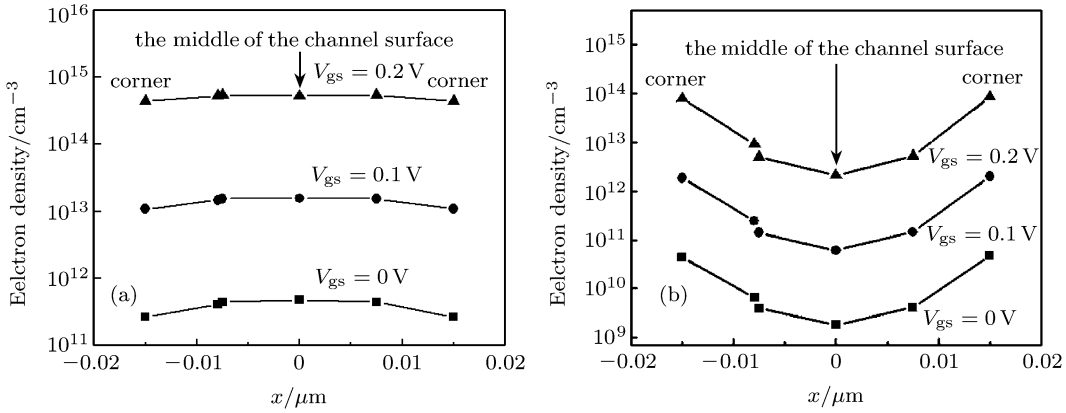



**Fig.4.** Electron distribution along one side of the cross section of channel in the middle of the gate of GAA transistor: (a) $N_{\rm ch}=5.0\times10^{17}\,{\rm cm}^{-3}$. The electron density in the corner region is lower than that in the middle of the channel surface. (b) $N_{\rm ch}=4.0\times10^{18}\,{\rm cm}^{-3}$. The electron density in the corner region is higher than that in the middle of the channel surface.

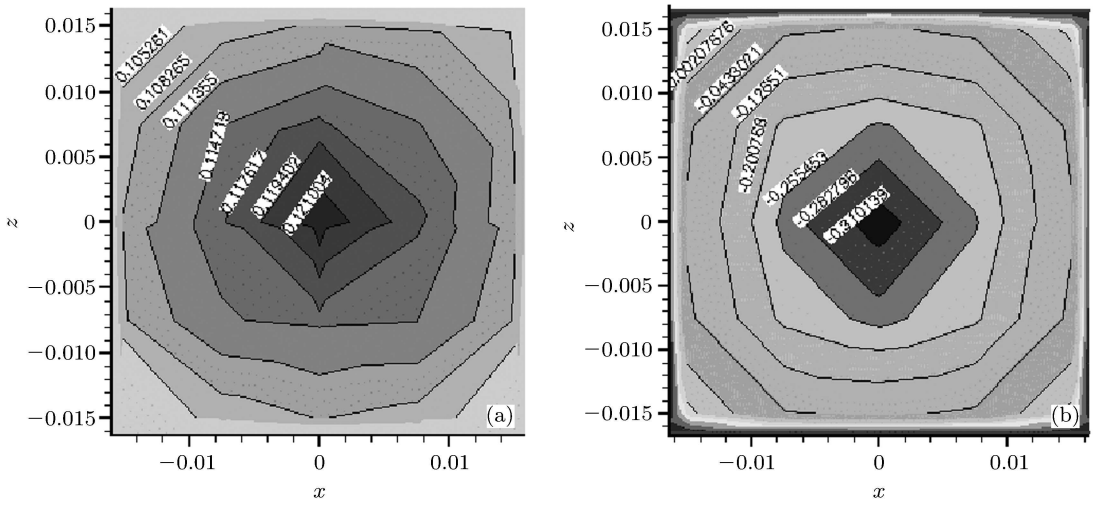



**Fig.5.** Electrostatic potential distribution in the cross section of channel in the middle of the gate when $V_{\rm gs}=0\,{\rm V}$: (a) $N_{\rm ch}=5.0\times10^{17}\,{\rm cm}^{-3}$. (b) $N_{\rm ch}=4.0\times10^{18}\,{\rm cm}^{-3}$.

Further analysis of the opposite roles the corner plays in the device with high and low channel doping is carried out by investigating the potential distribution at zero gate voltage. Figure 5(a) shows the potential distribution in the cross section of channel in the middle of the gate for channel doping of $5.0\times10^{17}\,{\rm cm}^{-3}$. It can be seen that the potential rises from the surface to the centre of the channel, that is to say, the bands at the surface bend upward. Because of the shape of the corner, this effect will be strengthened at the corner, therefore the electric field there is stronger than in other regions of the surface, resulting in lower potential in the corner region, compared with the surface outside it. Since the inversion-electron density

is determined by the condition of the surface energy band, the lower potential at the corner will cause diminished electron density in the corner region. However, for high channel doping, say $4.0 \times 10^{18}\,\mathrm{cm}^{-3}$, the case is the opposite. As shown in Fig.5(b), the potential decreases from the surface to the centre of the channel and bands at the surface bend downward. Therefore the shape of the corner will cause higher potential in the corner region than in the surface outside it. As a result, the electron density at the corner will be higher, too. The above analysis is in agreement with the electron distribution shown in Fig.4.

## 2.2. Corner effect in S-top and D-top structures

Another corner effect existing in the corners at the bottom of the silicon pillar of DG/GAA vertical MOSFETs is studied by 2D simulations of S-top and D-top structures of DG vertical transistors having gate length of 100 nm. Figure 6 shows the $I_{\mathrm{on}}$ and $I_{\mathrm{off}}$ of these two structures under different channel dopings. The $I_{\mathrm{on}}$ of D-top structure is a little higher than the S-top structure, but the advantage is limited. However, it is found that the leakage current of D-top structure is distinctly lower than that of S-top structure when the channel doping is above $1.0 \times 10^{17}\,\mathrm{cm}^{-3}$. And the higher the channel doping, the more significant this advantage is. When channel doping is $1.0 \times 10^{18}\,\mathrm{cm}^{-3}$, the $I_{\mathrm{off}}$ of D-top structure is $5.35 \times 10^{-14}\,\mathrm{A}/\mu\mathrm{m}$, being only 0.75% of that of S-top structure, which is $7.10 \times 10^{-12}\,\mathrm{A}/\mu\mathrm{m}$. When channel doping is $2.0 \times 10^{18}\,\mathrm{cm}^{-3}$, this ratio reached as much as 0.28‰.

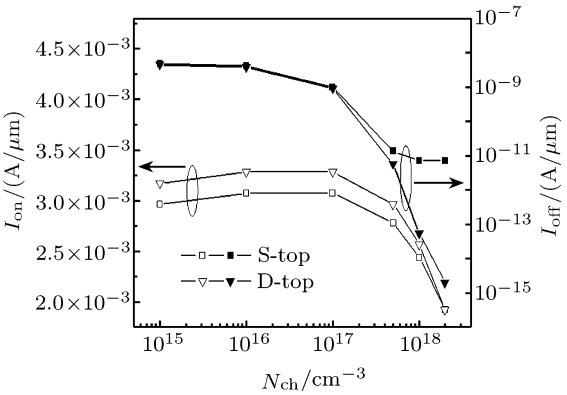



**Fig.6.** $I_{\mathrm{on}}$ and $I_{\mathrm{off}}$ versus channel doping of S-top and D-top structures. When channel doping is above $1.0 \times 10^{17}\,\mathrm{cm}^{-3}$, the leakage current of D-top structure is distinctly lower than that of S-top structure.

The reason lies in the potential barrier caused by the corner. Since gate control of the channel in the corner region is weakened, a potential barrier will be generated there, like the situation in recessed channel MOSFETs.[10] Also, the barrier will rise when the channel doping is increased.[11] This kind of barrier is at the drain side in S-top structure while is at the source side in D-top structure. The leakage current greatly depends on the barrier at the source side, therefore the leakage current of D-top structure is much lower than that of S-top structure and becomes apparently reduced as the channel doping increases. When the channel doping is above $1.0 \times 10^{18}\,\mathrm{cm}^{-3}$, the leakage current of D-top structure is almost two orders of magnitude lower, compared with S-top structure.

The comparison of DIBL effect of these two structures at different levels of channel doping is shown in Fig.7. $\delta V_{\mathrm{th}}$ is defined as the difference between values of $V_{\mathrm{th}}$ at $V_{\mathrm{ds}} = 0.1$ and 1.5 V. It can be seen that D-top structure has smaller $V_{\mathrm{th}}$ variation than S-top in all cases. This is also caused by the potential barrier at the corner of the source end in D-top structure. The penetration of drain voltage is greatly weakened by the corner, therefore the potential in the source region is only slightly affected by the drain voltage. Figure 8 shows the potential distribution near the source junction of S-top and D-top structures, which illustrates this effect of corner. It can be seen that the potential near the source in D-top structure is pinned, while the potential near the source in S-top structure is heavily influenced by drain voltage.

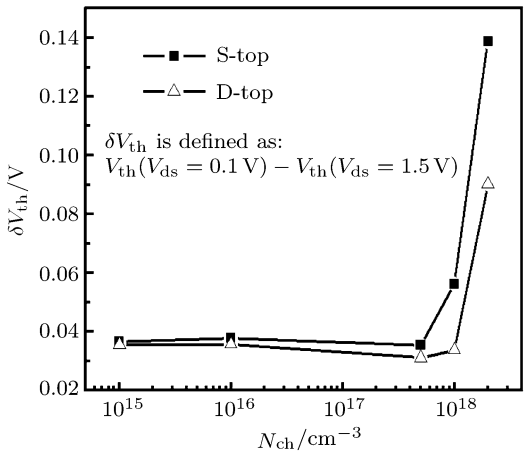



**Fig.7.** Comparison of DIBL effect of S-top and D-top structures.

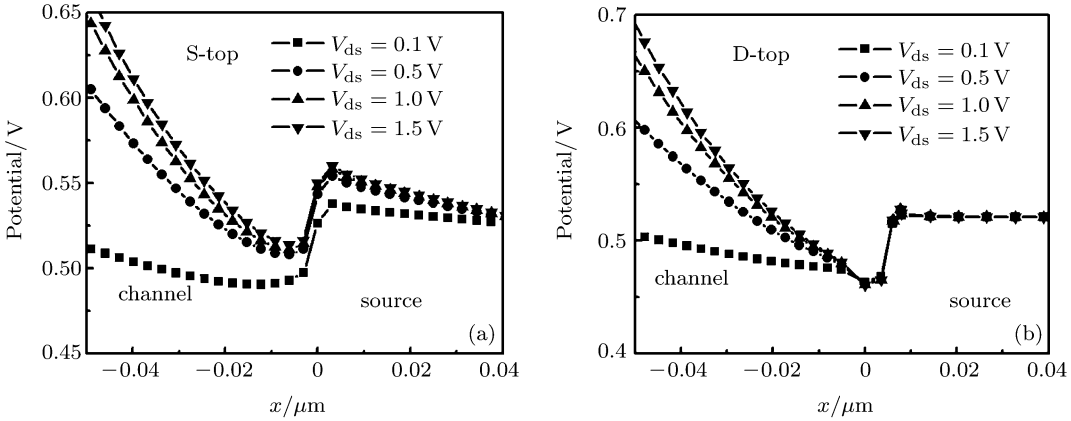



**Fig.8.** Potential distribution near the source junction: (a) S-top structure. The potential near the source is heavily influenced by drain voltage. (b) D-top structure. The potential near the source is pinned.

When the requirement of leakage current and short channel character is critical, D-top structure is more advantageous due to its low, leakage current and better suppression of DIBL effect caused by the corner effect.

## 3. Conclusion

Two kinds of corner effects in double-gate and gate-all-around MOSFETs are investigated in this paper. It is found and explained that GAA vertical transistor with low channel doping can reduce leakage current due to the corner effect caused by conterminous gate. This gives another reason for the preference of low doped device, besides the high mobility and low fluctuation it can provide. Moreover, due to the barrier generated by the corner at the bottom of the silicon pillar, D-top structure of vertical transistor shows better suppression of leakage current and the DIBL effect than the S-top structure does.

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