Vol 16 No 3, March 2007
1009-1963/2007/16(03)/0795-04
Chinese Physics
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Charge storage characteristics of hydrogenated nanocrystalline silicon film prepared by rapid thermal annealing*

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(Received 8 May 2006; revised manuscript received 28 September 2006)

The early stages of hydrogenated nanocrystalline silicon (nc-Si:H) films deposited by plasma-enhanced chemical vapour deposition were characterized by atomic force microscopy. To increase the density of nanocrystals in the nc-Si:H films, the films were annealed by rapid thermal annealing (RTA) at different temperatures and then analysed by Raman spectroscopy. It was found that the recrystallization process of the film was optimal at around 1000 °C. The effects of different RTA conditions on charge storage were characterized by capacitance–voltage measurement. Experimental results show that nc-Si:H films obtained by RTA have good charge storage characteristics for nonvolatile memory.

Keywords: nc-Si, hydrogenated nanocrystalline silicon, charge storage, rapid thermal annealing
PACC: 6170A, 7360, 7340Q

1. Introduction

Hydrogenated nanocrystalline silicon (nc-Si:H) films have been widely used in solar cells,[1] light emitting devices,[2] single electron memory,[3] and thin film transistors[4] for their unique material properties. Especially in the application of semiconductor charge storage devices, nanocrystalline silicon layer has the potential to replace the continuous thick poly-Si charge storage layer of traditional floating gate memory. It has the benefit of a separated storage mechanism, which can realize thinner tunnel oxide, lower operation voltage, and shorter writing time.[5] Normally, low-pressure chemical vapour deposition (LPCVD) is widely employed to deposit silicon nanocrystal layers.[6−9] The nc-Si:H films deposited by plasma-enhanced chemical vapour deposition (PECVD) are rarely used as charge storage layers due to the low density of silicon nanocrystals and the existence of partial amorphous silicon in the film. However, the amorphous silicon in nc-Si:H (or a-Si:H) films can turn into nanocrystalline silicon when the films are processed under proper conditions, such as high-temperature thermal annealing and laser annealing.[10−15] Moreover, rapid thermal annealing (RTA) can induce high-density, size-limited recrystallization in nc-Si:H film. This means that a nc-Si:H film can be easily changed into a nanocrystalline silicon layer to satisfy the requirements of a nonvolatile memory device. In the work reported in this paper, hydrogenated nanocrystalline silicon films deposited by PECVD were recrystallized under RTA processes. Capacitance–voltage ($C-V$) measurements were used to characterize the influence of nc-Si:H films obtained at different RTA temperatures on charge storage. The experimental results show that the nc-Si:H films obtained by RTA had good charge storage characteristics.

2. Experiments

The nc-Si:H films were deposited on SiO_2 (2.5 nm)/p-Si(100) substrate using radio frequency (RF,13.56MHz) PECVD. They had a crystalline volume fraction (X_c) of over 40% and were grown under the following conditions, which we collectively denote

*Project supported by the National Basic Research Program of China (973 Program) (Grant No 2006CB302706) and the National Natural Science Foundation of China (Grant Nos 90607022, 90401002, 90207004, and 60506005).
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by 'condition A': H_2 dilution ratio ($R = H_2/SiH_4$) ~ 99, deposition pressure ~ 120 Pa, deposition temperature ~ 250 °C, negative bias voltage ~ 220 V, and RF power density ~ 0.8 W/cm^2. The reference samples, which were completely a-Si:H films, were fabricated under the same conditions except for the following differences, which we collectively denote by 'condition B': the negative bias voltage and RF power density were changed to 50 V and 1.6W/cm^2. During the fabrication, film thickness could be monitored in situ by a film thickness measurement instrument. The surface morphologies of the nc-Si:H films were characterized by atomic force microscopy (AFM). Then the RTA processes were carried out under N_2 atmosphere at a heating rate of 120 °C/s. Finally, 20 nm of control oxide and Al were deposited and evaporated, separately, on top of the nc-Si:H film to form a metal–oxide–nanocrystal–oxide–silicon structure for the $C-V$ measurement. The area of the MIS (metal–insulator–silicon) capacitor was 0.1 mm^2, and the $C-V$ measurements were performed with an HP 4284A.

3. Results and discussion

The AFM images of the thin nc-Si:H films deposited under condition A, with thicknesses of 10 and 20 nm, are shown in Figs.1(a) and 1(b), respectively. Nanocrystalline silicon dots can be seen, which could be single silicon nanocrystals or clusters of several nanocrystals. For the 10 nm nc-Si:H film, the statistical values of the nanocrystalline silicon dots are: diameter ~(15 to 30) nm, height ~ (1 to 3) nm, and density ~ 1×10^{10}/cm^2. For the 20 nm film, the dot diameter and the height increase as the density decreases. This means that the dot density will decrease with the increase of the film thickness in the early stages of the growth of nc-Si:H films. But this trend will not continue, and stacks of silicon nanocrystal dots will appear when the film thickness reaches a certain value. In order to observe the obvious memory characteristics, the 10 nm-thick nc-Si:H films are chosen here for $C-V$ measurements.

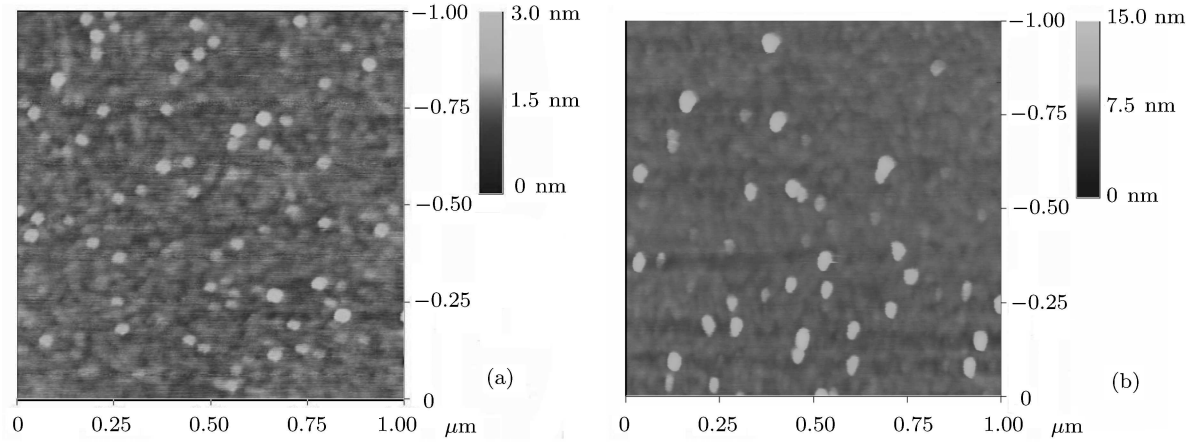


Fig.1. AFM images of nc-Si:H film surface. (a) 10 nm film thickness, (b) 20 nm film thickness.

First, the optimal crystallized temperature should be found so that it can be used to recrystallize nc-Si:H films and improve the silicon nanocrystal density in the films. In order to do this, 200 nm-thick a-Si:H films were deposited on quartz substrate under condition B and subjected to RTA. Raman measurement was then used to characterize the results of the RTA processes so as to choose a suitable annealing condition. The reason for using quartz substrate was to avoid the influence of Si substrate during the Raman measurements. Figure 2 shows the Raman spectra of the deposited films at different RTA temperatures. We cannot see a clear and sharp Raman peak from the sample without annealing, as shown in curve *a* in Fig.2, since there are no nanocrystals in the film. Furthermore, no distinct Raman peaks of silicon crystal can be seen when the RTA temperature is 800 °C and the annealing time is 30 s or 90 s, as shown in

curve b, which is similar to curve a. Hazra *et al*[16] also claimed that 4 nm a-Si:H film would not crystallize under RTA at 800 °C. However, clear Raman peaks of silicon crystal appear when the RTA temperature is 1000 °C and the annealing time is 30 s. With the prolonging of the annealing time to 90 s at 1000 °C, a sharper Raman peak of crystallized silicon can be observed, which indicates better crystallization. The size of a silicon crystal could be determined to be 5 nm from the Raman peak shift using the formula $d = 2\pi(B/\Delta\omega)^{1/2}$, where d is the diameter, B a constant (2.12 $\mathrm{nm^2{\cdot}cm^{-1}}$), and $\Delta\omega$ is the Raman peak shift. Hence, we have determined the optimal annealing temperature to be 1000 °C for crystallization.

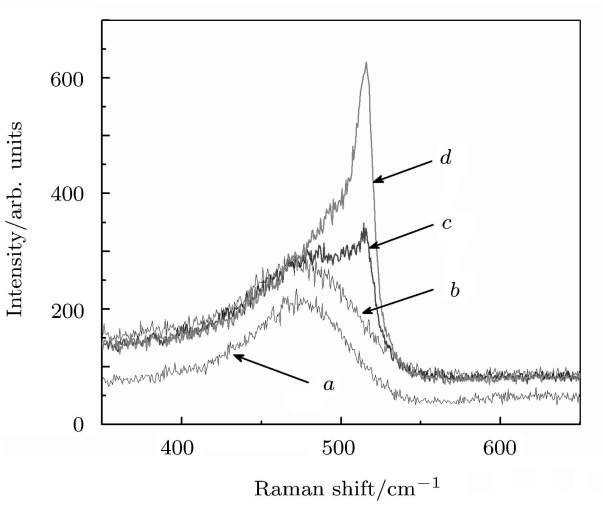


Fig.2. Raman spectrogram for various samples at different annealing temperatures. (a) as-deposited, (b) 800 °C (30 s) RTA, (c) 1000 °C (30 s) RTA, (d) 1000 °C (90 s) RTA.

The charge storage characteristics of nc-Si:H films deposited under condition A were evaluated by $C-V$ measurement using 10 nm-thick film samples. The dc voltage scan range was from −8 to 2 V. Figure 3 shows the $C-V$ hysteresis curves for different RTA temperatures and different annealing times. The sample without annealing has a small flat band voltage shift (−0.4 V), which might be caused by a low silicon nanocrystal density. Then the RTA process was used to obtain higher crystalline density for the nc-Si:H films. Because the annealing time was short, the growth of silicon nanocrystals was limited. Moreover, the oxide interfaces in the nc-Si:H film also restrained crystal growth. The $C-V$ hysteresis loop for the sample annealed at 800 °C is similar to that of the non-annealed sample. For the RTA temperature of 1000 °C, as the annealing time changed from 30 to 60 s, the flat band voltage changed from 1.2 to 1.6 V. However, it did not change further for the annealing time of 90 s. It seems that extending the annealing time beyond 60 s does not improve the charge storage characteristics of nc-Si:H film any more. Therefore we conclude that RTA at 1000 °C for 60 s is the optimal condition for the recrystallization of 10 nm nc-Si:H film. The centre of the hysteresis curves is near −3 V, which, in principle, should be near 0 V. The difference might be caused by an excess of immobile charges remaining in the 20 nm control oxide layer, which can be partly eliminated by optimizing the fabrication process.

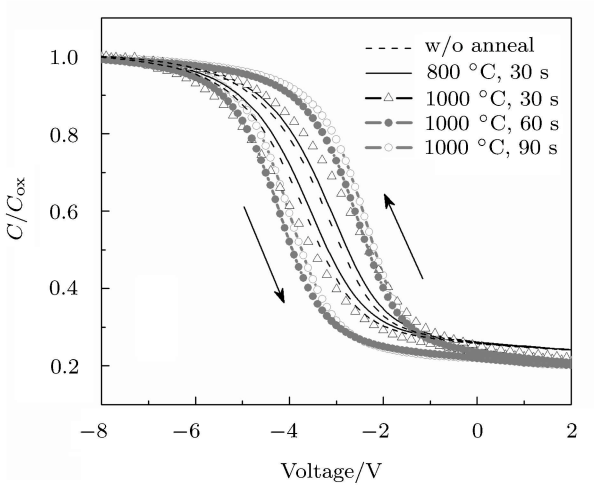


Fig.3. The $C-V$ hysteresis under −8 V and 2 V bidirectional scan for samples at different annealing temperatures.

$C-V$ measurements under different scan voltages were performed for the further analysis of charge trap characteristics. For the thinner tunnel oxide (2.5 nm), a direct tunnelling mechanism explains the electron injection from the channel into the nc-Si (write operation) or the driving-out of the trapped electrons from the nc-Si into the channel (erase operation). When applying a positive gate voltage to the device, electrons in the channel will tunnel into the nanocrystalline silicon layer and be blocked by the control oxide (20 nm); when applying a negative voltage, electrons will escape from the nc-Si layer. For the p-type silicon substrate, the $C-V$ curve will shift to the right because of the negative charges stored in the nc-Si floating gate when the scan range starts from a positive voltage. The right shift will be larger when the applied positive gate voltage increases. Correspondingly, the $C-V$ curve will shift to the left when the scan range starts from

a negative voltage.

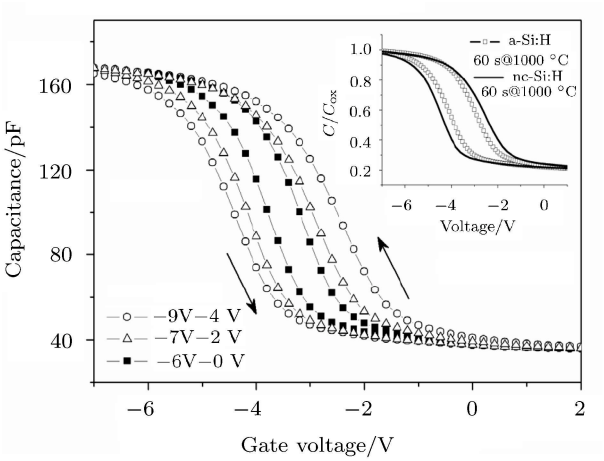


Fig.4. The threshold voltage shifts for different scan voltages. The inset $C-V$ curves were measured under a -8 V to 3 V bidirectional scan range and show the comparison between the nc-Si:H film and a-Si:H film samples, which were subjected to the same RTA process.

Figure 4 shows the $C-V$ curves of RTA samples annealed for 60 s at 1000 °C. As the scan range changes from $-6-0$ V to $-8-4$ V, the flat band voltage shift increases from 0.6 to 1.9 V, as shown in Fig.4, which indicates that the nc-Si:H film subjected to the RTA process has good charge trap characteristics. The inset in Fig.4 shows a $C-V$ comparison between the nc-Si:H film and a-Si:H film, which had the same thickness (10 nm) and were subjected to the same RTA process for 60 s at 1000 °C. Corresponding to the same scan voltage range ($-8-3$ V), the nc-Si:H film has a larger flat band voltage shift. The reason for this phenomenon might be that there are more nucleated centres in the nc-Si:H film, which can result in a higher nanocrystalline density than the a-Si:H film under the same RTA processing conditions.

4. Conclusions

In conclusion, RTA helps to increase the density of nanocrystals in hydrogenated nanocrystalline silicon (nc-Si:H) films deposited by PECVD. Raman spectroscopy analysis showed that RTA at 1000 °C is the optimal processing condition for the recrystallization of the film. It was found that nc-Si:H film subjected to this optimal condition has better charge storage characteristics for the nonvolatile memory.

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