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Investigation of gate current in nano-scale MOSFETs by Monte Carlo solution of quantum Boltzmann equation*

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This paper investigates gate current through ultra-thin gate oxide of nano-scale metal oxide semiconductor field effect transistors (MOSFETs), using two-dimensional (2D) full-band self-consistent ensemble Monte Carlo method based on solving quantum Boltzmann equation. Direct tunnelling, Fowler–Nordheim tunnelling and thermionic emission currents have been taken into account for the calculation of total gate current. The 2D effect on the gate current is investigated by including the details of the energy distribution for electron tunnelling through the barrier. In order to investigate the properties of nano scale MOSFETs, it is necessary to simulate gate tunnelling current in 2D including non-equilibrium transport.

Keywords: tunnelling, quantum effect, Monte Carlo, metal oxide semiconductor field effect transistor

PACC: 7335C, 1220D, 7115Q

1. Introduction

The continued scaling of the metal oxide semiconductor field effect transistor (MOSFET) has resulted in the use of ultra-thin gate oxides in order to achieve a good control of the inversion charge and to suppress short channel effects.[1] According to the 2005 International Technological Roadmap for Semiconductors, an equivalent SiO_2 gate dielectric thickness less than 1.5 nm will be required for sub-100-nm generation MOS devices. At such a thickness, tunnelling current leads to an exponential increase in gate current.[2−6] This increased current not only affects the device performance but also increases the stand-by power consumption. Thus investigating the gate current is important to optimizing and modelling the MOSFETs in nano scale. On the other hand, non-equilibrium transport plays a more and more dominant role in nanoscale MOSFETs. The electrons tunnelling through the barrier will increase with the proportion of carriers with higher energy in the inversion layer with quantum confinement. The pioneering work[7] has been done on the direct tunnelling through gate oxide in 70-nm gate length nMOSFETs by using Monte Carlo (MC) device simulation. They have used transfer-matrix method for solving the Schrödinger equation to calculate the transmission probability. However, their work did not include the quantum confinement to the carrier transport in the channel which is of great importance to the property of nano-scale MOSFETs. The tunnelling current was simulated by the constant effective mass approximation.[7] The influence of detailed band structure was not included which is extremely important to the transport of the carriers with higher energy in devices.

In this work, we simulate the gate tunnelling current by 2D ensemble full-band MC simulation[8] based on solving quantum Boltzmann equation (QBE). The 2D quantum mechanical (QM) effect can be simulated by this method.[9] The tunnelling energy of the carriers within the full-band MC simulation is approximated as that in Ref.[10]. Direct tunnelling (DT), Fowler–Nordheim (FN) tunnelling as well as the thermionic emission currents are all included at the same time in the calculation of total gate current. The 2D effect of MOSFET on the gate current can be simulated. The influence of hot carriers and even the non-equilibrium transport in nanoscale MOSFETs on

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the gate current can be investigated by this method. The simulation method is described in Section 2, and the simulated results are discussed in Section 3. The influence of drain voltage on gate current in nano-scale ultra-thin-body (UTB) MOSFET is investigated. The distribution of gate tunnelling current along the channel is obtained.

2. Simulation method

The 2D full-band self-consistent ensemble MC method to solve QBE[9,11] is used. Accurate band structure is of great importance for the gate tunnelling current calculation including channel hot electron injection. The full-band structure is obtained from empirical pseudo-potential calculation including spin-orbit interactions. Four conduction bands and three valence bands for Si and one conduction band for SiO_2 are involved. The transition rates for the various scattering processes are calculated based on Fermi's Golden rule. The acoustic and optical phonon scattering, the ionized impurity scattering, the impact ionization scattering are taken into account.[12,13] The deformation potentials of Si used in this work are the same as those described in Ref.[14]. An efficient model for electron surface roughness scattering in semiconductor/dielectric interface for MC device simulation compatible with quantum correction is used.[15] The barrier lowering due to the image force is neglected since the influence of the image force is still questionable.[3,6,16]

Figure 1 shows the schematic for electron tunnelling through gate dielectric. Electron energy below $E_{\rm L}$ will have a transmission probability through gate dielectric with DT. If electron energy is between $E_{\rm L}$ and $E_{\rm H}$ which is equal to 3.15 eV for SiO_2, electron will have a transmission probability through gate dielectric with FN tunnelling. When electron energy is greater than $E_{\rm H}$, thermionic emission occurs, and the transmission probability is taken as 1.

In our MC simulation, the tunnelling current through gate dielectric from semiconductor to metal is obtained by recording each electron tunnelling through gate dielectric during the simulation time. When an electron approaches to the semiconductor/dielectric interface, the transmission probability $T_{\rm E}$ is calculated in the Wentzel–Kramers–Brillouin (WKB) approximation for simplifying the barrier with various shapes. Figure 2 shows the calculated transmission probabilities for a metal-oxide-semiconductor (MOS) structure with 1-nm thick oxide. For comparison, the result obtained by using numerical solution of the envelope Schrödinger equation (transfer matrix method) is also plotted in the figure. It can be seen that the transmission probability obtained by using WKB method in full band MC simulation is accurate in wide energy region and can be used in the simulator. During MC simulation, a random number γ between 0 and 1 is selected and compared with $T_{\rm E}$. The particle will tunnel through dielectric when $T_{\rm E} \geq \gamma$. And the particle will be still transported in the channel when $T_{\rm E} < \gamma$.

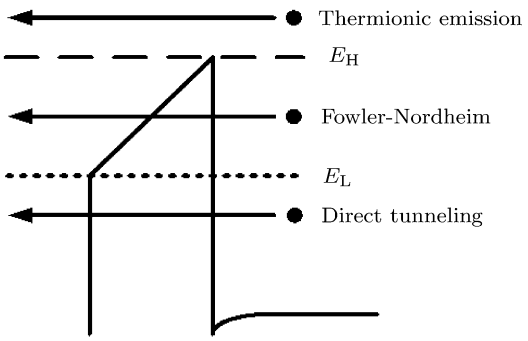


Fig.1. Schematic for the electron tunnelling through gate dielectric.

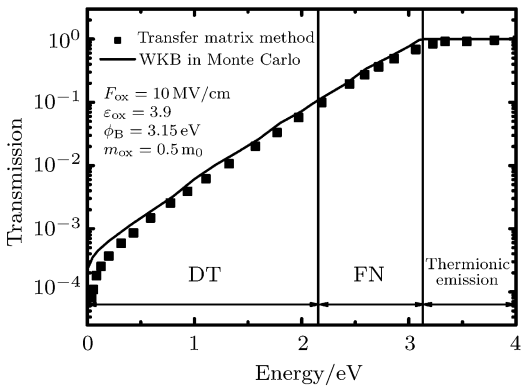


Fig.2. Comparison between the transmission probabilities for a MOS structure with 1-nm thick oxide. Parameters: $F_{\rm ox} = 10\,{\rm MV/cm}$, $\varepsilon_{\rm ox} = 3.9$, $\phi_B = 3.15\,{\rm eV}$, $m_{\rm ox} = 0.5\,m_0$.

In MC simulation, each particle has its charge weight $P_{{\rm c}_i}$. In grid i, during time step ΔT, the number of particles N_i and its charge Q_i tunnelling through gate dielectric are recorded and calculated. The tunnelling current density for each interface area can be evaluated as

$$I_{g-i}^{\rm sc\to metal} = Q_i/(\Delta T^* \Delta L_i) \qquad (1)$$

where ΔL_i is the length of the grid i. Then the gate tunnelling current can be calculated as

$$I_{g_{-\text{total}}}^{\text{sc}\to\text{metal}} = \sum_{i=0}^{n} Q_i/\Delta T \tag{2}$$

The calculation of current tunnelling through gate dielectric from metal to semiconductor ($I_{g_{-\text{total}}}^{\text{metal}\to\text{sc}}$) is the same as that in Ref.[7]. Then, the net gate tunnelling current can be evaluated as

$$I_{g_{-\text{net}}} = I_{g_{-\text{total}}}^{\text{sc}\to\text{metal}} - I_{g_{-\text{total}}}^{\text{metal}\to\text{sc}} \tag{3}$$

Figure 3 shows the simulated gate tunnelling current density versus gate voltage for a MOS structure with 1.5-nm thick oxide using full-band MC method. For comparison, the experimental data[1] and the full quantum calculation results using numerical solution of the Schrödinger equation[2] are also plotted in Fig.3. It can be seen that the difference between our simulation results and the results from full quantum simulation is very small as we use the MC method to solve QBE instead of semiclassical Boltzmann equation, and the 2D QM effect is included naturally. The difference between our results and the experimental data is also very small when gate voltage is less than 1 V. The reason that the difference between our results and the experimental data becomes larger at high gate voltages can be understood as the influence of serial resistance and the variation of channel doping concentration in the experiment.

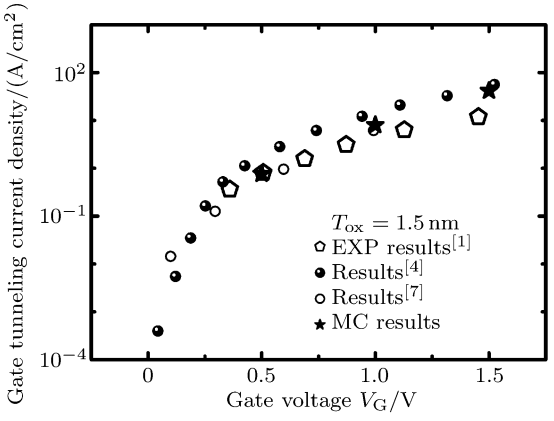


Fig.3. Simulated gate tunnelling current density by full-band MC method versus the gate voltage in a 1.5-nm thick gate oxide MOS structure. For comparison, the full quantum calculation result using numerical solution of the Schrödinger equation [2] is also plotted.

3. Results and discussions

A 40-nm gate-length Si UTB nMOSFET as shown in Fig.4 is simulated. The gate oxide is 1.2 nm thick. For simplification, we assume that uniform source and drain doping concentrations both are $1 \times 10^{20}\,\text{cm}^{-3}$, and the channel doping concentration is $1\times10^{15}\,\text{cm}^{-3}$. The silicon film thickness (T_{si}) is 10 nm, which is less than 1/3 channel length, so short channel effect (SCE) can be well suppressed. The source and drain extension distance L_{sd} is 20 nm for reducing parasitical resistance.

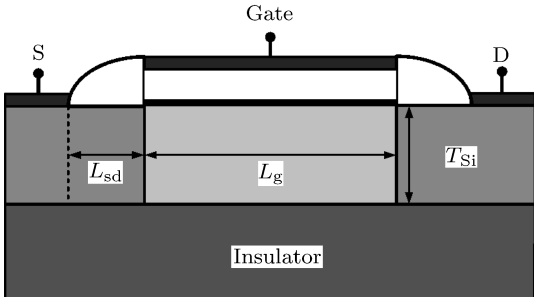


Fig.4. Schematic for a nano-scale UTB nMOSFET.

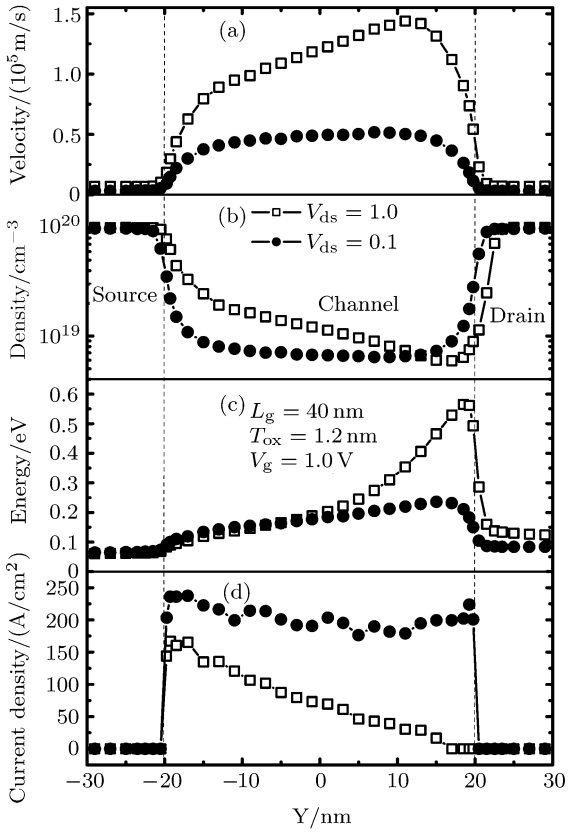


Fig.5. Electron density and energy distribution along the channel for a 40-nm gate-length nMOSFET.

Different from the MOS capacitor, in MOSFET the property of carriers' transport in the channel is affected by the factors in two directions which are along the channel and vertical to the channel. In nanoscale carrier transport in the channel of nano-scale MOSFETs the carriers can be energetic and even in non-equilibrium with the lattice. The tunnel effect is sensitive to the barrier shape and height, electron energy and the charge density. Thus it is necessary to investigate the gate current of MOSFET in 2D including the detailed band structure and non-equilibrium transport effect under different bias conditions. Figures 5(a)–(d) show the distribution of the carrier velocity, inversion charge density, electron energy and the gate current density along the channel of 40-nm nMOSFET under $V_{\rm gs} = 1\,{\rm V}$ and lower drain voltage $V_{\rm ds} = 0.1\,{\rm V}$ as well as higher drain voltage $V_{\rm ds} = 1\,{\rm V}$ respectively. From these figures, it can be seen that the gate current and its distribution are very sensitive to the drain voltage. When the drain voltage is lower, for example $V_{\rm ds} = 0.1\,{\rm V}$, the inversion layer can be formed in the whole channel and distributed almost uniformly as shown in Fig.5(b). The electric field is weaker, corresponding to a lower electron average velocity and lower electron energy. The distributions of the velocity and the energy are also almost uniform in the whole channel. But at the higher drain biases, say, $V_{\rm ds} = 1\,{\rm V}$, the inversion charge in the channel decreases while the energy increases rapidly near the drain side, and the electron average energy peak can reach 0.6 eV in the channel at the drain end as shown in Figs.5(b) and (c). The velocity overshoot can be found almost in the whole channel, in which electron average velocity exceeds the saturation velocity due to the non-equilibrium transport as shown in Fig.5(a). From Fig.5(d) it can be seen that the distribution of gate current density along the channel is also uniform under the lower drain biases, but decreases rapidly in the channel at the drain end under higher values of $V_{\rm ds}$. Hence drain voltage $V_{\rm ds}$ can influence the number and distribution of inversion charges in the channel which can tunnel through the barrier, and the energy distribution of inversion charges. Besides, at the same time $V_{\rm ds}$ can influence the barrier shape by modulating the potential distribution along the channel. Thus 2D full band simulation is necessary to simulate the gate tunnelling current. Figure 6 shows the gate tunnelling current versus drain voltage for a 40-nm gate-length and 1.2-nm thick gate oxide UTB nMOSFET. The gate tunnelling current density distributions along the channel for various drain voltages are displayed in Fig.7. Gate current decreases with the increase of $V_{\rm ds}$, which indicates that the number of inversion charges tunnelling through the barrier, instead of their energy, has a dominant influence on the gate current. The maximum gate tunnelling current is obtained for the lower drain voltages, which causes a serious problem of stand-by power consumption.

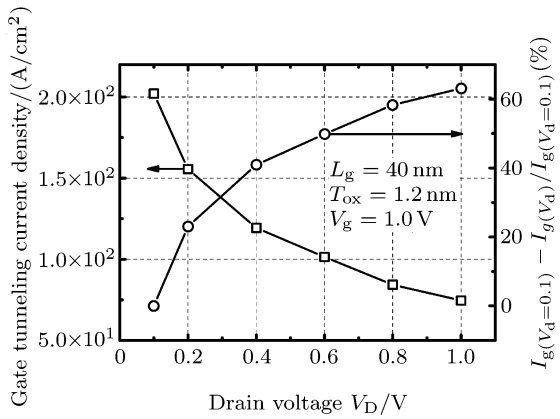


Fig.6. Gate tunnelling current for different gate-length UTB nMOSFET versus drain voltage.

On the other hand, with the increase of $V_{\rm ds}$, the energy of inversion charges increases rapidly especially near the drain side, then the electrons tunnelling through the barrier are very 'hot'. These hot electrons transporting across the gate dielectric will influence the reliability of MOSFET even though the number of the hot electrons is small. Thus 2D full band simulation is important to investigating the properties of nano scale MOSFETs.

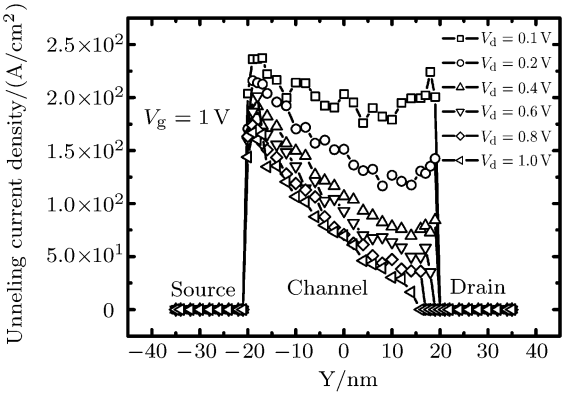


Fig.7. Gate tunnelling current density distribution along the channel under different drain voltages.

4. Conclusion

The gate tunnelling current in nano-scale UTB nMOSFETs is investigated by 2D full-band MC simulation based on solving QBE. The gate tunnelling current distribution along the channel is also demonstrated. The influence of drain voltage on gate tunnelling current is studied. Results show that the drain voltage has a significant effect on gate tunnelling current. The maximum gate tunnelling current is obtained for the lower drain voltages, which causes a serious problem of stand-by power consumption. Under the high values of $V_{\rm ds}$, the hot electrons' transport across the gate dielectric will influence the reliability of MOSFET.

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