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Electrical properties and reliability of HfO_2 gate-dielectric MOS capacitors with trichloroethylene surface pretreatment*

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Trichloroethylene (TCE) pretreatment of Si surface prior to HfO_2 deposition is employed to fabricate HfO_2 gate-dielectric MOS capacitors. Influence of this processing procedure on interlayer growth, HfO_2/Si interface properties, gate-oxide leakage and device reliability is investigated. Among the surface pretreatments in NH_3, NO, N_2O and TCE ambients, the TCE pretreatment gives the least interlayer growth, the lowest interface-state density, the smallest gate leakage and the highest reliability. All these improvements should be ascribed to the passivation effects of Cl_2 and HCl on the structural defects in the interlayer and at the interface, and also their gettering effects on the ion contamination in the gate dielectric.

Keywords: MOS capacitors, high-k gate dielectric, HfO_2, interlayer, surface treatment
PACC: 7300, 7340Q

1. Introduction

With aggressive scaling of CMOS devices, sub-2-nm gate dielectrics are needed for sub-100-nm MOSFET. Such an ultra-thin gate oxide results in significant gate leakage (direct tunnelling current) and poor reliability. As an alternative, high-dielectric-constant (high-k) gate dielectrics have been widely studied.[1−7] Among them, HfO_2 is currently considered as the most promising candidate due to its high dielectric constant (∼25), relatively large bandgap (5.68 eV) and compatibility with conventional CMOS processes because of its thermo dynamic stability on Si.[8−9] However, an interlayer (IL) of SiO_2 is usually formed as a low-dielectric-constant layer by the thermal oxidation of the Si substrate during the deposition of HfO_2 and subsequent high-temperature processing, thus increasing the equivalent oxide thickness (EOT) and degrading the performance of the device. To fabricate high-quality gate dielectrics with the interlayer formation well suppressed, some processes were proposed, including NH_3 surface nitridation,[10] and thin Hf predeposition.[11−12]

In this study, a novel process is proposed to fabricate HfO_2 gate dielectric with a TCE pretreatment before HfO_2 deposition. As a result, not only the IL growth is effectively suppressed, but also the oxide charges and interface states are reduced, due to the passivation and gettering effects of Cl_2 and HCl resulting from the decomposition of TCE. For comparison, various surface nitridation processes in NH_3, NO and N_2O ambients are also employed to prepare HfO_2 gate-dielectric MOS capacitors. While the NO-pretreated device exhibits good interface properties and reliability as compared with the other two nitrided devices, the TCE-pretreated device presents the least interlayer growth, the lowest interface-state density, the smallest gate leakage and the highest reliability among these devices.

2. Experiment

MOS capacitors were fabricated on (100)-oriented n-type Si substrates with a doping concentration of

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$5 \times 10^{15}\,\mathrm{cm}^{-3}$. The wafers were cleaned using the standard RCA method followed by a 1-min dip in 5% HF to remove the native oxide. Before deposition of HfO_2, different surface pretreatments were performed at 800 °C for 4 min in NH_3, NO, N_2O and TCE ambients, denoted as NH_3, NO, N_2O and TCE samples respectively. TCE was carried by bubbling dry O_2 gas (50 ml/min) through a TCE solution at room temperature. HfO_2 was subsequently deposited by reactive RF sputtering in 20% O_2 + 80% Ar ambient at room temperature, about 0.4 Pa of pressure and 100 W of power. All samples were then annealed at 800 °C for 5 min in N_2. Finally, Al was thermally evaporated and patterned as the gate electrode of the MOS capacitor with an area of $7.85 \times 10^{-5}\,\mathrm{cm}^2$. In order to clearly distinguish the interlayer thickness among the samples and thus determine optimal pretreatment technology, a thicker HfO_2 film with a thickness of 10 nm, measured by ellipsometry, higher pretreatment/anneal temperature of 800 °C and longer pretreatment/anneal time of 4 min/5 min was used.

High-frequency (1 MHz) capacitance–voltage (C–V) characteristics were measured at room temperature using HP4284A precision LCR meter. Oxide capacitance (hence oxide thickness), flat-band voltage, and oxide-charge density were extracted from the high-frequency C-V curve. The interface-state density at midgap was extracted from the high-frequency C–V curve using the Terman method.[13] A high-field stress (10 MV/cm), with the capacitors biased in accumulation by HP 4156 A precision semiconductor parameter analyser, was used to examine device reliability in terms of gate-leakage increase and flat-band-voltage shift. All measurements were carried out under a light-tight and electrically-shielded condition.

3. Results and discussion

Figure 1 shows the typical high-frequency C–V curves of all the samples under dark condition. The values of electrical thickness (t_{ox}) of the gate oxide and flat-band voltage (V_{fb}) extracted from the high-frequency C–V curves are listed in Table 1. The equivalent oxide-charge density (Q_{ox}) is calculated as $-C_{ox}(V_{fb} - \varphi_{ms})/q$, where the work-function difference φ_{ms} between Al and Si is calculated to be −0.0027 V. Obviously, different accumulation capacitances (C_{ox}), thus different oxide thicknesses are observed for the samples under different surface pretreatments. The N_2O sample has the minimum C_{ox}, indicating that the thickest interfacial layer (5.4 nm) was grown because of enhanced oxidation during N_2O pretreatment[14] and poor resistance (due to little nitrogen incorporation in the grown SiO_2) against further oxidation during HfO_2 deposition and anneal. For the NO sample, the IL thickness (4.3 nm) is smaller than that of the N_2O sample due to the self-limiting nature of NO oxidation and better nitridation effect using NO gas (more nitrogen incorporation).[15] More significantly, the IL is effectively suppressed for the TCE- and NH_3-pretreated samples (2.7 nm and 3.1 nm in thickness respectively), especially for the TCE sample. The NH_3 treatment leads to the formation of a thin nitrogen-terminated passivation layer, thus effectively preventing the growth of a SiO_2-like interfacial layer during HfO_2 deposition and anneal. On the other hand, the TCE treatment could give a Cl-terminated surface, which, like a nitrided surface, probably plays a role in retarding further oxidation during HfO_2 deposition and anneal. It should be noted that based on the smallest t_{ox} of the TCE sample, the growth of interfacial oxide during the TCE pretreatment is negligible, which is possibly due to the use of very low O_2 flow rate (50 ml/min), and also the formation of CO_2 and CO through the reaction of O_2 with C decomposed from TCE. Furthermore, another advantage of the TCE treatment lies in low oxide-charge and interface-state densities as shown in Table 1. This is ascribed to the passivation effect in which Cl_2 or HCl from TCE decomposition can combine with dangling Si and non-bridging O to reduce interface states, and also to the fact that Cl_2 and HCl can getter the ion contamination from the out-diffusions of the substrate dopant and the gate dielectric, thereby leading to reduction of the oxide charges.[16]

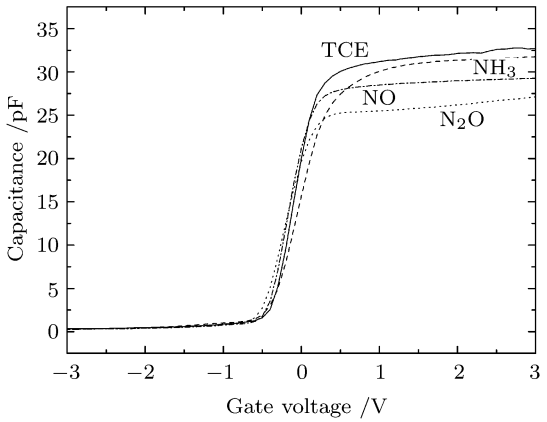


Fig.1. Typical high-frequency C–V curves of the samples under dark condition at room temperature, with capacitor area of $7.85 \times 10^{-5}\,\mathrm{cm}^2$.

Table 1. Oxide capacitance and thickness, oxide-charge and interface-state densities, and flatband voltage of the samples extracted from high-frequency C–V curve. The flatband-voltage shift of the samples is due to a high-field stress of 10 MV/cm for 1000 s.

Sample	C_{ox}/pF	t_{ox}/nm	$Q_{ox}/10^{11}cm^{-2}$	D_{it} at midgap/$10^{11}cm^{-2}\cdot eV^{-1}$	V_{fb}/V	ΔV_{fb}/V
NH_3	31.7	13.1	3.71	9.08	−0.15	−0.45
NO	29.2	14.3	5.74	3.97	−0.25	−0.09
N_2O	27.1	15.4	5.98	5.93	−0.28	−0.28
TCE	32.7	12.7	4.87	3.76	−0.19	−0.04

It is worth pointing out that the small values of V_{fb} and Q_{ox} of the NH_3 sample (see Table 1) probably arise from a compensation effect between the negative charges of electron traps related to hydrogen[17] and the positive fixed charges associated with N incorporation.[17] The existence of a large number of electron traps induced by nitridation (due to the formation of NH_3) is supported by a large gate leakage current in the accumulation region as shown in Fig.2. For the TCE sample, despite its smallest t_{ox}, low oxide-charge and interface-state densities could be responsible for its lowest gate leakage current among the samples.

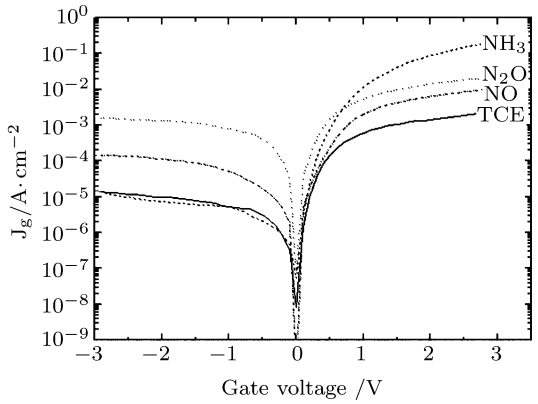


Fig.2. Gate leakage of the samples.

Figure 3 shows the gate leakage features of the samples before and after suffering a high-field stress of 10 MV for 1000 s. Clearly, the gate leakage currents of the NO and N_2O samples hardly increase, while the NH_3 sample shows the largest increase in gate leakage current after being stressed. This indicates that the hard IL and IL/Si interface with strong Si–N bonds (E_{Si-N} = 4.6 eV) are formed by NO or N_2O surface nitride, while weak –H and -OH bonds produced by NH_3 surface nitride in the IL and at the interface are easily broken under the high-field stress, thus inducing a large increase in gate leakage current. For the TCE sample, a small increase in gate leakage current is observed in Fig.3, implying the less generation of interface and near-interface traps. This is probably related to the formation of strong Si–Cl bonds (E_{Si-Cl} = 4.16 eV) by the passivation effect of Cl_2 and HCl in the IL and at the interface. The stress-induced shift of flat-band voltage (ΔV_{fb}) as listed in Table 1 is basically consistent with the increase of gate leakage current, and with the minimum shift for the NO and TCE samples, which further supports the above analysis.

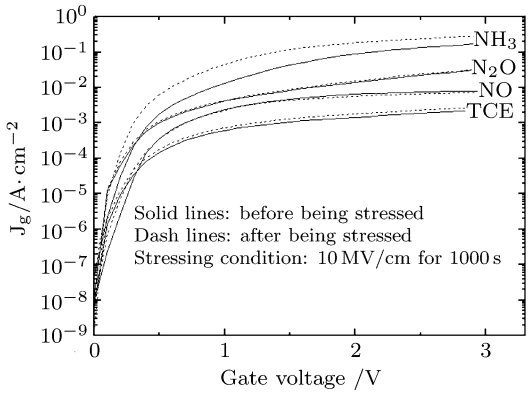


Fig.3. Gate-leakage increase of the samples after suffering a high-field stress of 10 MV/cm for 1000 s.

From the above results and discussion, it could be expected that a thin IL would be obtained if both pretreatment and anneal temperature/time are properly lowered/shortened, and a thin HfO_2 film (e.g. 4–5 nm) is deposited. Further studies are underway.

4. Summary

A new TCE pretreatment of Si surface before HfO_2 deposition is proposed to fabricate high-k gate dielectric. Among the samples with surfaces pretreated in NH_3, NO, N_2O and TCE ambients, the TCE-pretreated sample exhibits the least IL growth, the lowest interface-state density, and the smallest

gate leakage. The mechanisms involved probably are the passivation effects of Cl_2 and HCl on the structural defects in the IL and at the interface, and their gettering effects on ion contamination. Furthermore, the TCE pretreatment results in better device reliability due to the formation of strong Si–Cl bonds at/near the interface, like the nitridation-induced formation of strong Si–N and N–O bonds. Therefore, the TCE pretreatment prior to HfO_2 deposition has high potential of suppressing the growth of an IL with a low dielectric constant, decreasing the gate leakage current, improving the HfO_2/Si interface properties and enhancing the device reliability.

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