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Effect of interface-roughness scattering on mobility degradation in SiGe p-MOSFETs with a high-k dielectric/SiO_2 gate stack*

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A physical model for mobility degradation by interface-roughness scattering and Coulomb scattering is proposed for SiGe p-MOSFET with a high-k dielectric/SiO_2 gate stack. Impacts of the two kinds of scatterings on mobility degradation are investigated. Effects of interlayer (SiO_2) thickness and permittivities of the high-k dielectric and interlayer on carrier mobility are also discussed. It is shown that a smooth interface between high-k dielectric and interlayer, as well as moderate permittivities of high-k dielectrics, is highly desired to improve carriers mobility while keeping a low equivalent oxide thickness. Simulated results agree reasonably with experimental data.

Keywords: MOSFET, high-k dielectric, SiGe, interface roughness scattering, Coulomb scattering
PACC: 7340Q, 7220F

1. Introduction

High permittivity (high-k) gate dielectrics are promising materials for their capability to reduce gate-leakage current of metal–oxide–semiconductor field effect transistor (MOSFET) with a small equivalent oxide thickness (EOT). Among the issues raised by the integration of high-k materials, degradation of the carrier mobility has been observed in the devices, whatever is the kind of high-k dielectric.[1] It has been suggested that the mobility loss is caused by several physical mechanisms,[2] such as remote Coulomb scattering from poly-Si gate, remote surface-roughness scattering and remote soft-optical phonon scattering. Besides these scattering mechanisms, there are some other scattering mechanisms which also can reduce the mobility of carriers in the channel.

While depositing high-k dielectrics on Si, SiGe or Ge substrate, a thin interlayer such as SiO_2, GeON, is often formed.[3−5] The interlayer is intentionally inserted as a passivation layer to improve the quality of the interface between high-k gate dielectric and channel (especially for SiGe or Ge channel),[6−8] or unintentionally formed during high-k dielectric deposition and annealing process. The interface between high-k gate dielectric and interlayer is usually not smooth, leading to the following two effects: 1) fluctuation of the interface will induce an effective dipole moment due to permittivity difference between the high-k dielectric and interlayer, generating a perturbation potential on the carriers in the channel; 2) fluctuation of the interface will cause a change of local capacitance, inducing extra charges both in the gate and channel which thus exert additional scattering on carriers inside the channel, as shown in Fig.1. At the same time, the fixed charges near/at the high-k dielectric/SiO_2 interface can also reduce carrier mobility.[1,9,10] To our knowledge, although the remote Coulomb scattering at the high-k dielectric/SiO_2 interface has been discussed,[2,9,10] the roughness scattering resulting from the fluctuation of the high-k dielectric/SiO_2 interface has not been addressed. In this work, we present a theoretical model describing

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how the carriers get scattered by the fixed charged defects near the high-k dielectric/SiO_2 interface, as well as the interface roughness or interface-fluctuation. Only three experience parameters such as rms Δ_m, correlation length Λ and the density of fixed charged defects N_{it} are needed in the model. Using the Fang-Howard's variational wave function, the hole mobility is calculated by taking the above scattering mechanisms into account.

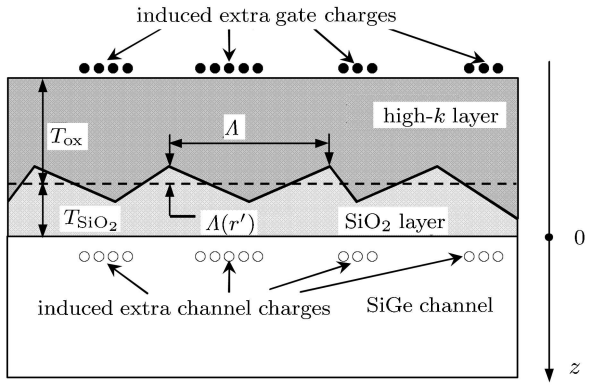


Fig.1. Schematic model for the roughness of the high-k dielectric/SiO_2 interface. The dashed line represents the average interface between the high-k dielectric and SiO_2.

2. Model

2.1. Remote interface-roughness scattering (RIRS)

A high-k dielectric/SiO_2 stacked gate system is schematically shown in Fig.1. Fluctuation of the interface induces an effective dipole moment, and disturbs the potential in the channel. In the presence of a thickness deviation $\Delta(r')$ from its average value T_{ox} for the high-k dielectric, an effective dipole moment p_z is generated:

$$p_z(\boldsymbol{r}') = (\varepsilon_{ox} - \varepsilon_{SiO_2}) E_z \Delta(r') \mathrm{d}r', \tag{1}$$

where ε_{ox} and ε_{SiO_2} are permittivities of the high-k dielectric and SiO_2 respectively; and E_z is the vertical field in the high-k dielectric. From the Ando's model,[11] this effective dipole moment gives a perturbation potential at any point $(\boldsymbol{r}, z)$ in the SiGe channel:

$$\delta V^{(1)} = \frac{1}{4\pi\varepsilon_{SiO_2}} \Big(1 - \frac{\varepsilon_{SiO_2} - \varepsilon_{ox}}{\varepsilon_{SiO_2} + \varepsilon_{ox}}\Big) \times p_z(\boldsymbol{r}') z[(\boldsymbol{r} - \boldsymbol{r}')^2 + (z + T_{SiO_2})^2], \tag{2}$$

with relevant perturbation matrix element

$$M^{(1)}(q) = \frac{e^2(\varepsilon_{SiO_2} - \varepsilon_{ox})}{\varepsilon_{SiO_2}(\varepsilon_{SiO_2} + \varepsilon_{ox})\varepsilon(q)} \times (N_s + N_{depl}) \Delta_q P_0 \mathrm{e}^{-qT_{SiO_2}}. \tag{3}$$

where N_{depl} and N_s are respectively the depletion-charge and inversion-charge areal density in the channel, which are obtained by self-consistently solving the Schrödinger-Poisson equations; Δ_q is the Fourier transform of $\Delta(r')$. A Gaussian power spectrum for Δ_q is assumed to characterize the roughness of the interface as usually done.[11−13] In Eq.(3), the wave-vector-dependent dielectric function $\varepsilon(q)$ is used to account for the screening effect. The function $\varepsilon(q)$ can be expressed as

$$\varepsilon(q) = 1 + \frac{q_s(q)}{q}(P_{av} + \chi_2 \boldsymbol{P}_0^2), \tag{4}$$

in which parameters P_0 and P_{av} are defined as:

$$P_0 = \int_0^\infty \mathrm{d}z |\xi_0(z)|^2 \mathrm{e}^{-qz} = \Big(\frac{b}{b+q}\Big)^3,$$
$$P_{av} = \iint \mathrm{d}z \mathrm{d}z' |\xi_0(z)|^2 |\xi_0(z')|^2 \mathrm{e}^{-q|z-z'|} = \frac{8b^3 + 9b^2 q + 3bq^2}{8(b+q)^3}. \tag{5}$$

Here, b is a variational parameter:

$$b = [12e^2 m_l \Big(N_{depl} + \frac{11}{32} N_s\Big) \Big/ (\varepsilon_{sc}\hbar^2)]^{1/3};$$

m_l is the longitudinal effective mass of holes, in Eq.(4) χ_2 is a permittivity-related parameter which is presented in the following section; and $q_s(q)$ is a wave-vector-dependent screening parameter:[13]

$$q_s(q) = \frac{e^2 m_d}{4\pi\varepsilon_{sc}\hbar^2} \int_0^1 \frac{f(bx - E_f/k_B T)}{\sqrt{1-x}} \mathrm{d}x, \tag{6}$$

where E_f is Fermi level; k_B the Boltzmann's constant, T absolute temperature, m_d the density-of-state effective mass for holes, and f the Fermi–Dirac distribution function.

The deviation $\Delta(\boldsymbol{r}')$ can also lead to a change of local capacitance,

$$\delta C_{ox}^{eff} = -C_{ox}^{eff}(\varepsilon_{ox} - \varepsilon_{SiO_2}) \frac{\Delta(r')}{t_{ox}^{eff}}, \tag{7}$$

where C_{ox}^{eff} is the effective oxide capacitance, and t_{ox}^{eff} the effective oxide thickness:

$$C_{ox}^{eff} = \Big(\frac{T_{ox}}{\varepsilon_{ox}} + \frac{T_{SiO_2}}{\varepsilon_{SiO_2}}\Big)^{-1},$$
$$t_{ox}^{eff} = \varepsilon_{ox} T_{SiO_2} + \varepsilon_{SiO_2} T_{ox}. \tag{8}$$

T_{SiO_2} and $T_{ox}$are thicknesses of SiO_2 and high-k dielectric layers respectively (see Fig.1). This small change of capacitance δC_{ox}^{eff} induces extra charges δQ_gin gate electrode and δQ_s in the channel

$$\delta Q_g = -Q_g(\varepsilon_{ox} - \varepsilon_{SiO_2})\frac{\Delta(\boldsymbol{r}')}{t_{ox}^{eff}}dr', \quad (9)$$

$$\delta Q_s = -\delta Q_g, \quad (10)$$

where Q_g is the total gate sheet-charge density. The perturbation electrostatic potential caused by these extra charges can be obtained by solving the Poisson's equation

$$\nabla \cdot [\varepsilon(z)\nabla V(\boldsymbol{r}, z)] = -(\rho_0 + \rho_{ind}), \quad (11)$$

where ρ_0 and ρ_{ind} are extra charge density and induced screening-charge density respectively. In gate electrode, ρ_0 and ρ_{ind} can be expressed as

$$\rho_0(r', z) = \delta Q_g \delta(\boldsymbol{r} - \boldsymbol{r}')\delta(z - z_0), \quad (12)$$

$$\rho_{ind} = -2\varepsilon_{sc} q_s(q)\langle V(\boldsymbol{r}, z_0)\rangle |\xi_0(z)|^2, \quad (13)$$

in which $z_0 = -(T_{SiO_2} + T_{ox})$, $\delta(\boldsymbol{r} - \boldsymbol{r}')$ is the Dirac's delta function and $\langle V(\boldsymbol{r}, z_0)\rangle$ is the perturbation potential averaged over the inversion-charge distribution in the z direction. By performing a two-dimensional Fourier transform, Eq.(11) can be expressed as

$$\Big(\frac{\partial}{\partial z}\varepsilon(z)\frac{\partial}{\partial z} - \varepsilon(z)q^2\Big)V(q, z; z_0) = -\frac{\delta Q_g}{\varepsilon(z_0)}\delta(z - z_0) + 2\varepsilon_{sc} q_s(q)\langle V(q, z_0)\rangle |\xi(z)|^2, \quad (14)$$

where $V(q, z)$ is a Fourier transform component of the perturbation potential $V(r, z)$. Equation (14) can be solved by the Green's function method,[14]

$$V(q, z; z_0) = \frac{\delta Q_g \chi_1}{2\varepsilon(z_0)q}e^{q(z - z_0)} - \frac{q_s(q)\langle V(q, z_0)\rangle}{q} \times \int_0^\infty [e^{-q|z' - z|} + \chi_2 e^{-q(z' + z)}]|\xi_0(z')|^2 dz', \quad (15)$$

with parameters

$$\beta_1 = \frac{\varepsilon_{sc} - \varepsilon_{SiO_2}}{\varepsilon_{sc} + \varepsilon_{SiO_2}}, \quad \beta_2 = \frac{\varepsilon_{ox} - \varepsilon_{SiO_2}}{\varepsilon_{ox} + \varepsilon_{SiO_2}}; \quad (16)$$

and

$$\chi_1 = \frac{(1 - \beta_1)(1 + \beta_2)}{1 - \beta_1\beta_2 e^{-2qT_{SiO_2}}},$$

$$\chi_2 = \frac{\beta_1 - \beta_2 e^{-2qT_{SiO_2}}}{1 - \beta_1\beta_2 e^{-2qT_{SiO_2}}}. \quad (17)$$

From Eq.(15), the scattering matrix element is obtained

$$M^{(2)}(q) = -\frac{e\delta Q_g \chi_1}{2\varepsilon_{ox}} \times P_0 \frac{e^{-q(T_{SiO_2} + T_{ox})}}{q + q_s(q)(P_{av} + \chi_2 P_0^2)}. \quad (18)$$

The perturbation electrostatic potential caused by δQ_s can be obtained with the same procedure as the above. But it should be noted that δQ_s distributes in the channel with a finite depth unlike the sheet charges δQ_g. Under the strong inversion condition, the change of Q_s is dominated by Q_{inv}, and therefore $\delta Q_s \sim \delta Q_{inv}$. So we use $\delta Q_s(z) = \delta Q_{inv}(z) = \delta Q_g|\xi_0(z)|^2$ to model the finite depth distribution of δQ_s, and obtain

$$\rho_0(\boldsymbol{r}, z) = \delta Q_g \delta(\mathbf{r} - \boldsymbol{r}')|\xi_0(z)|^2. \quad (19)$$

Finally, the scattering matrix element is deduced as

$$M^{(3)}(q) = \frac{P_{av} + \chi_2 P_0}{2\varepsilon_{sc}[q + q_s(q)(P_{av} + \chi_2 P_0^2)]}e\delta Q_g. \quad (20)$$

From Eqs.(3), (18) and (20), the remote interface-roughness scattering (RIRS) matrix element is given by

$$M^{(RIRS)}(q) = M^{(1)} + M^{(2)} + M^{(3)}. \quad (21)$$

2.2. Remote Coulomb Scattering (RCS)

Near the high-k dielectric/SiO_2 interface, there exist a lot of fixed charges.[1,9,10] These charges can scatter those carriers in the SiGe channel, i.e. remote Coulomb scattering. Assuming that Ze is a fixed charge located at z_0 in the high-k gate dielectrics near the high-k dielectric/SiO_2 interface, we see that the perturbation electrostatic potential caused by this fixed charge can be obtained by solving the Poisson's equation as we have done in subsection 2.1. The scattering matrix element is given by

$$M^{(RCS)}(q) = \langle k|e\delta V_{RCS}|k'\rangle = \frac{Ze\chi_1}{2\varepsilon_{ox}}P_0\frac{e^{qz_0}}{q + q_s(q)(P_{av} + \chi_2 P_0^2)}. \quad (22)$$

According to Refs.[1], [15] and [16], we can assume that the fixed charges are located at the high-k dielectric /SiO_2 interface with areal density N_f. So the scattering matrix element can be expressed as

$$M^{(RCS)}(q) = \frac{N_f Ze\chi_1}{2\varepsilon_{ox}}P_0\frac{e^{-qT_{SiO_2}}}{q + q_s(q)(P_{av} + \chi_2 P_0^2)}. \quad (23)$$

From Refs.[1], [9] and [10], N_f ranges from 10^{12} to 7×10^{13} cm^{-2}. In following calculations, a value of 6×10^{13} cm^{-2} is used to best fit the experimental data.

Once the perturbation matrix element is obtained, the relaxation time $\tau_i(E)$ can be calculated using

$$\frac{1}{\tau_i(E)} = \frac{m_{\rm d}}{\pi\hbar^3}\int_0^{\pi} |M^{(i)}(q)|^2(1-\cos\theta){\rm d}\theta, \qquad (24)$$

where i represents remote interface-roughness scattering or remote Coulomb scattering. Finally, carrier mobility is calculated by the relaxation-time approximation[11]

$$\mu_i = \frac{e\langle\tau_i\rangle}{m_{\rm c}}, \qquad (25)$$

$m_{\rm c}$ is the effective transverse mass of holes in the channel and $\langle\tau_i\rangle$ is the averaged relaxation time over kinetic energy E, i.e.

$$\langle\tau_i\rangle = \frac{\int_{E_0}^{\infty} E\tau_i(E)(-\partial f/\partial E){\rm d}E}{k_{\rm B}T\ln[1+{\rm e}^{(E_{\rm f}-E_0)/k_{\rm B}T}]}, \qquad (26)$$

where E_0 denotes the ground level of the first subband. In order to investigate the impact of IRSR and RCS on the hole mobility, the 'universal curve'[17] of holes in SiGe p-MOSFETs is taken as a reference. The effective mobility $\mu_{\rm eff}$ is calculated by the Matthiessen's rule

$$\mu_{\rm eff}^{-1} = \mu_{\rm RIRS}^{-1} + \mu_{\rm RCS}^{-1} + \mu_{\rm universal}^{-1}. \qquad (27)$$

3. Results and discussion

Figure 2 shows the RIRS-limited mobility as a function of effective field with a variable parameter $\Delta_{\rm m}$ for a strained $Si_{1-x}Ge_x$ ($x = 0.28$, and channel doping $N_{\rm a} = 4\times10^{17}$ cm^{-3}) p-MOSFET with a high-k/SiO_2 stacked gate. The strain-related parameters, such as hole effective mass, density-of-states effective mass, permittivity and so on, are calculated according to Ref.[18] and listed in Table 1. As expected, the increase of $\Delta_{\rm m}$ leads to severe reduction of $\mu_{\rm RIRS}$. The RIRS-limited mobility behaves similarly to the surface roughness-limited (SR-limited) mobility resulting from gate-oxide/substrate interface, which decreases with the increase of effective field. However, a little kink exists in the curve of the RIRS-limited mobility. This is because one of the sources of the perturbation potential is the extra charges distributed in both gate and channel. As the gate voltage is raised above the threshold, the increase of the screening effect exceeds the increase of the scattering potential and thus $\mu_{\rm RIRS}$ rises. While at higher effective fields, the increase of the scattering potential becomes dominant and $\mu_{\rm RIRS}$ will decrease with effective field. Figure 3 shows the dependence of $\mu_{\rm RIRS}$ on Λ at an effective field $E_{\rm eff} = 1$ MV/cm. As Λ approaches 0 or ∞, $\mu_{\rm RIRS}$ goes to ∞, corresponding to the case that the interface of high-k dielectric/SiO_2 is smooth and thus no RTRS occurs. From Fig.3, it is found that $\mu_{\rm RIRS}$ has a minimum at $\Lambda \sim 3$ nm. Similar phenomena have been also found for SR-limited mobility and RSR-limited mobility.[12,13,19] The involved mechanism lies in that inversion carriers are most severely affected by the structure whose size is comparable to the inverse of the thermal de Broglie wave number ($k_{\rm th}^{-1} \sim 2.73$ nm). Therefore, the processing condition of gate dielectrics should be optimized to avoid $\Lambda \sim 2.73$ nm and reduce the thickness deviation Δ of gate dielectric for obtaining high hole mobility.

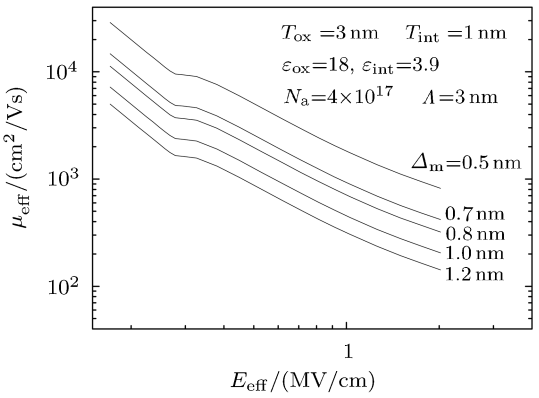


Fig.2. Dependence of RIRS-limited mobility on rms $\Delta_{\rm m}$.

Table 1. Parameters used in the model of $Si_{1-x}Ge_x$ p-MOSFET.

x	$m_{\rm d}/m_0$	$m_{\rm c}/m_0$	$m_{\rm l}/m_0$	$\varepsilon_{\rm sc}/\varepsilon_0$
0.28	0.63023	0.39698	0.39698	12.719

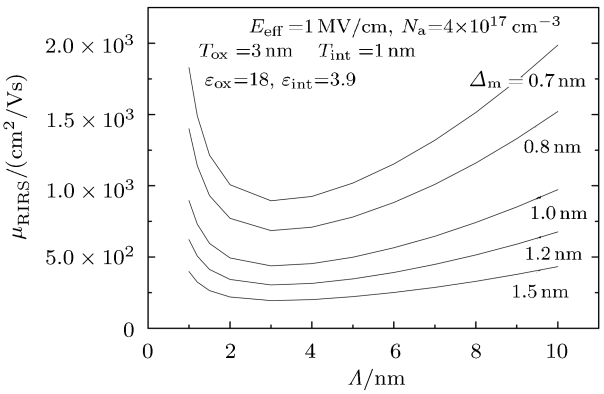


Fig.3. Dependence of RIRS-limited mobility on correlation length Λ.

Figure 4 is the simulated effective holes mobility for strained $Si_{0.72}Ge_{0.28}$ p-MOSFETs with HfO_2/SiO_2

stacked gate by taking into account RIRS and RCS and setting the thicknesses of SiO_2 interlayer to be 1 nm and 0.5 nm respectively. In simulation, $\varepsilon_{ox} = 18$ is used to represent the dielectric constant of HfO_2 in accordance with the experimental data[20] and Δ_m of ~ 0.8 nm and Λ of ~ 3 nm are selected to fit the experimental data. To examine this model, we compare the simulated results with the experimental data in Ref.[20], where it was stated that even for the thickest Si cap (i.e. 1 nm, SiGe), holes are mainly distributed in the strained-SiGe layer and there is no Si cap parasitic channel. So, it was believed that the Si cap layer was fully transferred into SiO_2 during subsequent processing, and thus SiO_2 thicknesses of 0.5 nm and 1 nm were used in the calculation. Considering the single subband approximation and ignoring the interband scattering in the model, the simulated results show reasonable agreement with experimental data,[20] indicating the correctness of the proposed model. As can be seen, the hole mobility is decreased as the thickness of the SiO_2 interlayer reduces, revealing the existence of the remote-scattering mechanisms for such a stacked gate-oxide structure.

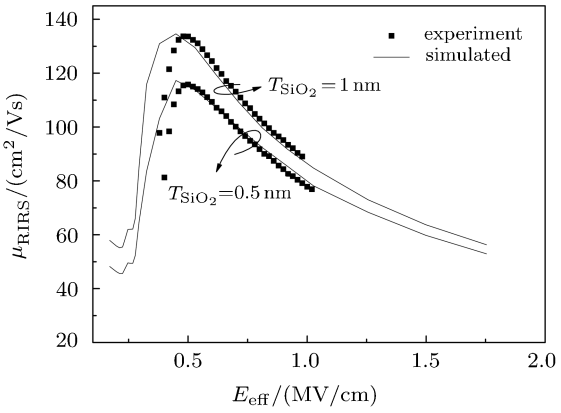


Fig.4. Simulated and experimental effective hole mobilities of SiGe MOSFET with HfO_2 gate dielectric for two thicknesses of SiO_2 cap layer, with an equivalent oxide thickness (EOT) of 1.65 nm.

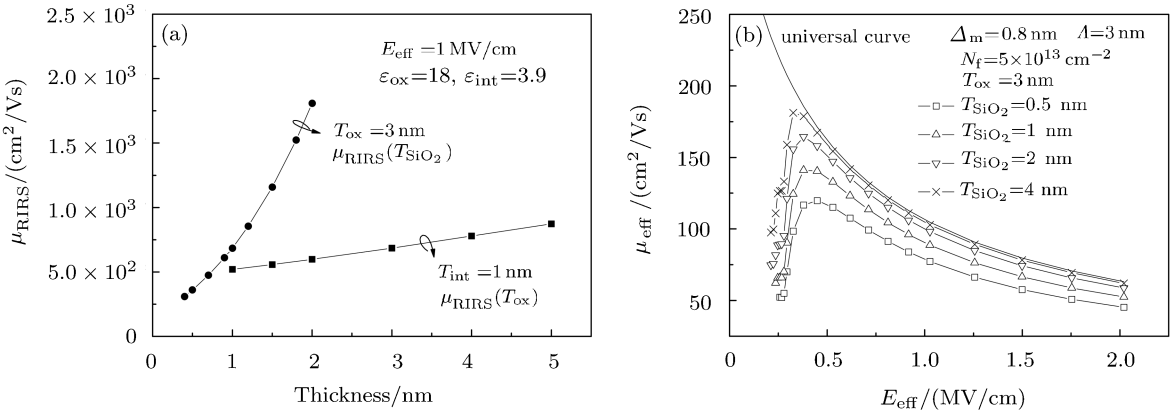


Fig.5. (a) RIRS-limited mobility versus dielectric thickness (T_{ox} or T_{SiO_2}) at $E_{eff} = 1$ MV/cm and (b) effective mobility versus effective field for different T_{SiO_2}.

Dependence of μ_{RIRS} on T_{ox} and T_{SiO_2} and impact of RIRS on degradation of effective mobility are shown in Figs.5(a) and 5(b) respectively. Calculated results show that a higher RIRS-limited mobility corresponds to the thicker high-k dielectric and SiO_2 interlayer. However, μ_{RIRS} is more sensitive to T_{SiO_2} than to T_{ox}. This can be explained as follows. On the one hand, the scattering matrix element is decreased with the increase of T_{ox} and T_{SiO_2} since $M^{(1)}$, $M^{(2)}$ and $M^{(RCS)}$ are proportional to $e^{-qT_{ox}}$, $e^{-q(T_{ox}+T_{SiO_2})}$ and $e^{-qT_{SiO_2}}$, respectively; and thus μ_{RIRS} is increased with T_{ox} and T_{SiO_2}. On the other hand, the extra induced charges $|\delta Q_g|$ or $|\delta Q_s|$ is proportional to $(\varepsilon_{ox}T_{SiO_2} + \varepsilon_{SiO_2}T_{ox})^{-1}$, where $\varepsilon_{ox} > \varepsilon_{SiO_2}$, and thus reducing of T_{SiO_2} can lead to a larger $|\delta Q_g|$ (and $|\delta Q_s|$) than reducing of T_{ox}. As a result, small T_{SiO_2} will lead to a severe degradation of effective mobility, as can be seen more clearly in Fig.5(b). So, a compromise should be tuned between small EOT and high carrier mobility.

Figure 6 shows the dependence of RIRS-limited mobility and RCS-limited mobility on the permittivity of high-k and interfacial layer. The calculated results show that increasing permittivity of high-k dielectric ε_{ox} can improve the Coulomb-scattered mobility but deteriorate the interface roughness-scattered mobility. However, the opposite case occurs when increasing permittivity (ε_{int}) of the interfacial layer.

The possible reasons are two-fold: 1) as can be seen from Eqs.(1) and (7), the dipole moment and local capacitance variations increase with increasing difference between $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm int}$ (normally $\varepsilon_{\rm ox} > \varepsilon_{\rm int}$), giving rise to a larger perturbation potential related to the interface-roughness scattering, and thus causing a strong interface-roughness scattering when the high-k dielectric constant is increased and the dielectric constant of interlayer is fixed. For a special case of $\varepsilon_{\rm ox} = \varepsilon_{\rm int}$, the perturbation matrix element $M^{(\rm RIRS)}$ vanishes, since it simply corresponds to a homogeneous gate dielectric and no interface-roughness scattering exists.; 2) the image-charge-modified terms of $\chi_1/\varepsilon_{\rm ox}$ and χ_2 in Eq.(23) decrease with increasing sum of the two dielectric constants $(\varepsilon_{\rm ox} + \varepsilon_{\rm int})$, leading to a reduction of fixed-charge perturbation potential and thus the reduction of Coulomb scattering.

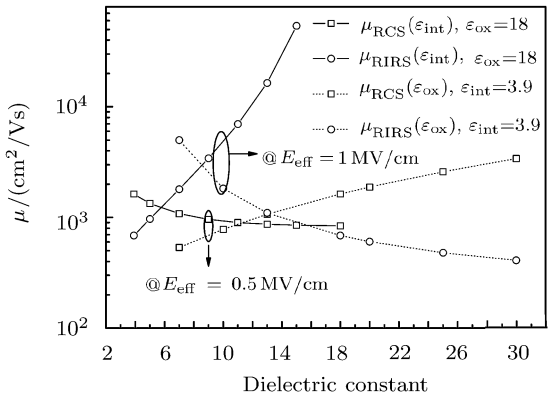


Fig.6. Calculated RIRS-limited hole mobility and RCS-limited hole mobility versus the dielectric constant of the interlayer ($\varepsilon_{\rm int}$) or high-k layer ($\varepsilon_{\rm ox}$).

Figure 7 shows the effective mobility degradation by taking into account both RCS and RIRS for different $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm int}$. In the calculation, equivalent oxide thickness (EOT) of ∼1.5 nm and $T_{\rm SiO_2}$ of 0.7 nm are used. As can be seen, the larger dielectric constant $\varepsilon_{\rm ox}$ of the high-k material results in higher effective mobility in the low-field region but lower effective mobility in the high-field region. This is because the RIRS/RCS-limited mobility dominates in the high/low-field region, while the RIRS (RCS) scattering is enhanced (weakened) as the dielectric constant of the high-k layer increases. Therefore, to obtain an optimum hole mobility in both low-field region and high-field region for high-k dilelectric/SiO_2 gate stacked MOSFETs, a moderate permittivity of high-k dielectric, e.g. $\varepsilon_{\rm ox} = 18 - 25$, is preferable according to Fig.7.

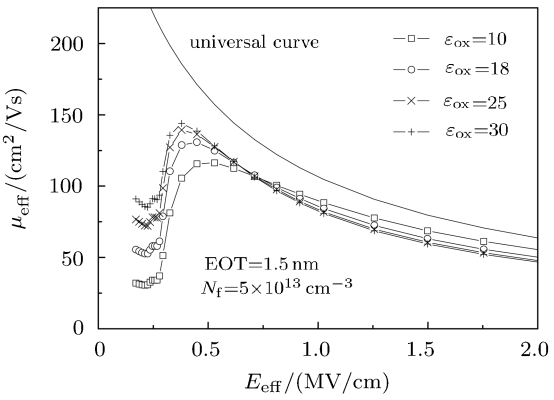


Fig.7. Impact of RIRS and RCS on effective hole mobility for different $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm int}$.

4. Summary

A physical model has been proposed to simulate carrier's mobility degradation in MOSFETs with high-k dielectric/interlayer stacked gate, such as HfO_2/SiO_2 stacked gate dielectrics. Extra charges are induced in both gate electrode and channel due to the rough interface of high-k dielectric/interlayer in such a stacked gate. The carriers are scattered by these extra induced charges, as well as fixed charges near the high-k dielectric/interlayer interface. The carriers mobility degradation caused by aforementioned scattering mechanisms is calculated using the relaxation-time approximation. By adjusting parameters of $\Delta_{\rm m}$, Λ and $N_{\rm it}$, the simulated results agree reasonably with experimental data. The effects of some parameters, e.g. rms $\Delta_{\rm m}$, correlation-length Λ, the thickness of interlayer (SiO_2), permittivities of high-k dielectric and interlayer, on degradation of hole mobility are also discussed. Simulated results show that the hole mobility is reduced as the thickness of the SiO_2 interlayer decreases. The interface-roughness scattering becomes strongest as the correlation length Λ approaches the inverse of the thermal de Broglie wave number ($k_{\rm th}^{-1}$). Therefore, the processing condition of gate dielectrics should be optimized to avoid $\Lambda \sim k_{\rm th}^{-1}$. A smooth interface between high-k dielectric and interlayer as well as moderate permittivities of high-k dielectrics ($\varepsilon_{\rm ox} = 18 - 25$) is highly desired to improve carriers mobility while keeping low EOT in such gate-stacked MOSFETs.

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