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Study of total ionizing dose radiation effects on enclosed gate transistors in a commercial CMOS technology*

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This paper studies the total ionizing dose radiation effects on MOS (metal-oxide-semiconductor) transistors with normal and enclosed gate layout in a standard commercial CMOS (compensate MOS) bulk process. The leakage current, threshold voltage shift, and transconductance of the devices were monitored before and after γ-ray irradiation. The parameters of the devices with different layout under different bias condition during irradiation at different total dose are investigated. The results show that the enclosed layout not only effectively eliminates the leakage but also improves the performance of threshold voltage and transconductance for NMOS (n-type channel MOS) transistors. The experimental results also indicate that analogue bias during irradiation is the worst case for enclosed gate NMOS. There is no evident different behaviour observed between normal PMOS (p-type channel MOS) transistors and enclosed gate PMOS transistors.

Keywords: MOS transistors, radiation effects, total dose, layout
PACC: 6180, 7340Q

1. Introduction

As the linchpin integrated circuits, metal oxide semiconductor (MOS) structures are crucial elements in most silicon device technologies. Many integrated circuits operate in radiation environments, such as space, nuclear weapon application environment, and high-energy physical experiments.[1−4] Radiation total ionizing dose (TID) effects degrade the performance and reliability of MOS Field Effect Transistors (MOSFETs) and integrated circuits.[5,6] The radiation introduces both oxide-trapped charge and interface-trapped charge, which cause a shift in the threshold voltage.[5−11] Oxide-trapped charge is almost universally found to be net positive in MOS gate oxides,[12] which leads to negative threshold voltage shift in both n-type channel MOS (NMOS) and p-type channel MOS (PMOS) transistors during radiation exposure. Interface-trapped charge is predominantly negative for NMOS, leading to positive threshold voltage shift, and positive for PMOS, leading to negative threshold voltage shift.[6,12] Radiation-induced threshold voltage shift depends on oxide thickness t_{ox} according to a square law.[13]

Due to positive charge trapping, TID radiation may induce an inversion layer in oxide isolation regions (field oxide structures) at the bird's beak with local oxidation of silicon (LOCOS) technology, giving rise to transistor edge leakage current paths from the drain to the source for NMOS transistors,[14−17] as shown in Fig.1.

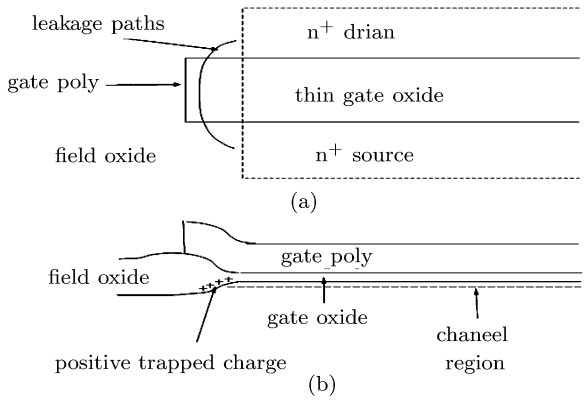


Fig.1. Schematic illustration of the LOCOS isolation structure of a NMOS transistor.

The MOS integrated circuits are radiation hardened by using special procedures in design, and/or processing operations.[6] CMOS hardness-by-design (HBD) approaches[1] use design techniques to over-

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come the inherent susceptibilities of commercial CMOS technologies to radiation effects. Special layout design is a very important part of HBD approaches.

Radiation induces source-to-drain leakage in NMOS transistors through the formation of an inversion layer at the edge of the active area due to the radiation-induced accumulation of positive charge in oxide. Enclosed geometry (or edgeless) NMOS layout structure along with p^+ guard rings (shown in Fig.2) can eliminate the excessive radiation-induced edge leakage and prevent leakage current between components. Because any current between the source and drain has to flow underneath the gate (thin oxide region), so there is no current path possible underneath the field oxide or along the edge of the active area.[18]

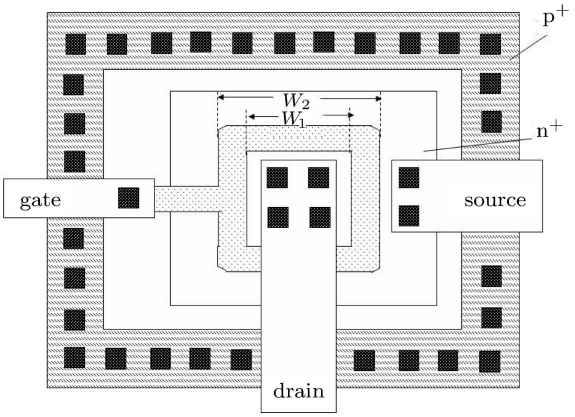


Fig.2. Layout structure of an enclosed NMOS.

The aim of this paper is to analyse the TID radiation effects of MOS transistors with enclosed layout in a commercial standard CMOS process. Under the ^{60}Co γ irradiation experimental condition, measurements of leakage current, threshold voltage, and transconductance before and after irradiation are presented, and the relevant results are discussed.

2. Experiments

2.1. Devices

The MOS transistors studied in this work were designed and processed in a standard commercial 0.6 μm CMOS/bulk process.

In order to evaluate the hardened enclosed layout, both PMOS and NMOS transistors were designed with normal layout and enclosed layout as shown in Fig.2. The channel length of normal transistors is 0.6 μm with the ratio of channel width and length (W/L) being 60μm/0.6μm. The effective ratio $(W/L)_{\rm eff}$ of enclosed gate transistors is calculated by the following equation:[18]

$$(W/L)_{\rm eff} = 8/\ln(W_2/W_1), \tag{1}$$

here $W_1 = 14.5$ μm, $W_2 = 15.7$ μm, so the $(W/L)_{\rm eff}$ is 100, the same as the W/L of normal devices.

2.2. Irradiation procedures

The devices were irradiated with a ^{60}Co source at room temperature. Since MOS radiation damage effects have a strong bias dependence,[6] the devices were biased under three different conditions during radiation exposure. The devices bias voltages during irradiation are shown in Table 1. The cases of Group A and Group C are logic bias, the gate-source voltage $V_{\rm GS}$ is 0V and the drain-source voltage is 5V(–5V for PMOS) in Group A, while $V_{\rm GS}$ is 0V and $V_{\rm DS}$ is 5V(–5V for PMOS) in Group A. The case of Group B is analogue bias with $|V_{\rm GS}| = 1.4$ V and $|V_{\rm DS}| = 1$ V. The base-source voltage $V_{\rm BS}$ is 0V for all transistors. For NMOS, the devices in Group C were under logic worst-bias.[19] The devices of Group B, Group C and some devices of Group A were irradiated with a total dose of about 3 kGy(Si) at a rate of 0.52Gy(Si)/s. They were measured before and after the irradiation. The other devices of Group A were irradiated up to 10 kGy(Si) total dose with intermediate measurements at 2.5-,5-, 7.5-,and 10 kGy(Si) dose with a dose rate of 0.68Gy(Si)/s. The edge leakage, threshold voltage shift, and transconductance were measured at room temperature with $|V_{\rm DS}| = 0.8$V.

Table 1. Devices bias during irradiation.

		Group A	Group B	Group C
$V_{\rm GS}$/V	NMOS	0	1.4	5
	PMOS	0	–1.4	–5
$V_{\rm DS}$/V	NMOS	5	1	0
	PMOS	–5	–1	0
$V_{\rm BS}$/V		0	0	0

3. Experimental results

3.1. Leakage current

Figure 3 shows drain current versus gate voltage characteristics pre- and post-irradiation for normal NMOS (as shown in Fig.3(a)) and enclosed gate

NMOS (as shown in Fig.3(b)). For normal NMOS transistors, the significant leakages are observed from Fig.3(a). The leakage currents are rising with the increase of V_{GS}, and unacceptable in case of the devices in Group B ($V_{GS} = 1.4$ V) and Group C ($V_{GS} = 5$ V). This could be explained by the contribution due to the oxide-trapped charge at the bird's beak. The gate bias voltage makes the electron–hole pairs induced by radiation separate quickly during irradiation, which decreases the recombination of the electrons and holes, leading more holes trapped in the edge oxide. Therefore, the higher V_{GS} voltage biases, the more easily inversion layer formed at the bird's beak, and leads more leakage current. Since the voltage V_{GS} in Group A is the lowest ($V_{GS} = 0$), and which in Group C is the highest ($V_{GS} = 5$ V), the leakages of Group A and C shown in Fig.3(a) are also the lowest and the highest, respectively.

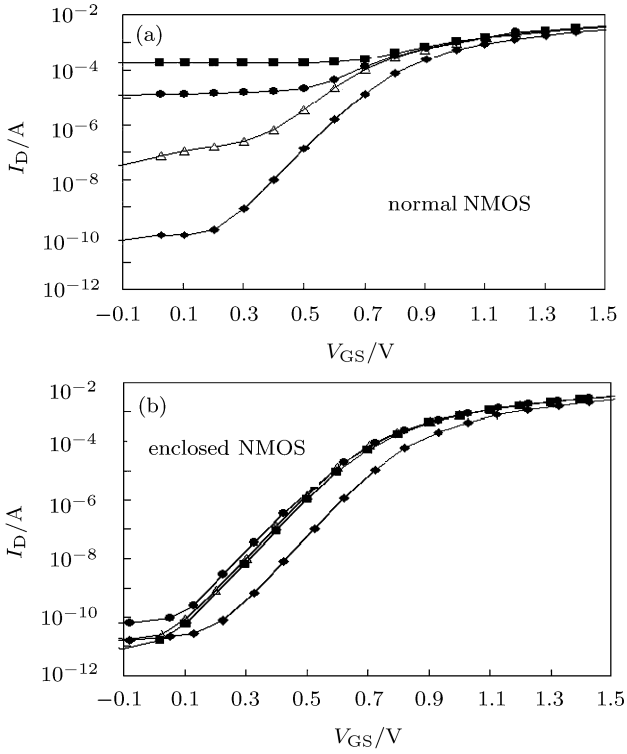


Fig.3. Drain current I_D versus gate voltage pre- and post-irradiation for (a) normal NMOS transistors and (b) enclosed NMOS transistors under different bias conditions during irradiation. The total dose was 3 kGy(Si) at 0.52Gy(Si)/s dose rate. The measurements were carried out with V_{DS}=0.8V. —♦— pre-rad, —Δ— post-rad (Group A), —●— post-rad (Group B), —■— post-rad (Group C)

As expected, the leakages are evidently eliminated for enclosed gate NMOS transistors after irradiation, which is illustrated in Fig.3(b). The leakages almost remain unchanged (less than 10^{-10}A) in different bias conditions during irradiation. Since there is no bird's beak at the edge of the transistor, it shows no increased leakage current induced by the parasitic field transistors for enclosed gate NMOS.

The drain current behaviour of normal and enclosed gate PMOS transistors is shown in Fig.4. Unlike NMOS transistors, measurements of irradiated PMOS transistors show no evident different performance between normal and enclosed layout devices. The magnitude of PMOS leakage maintains a very low level after irradiation, below the order of 10^{-12} A, and the data is out of the range of the plot in Fig.4. The result shows that enclosed layout is not necessary for PMOS, because the positive charges accumulated in the oxide push n-substrate more into accumulation without danger of the formation of an inversion layer. Therefore, there is no leakage path at the edges of PMOS, and the leakage current in PMOS transistors with any layout structure can usually be neglected.

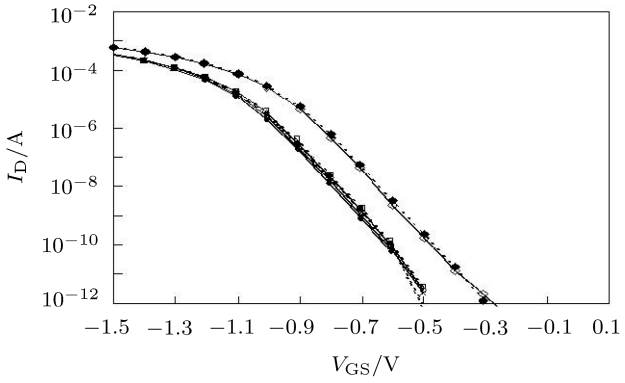


Fig.4. Drain current I_D versus gate voltage pre- and post- irradiation for a normal PMOS (solid lines) and an enclosed PMOS (dashed lines) transistors under different bias conditions during irradiation. The total dose was 3 kGy(Si) at 0.52Gy(Si)/s dose rate. The measurements were carried out with $|V_{DS}| = 0.8$ V. —◇— normal (pre-rad). —●— normal (post-rad, Group A), —×— normal (post-rad, Group B), —○— normal (post-rad, Group C), —♦— enclosed (pre-rad), —Δ— enclosed (post-rad, Group A), ---■--- enclosed (post-rad, Group B), ---□--- enclosed (post-rad, Group C).

3.2. Threshold voltage shift

In order to analyse the behaviour of the oxide-trapped and the interface-trapped charge, the threshold voltage shift ΔV_{th} has been split into a contribution due to the interface-trapped charge ΔV_{Nit} and a contribution due to the oxide-trapped charge ΔV_{Not},

which are extracted from the curves in Figs.3 and 4 by using the techniques described in Ref.[7].

The threshold voltage shifts $\Delta V_{\rm th}$, $\Delta V_{\rm Nit}$, and $\Delta V_{\rm Not}$ of NMOS and PMOS transistors after a 3 kGy(Si) irradiation are shown in Table2 and Table3, respectively. It can be seen that $\Delta V_{\rm Nit}$ is positive for NMOS transistors and negative for PMOS transistors, while $\Delta V_{\rm Not}$ is negative for both NMOS and PMOS transistors. Comparing the data in Table 2, we find that the threshold voltage shifts of enclosed gate NMOS are much smaller than that of normal NMOS. The voltage shifts of normal NMOS show strong dependence on the bias condition. The $\Delta V_{\rm th}$ varies from –150 mV (in Group A, $V_{\rm GS}$ = 0 V) to –658 mV (in Group C, $V_{\rm GS}$ = 5 V), increasing with $V_{\rm GS}$. Although in the case of the enclosed gate NMOS, $\Delta V_{\rm th}$ also varies with different bias, –131 mV in Group A, –142 mV in Group B, and –99 mV in Group C, the dependence of threshold voltage shift on $V_{\rm GS}$ is not as strong as that in the normal NMOS. The oxide-charge induced by irradiation is much more in thick field oxide layer at the bird's beak than in the thin gate oxide layer. So the charge variation with the bias is more at the edges. Because the enclosed gate NMOS is edgeless, the threshold voltage shift just induced by the oxide-charge in thin gate oxide is smaller. According to the data in Table 2, the trend of threshold voltage shift depending on $V_{\rm GS}$ for enclosed gate NMOS is quite different from that for normal NMOS. Without the thick oxide edges, the electric field strength E of enclosed gate NMOS in the 12nm thin gate oxide under 5V bias is high enough (about $\sim 10^6$ V/cm) to make the oxide-charge $N_{\rm ot}$ and interface traps $N_{\rm it}$ decrease with the increase of E.[20–23] Therefore the largest shift does not appear under the bias of $V_{\rm GS}$ = 5 V as normal NMOS, it appears under the analogue bias of $V_{\rm GS}$ = 1.4 V. It implies that, the worst case for enclosed gate NMOS is analogue biasing.

Table 2. Threshold voltage shifts of NMOS transistors after 3 kGy(Si) irradiation.

	Group A			Group B			Group C		
	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV
Normal NMOS	345	–495	–150	947	–1160	–213	2514	–3172	–658
Enclosed NMOS	13	–144	–131	42	–184	–142	5	–104	–99

Table 3. Threshold voltage shifts of PMOS transistors after 3 kGy(Si) irradiation.

	Group A			Group B			Group C		
	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV	$\Delta V_{\rm Nit}$/mV	$\Delta V_{\rm Not}$/mV	$\Delta V_{\rm th}$/mV
Normal PMOS	–3	–140	–143	–3	–114	–117	–5	–126	–131
Enclosed PMOS	–2	–140	–142	–2	–131	–148	–14	–136	–150

According to the data in Table 3, the enclosed layout shows no advantage for PMOS in comparison with the normal layout. In fact, the case seems a little worse for enclosed gate PMOS in Group B and C. Since $V_{\rm GS}$ is negative, the number of oxide-trapped positive charges induced by irradiation moving near the interface forming interface-trapped charges in Group B and C is smaller than that in Group A, where $V_{\rm GS}$ = 0. Because of the slight magnitude, the threshold voltage shifts ($\Delta V_{\rm Nit}$) of enclosed gate NMOS and all PMOS transistors can almost be neglected.

Figure 5 shows the threshold voltage shift $\Delta V_{\rm th}$, $\Delta V_{\rm Nit}$, and $\Delta V_{\rm Not}$ as a function of the total dose for some enclosed gate NMOS and PMOS transistors in Group A. As shown in Fig.5(a), the magnitude of $\Delta V_{\rm Nit}$, and $\Delta V_{\rm Not}$ increases with total dose for NMOS. Since $\Delta V_{\rm Nit}$ and $\Delta V_{\rm Not}$ have different signs, the magnitude of $\Delta V_{\rm th}$ does not rapidly increase, –0.29V at the highest dose of 10 kGy(Si). Figure 5(b) shows the case of PMOS, both $\Delta V_{\rm Nit}$, and $\Delta V_{\rm Not}$ are negative, so that $\Delta V_{\rm th}$ is more negative, –0.45V at the does of 10 kGy(Si). The oxide-trapped charge increases with the dose rising, so the magnitude of $\Delta V_{\rm Not}$ has a increase tend as NMOS. Unlike NMOS, the magnitude of $\Delta V_{\rm Nit}$ in PMOS shows increase at lower dose, while it shows saturation at higher dose. The formation of interface-trapped charge is complex. The density of the defects at the interface under gate oxide which might become interface-traps in PMOS is much

smaller than in NMOS. Limited by the finite number of defects, the $\Delta V_{\rm Nit}$ of PMOS shows saturation at higher dose.

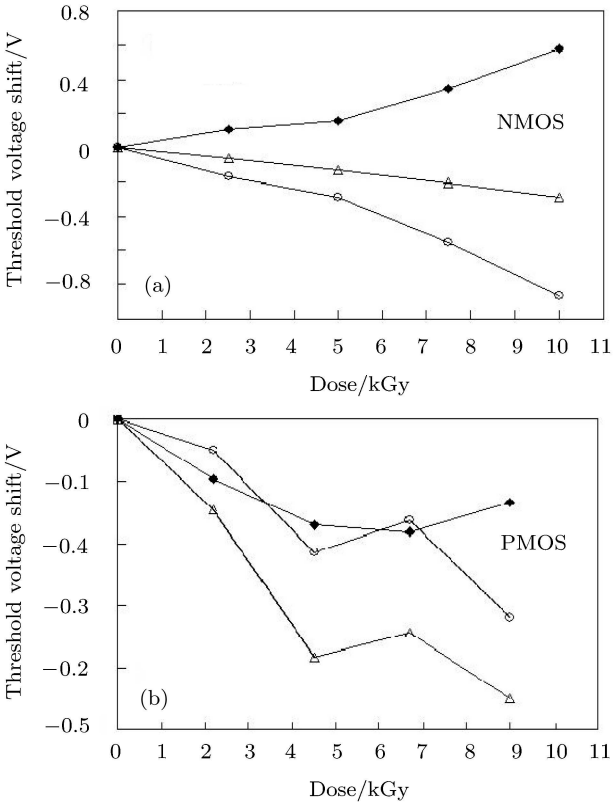


Fig.5. Threshold voltage shift after irradiation versus total dose for (a) an enclosed NMOS transistor and (b) an enclosed PMOS transistor. The devices were biased at $V_{\rm GS}$=5V (-5V for PMOS) during irradiation with 0.68Gy(Si)/s dose rate. The measurements were carried out with $|V_{\rm DS}|$ = 0.8 V. —♦— $\Delta V_{\rm Nit}$, —○— $\Delta V_{\rm Not}$, —Δ— $\Delta V_{\rm th}$.

3.3. Transconductance

The transconductance $g_{\rm m}$ is extracted from the $I_{\rm D}$-$V_{\rm GS}$ curves in Figs.3 and 4. The $g_{\rm m}$ behaviour of NMOS devices in the drain current region up to 1mA is shown in Fig.6(a). The transconductances show almost no change except the case of normal NMOS in Group C ($V_{\rm GS}$=5V bias condition). Since the $g_{\rm m}$ relates to the interface traps, more interface traps leads more $g_{\rm m}$ decrease. It can be inferred from Table 2 that the density of interface traps $N_{\rm it}$ increases with bias voltage, and it is much more in normal NMOS than in enclosed gate NMOS. Thereby the worst degrade of $g_{\rm m}$ appears in the normal NMOS of Group C, from 7% (at $I_{\rm D}$ = 1 mA) to 92% (at $I_{\rm D}$ = 0.2 mA).

The transconductance of PMOS devices is shown in Fig.6(b) with the drain current region up to 0.2 mA. The $g_{\rm m}$ of the devices in Group C shows 6% decrease (at $I_{\rm D}$ = 0.2 mA), while the $g_{\rm m}$ of the devices in Group B remains unchanged. For the reason described in Sec.3.1, the characters of PMOS whit both normal and enclosed gate are almost the same under any bias conditions.

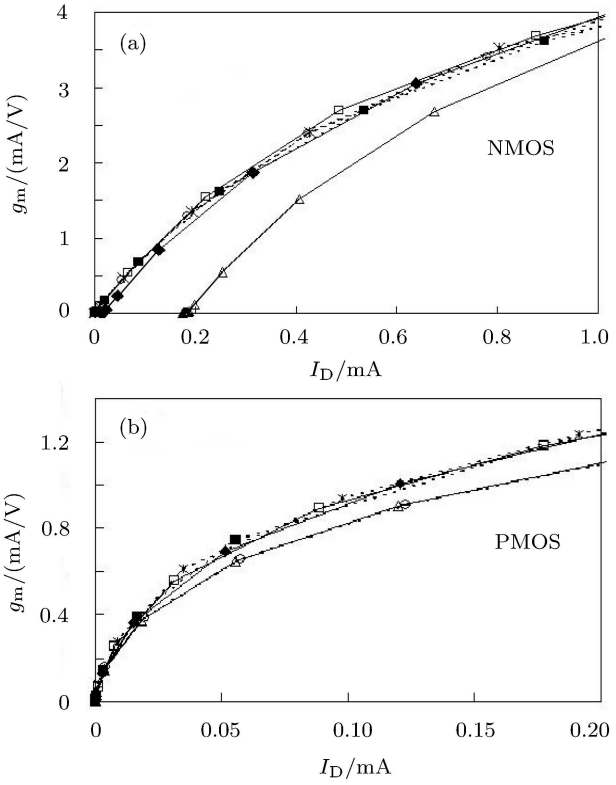


Fig.6. Transconductance $g_{\rm m}$ versus drain current I_D before and after irradiation for (a) a normal NMOS transistor (solid lines) and an enclosed NMOS transistor(dashed lines), and (b) a normal PMOS transistor (solid lines) and an enclosed PMOS transistor(dashed lines). The total dose was 3 kGy(Si) at 0.52Gy(Si)/s dose rate. The measurements were carried out with $|V_{\rm DS}|$ = 0.8 V. —□— normal(pre-rad), —♦— normal(post-rad, Group B), —Δ— normal(post-rad, Group C), ---∗--- enclosed(pre-rad), —■— enclosed(post-rad, Group B), ---○--- enclosed (post-rad, Group C).

4. Conclusion

The TID radiation effects on enclosed gate MOS transistors in a standard commercial 0.6 μm CMOS /bulk process have been investigated by γ-ray irradiation experiments. A comparison with normal and enclosed gate transistors for both NMOS and PMOS transistors has been carried out. The experimental results indicate that in the case of NMOS transistors, the enclosed layout not only effectively eliminates the leakage current but also reduces the threshold voltage shift and transconductance degradation due to irradi-

ation. The threshold voltage shift increases with total dose for both NMOS and PMOS. The shift appears strong dependence on bias condition during irradiation for normal NMOS, while it is less sensitive to the bias condition for PMOS and enclosed gate NMOS. The experimental results also indicate that analogue bias is the worst condition during irradiation for enclosed gate NMOS. No evident variation in leakage current, threshold voltage shift, or transconductance has been observed between normal PMOS and enclosed gate PMOS.

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