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New CMOS compatible super-junction LDMOST with n-type buried layer*

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A new super-junction lateral double diffused MOSFET (LDMOST) structure is designed with n-type charge compensation layer embedded in the p^--substrate near the drain to suppress substrate-assisted depletion effect that results from the compensating charges imbalance between the pillars in the n-type buried layer. A high electric field peak is introduced in the surface by the pn junction between the p^--substrate and n-type buried layer, which given rise to a more uniform surface electric field distribution by modulation effect. The effect of reduced bulk field (REBULF) is introduced to improve the vertical breakdown voltage by reducing the high bulk electric field around the drain. The new structure features high breakdown voltage, low on-resistance and charges balance in the drift region due to n-type buried layer.

Keywords: super-junction, LDMOST, n-type buried layer, REBULF, breakdown voltage
PACC: 6120J, 7280C, 7340Q

1. Introduction

Vertical double diffused metal oxide semiconductor field effect transistors (MOSFETs) based on the super-junction (SJ) concept[1,2] have been proposed to further improve the trade-off characteristics between the breakdown voltage (BV) and the specific on-resistance ($R_{\rm on,sp}$). In theory, the SJ structure results in high BV due to charges balance in the n and p pillars and low $R_{\rm on,sp}$ is achieved by highly doping in the n-pillars. The desired performance of the LDMOS (lateral double diffused MOSFET) is to minimize the conduction losses by the lowest $R_{\rm on,sp}$. Several technologies and structures have been proposed, such as RESURF (reduced surface field), LDMOS.[3] PSOI (partial silicon on insulator) with p-type buried layer,[4] buried oxide double step MOSFET[5] and the several new structures[6−8] based on RESURF technology and super-junction concept.[9] However, it is difficult to fabricate the structures with buried oxide double step and PSOI. In SJ-LDMOST the p-type pillars implemented on a p-substrate cannot be depleted completely before the electric field of silicon reaches its critical breakdown voltage resulting from substrate-assisted depletion n-type pillars. To eliminate this effect, several structures have been reported.[10,11] In RESURF LDMOS, the vertical BV can be increased by adopting REBULF technology.[12,13] The high bulk electric field around the drain is reduced in REBULF LDMOS. As the critical electric field of silicon is reached, the vertical BV of REBULF LDMOS is improved compared with RESURF LDMOS.

In this paper, we report, for the first time, a new SJ-LDMOST with n-type buried layer (n-buried SJ-LDMOST shown in Fig.1) to suppress the charges imbalance effect for high lateral BV by a more uniform surface electric field due to electric field modulation effect, and high vertical BV by REBULF effect. So, there are three key features in n-buried SJ-LDMOS. (i) The charge imbalance effect between the n and p pillars of SJ is suppressed by n-type buried layer. (ii) A more uniform surface electric field distribution in the drift region is obtained due to electric field modulation effect produced by a additional electric field between the p^--substrate and n-type buried layer. (iii) A new electric field peak is produced to reduce the high bulk electric field around the drain, which increases the vertical BV resulting from the REBULF effect.

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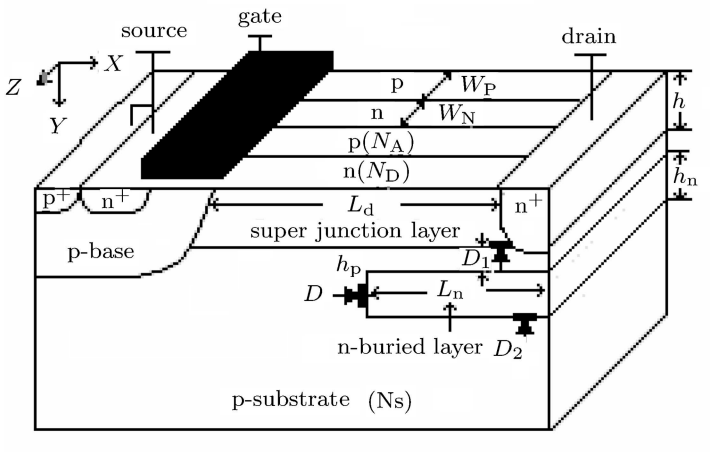


Fig.1. Three-dimensional view of the n-buried SJ-LDMOST.

2. Device structure and description

The master feature in the proposed n-buried SJ-LDMOST is the use of the partial n-type compensation layer implanted near the drain in the p^--substrate of which the concentration is 1.2×10^{14} cm^{-3} used in this paper. The concentration of n-type buried layer (N_n) is optimized according to different parameters of device. N_D and N_A are the concentrations of n-type and p-type pillars, respectively. L_d and L_n are the lengths of the super-junction and n-type buried layer, and the lengths of the source and channel regions are 2 and 3 μm in the discussion of this paper respectively. W_N and W_P are the widths of n-type and p-type pillars, and they are 1 μm in this paper. As the drain voltage is increases in the off-state, the n-pillars of the n-buried SJ-LDMOST are depleted by the neighbouring p-type pillars and the p-type substrate. The p-pillars can also be affected by the neighbouring n-pillars and the n-type buried layer when the charges of the p-type substrate above the n-type buried layer are depleted completely at a high enough drain voltage. In the n-buried SJ-LDMOST structure, both pillars are depleted by lateral (Z direction) and vertical (Y direction) electric fields, which causes the charges balance between the pillars, while in the conventional SJ structure only the n-pillars are affected by the p-type substrate.

The obvious merit of this structure is a new electric field peaks produced by the junctions of the partial n-type buried layer and p-type substrate along the lateral and vertical directions (shown in Figs.1 and 2), which modulate the surface and bulk electric field distributions. A uniform surface electric field distribution is obtained compared with buffered SJ-LDMOST[10] due to the new lateral electric field peak. This effect is similar to that in Ref.[14], in which a p-type buried layer is embedded in the substrate near the channel to modulate the concentration and electric field of the drift region. However, in n-buried SJ-LDMOST it is different from that in Ref.[14] that the n-type charges compensation layer takes effect near the drain to deplete the assisted p-type pillars in the super-junction drift region. The new electric field peak along the vertical direction reduces the bulk high electric field around the drain. It results from an important effect of REBULF. h_p is the distance from n-type buried layer to the bottom of super-junction layer that adjusts the modulation effect by modulating the height of new electric field peaks.

3. Results and discussion

The lateral electric field distributions on the silicon surface of the conventional, buffered and n-buried SJ-LDMOSTs are shown in Fig.2(a) by using simulation software ISE,[15] respectively. It is shown that there are two electric field peaks in the buffered and n-buried SJ-LDMOSTs compared with the conventional SJ-LDMOST along the silicon surface: one appears at the p n junction near the channel and the other at the n^+n junction near the drain, which results from n- and p-pillars depleted completely by suppressing substrate- assisted depletion effect. It is obvious that a new electric field P_k, which results in a more uni-

form electric field distribution than that of buffered SJ-LDMOS, is seen in n-buried SJ-LDMOST. In LDMOST, the low specific on-resistance will be obtained if the surface electric field can be uniform at the given BV, which has been explained by Ref.[16]. With the same length of the drift region, a higher BV can be achieved for the more uniform surface electric field distribution due to the increase of $\bar{E}_x$ which is the average lateral electric field. Thus, the breakdown voltage (375 V) in n-buried SJ-LDMOST is higher than that (287 V) in buffered SJ-LDMOS and that (204 V) in its conventional counterpart. Figure. 2(b) shows the lateral electric field distributions on the silicon surface of n-buried SJ-LDMOST for different values of $h_{\rm p}$. It is shown that the height of $P_{\rm k}$ increases as $h_{\rm p}$ decreases, which indicates that the parameter $h_{\rm p}$ adjusts the electric field modulation effect. The breakdown voltage can be saturated when $h_{\rm p}$ is designed to optimize the surface electric field.

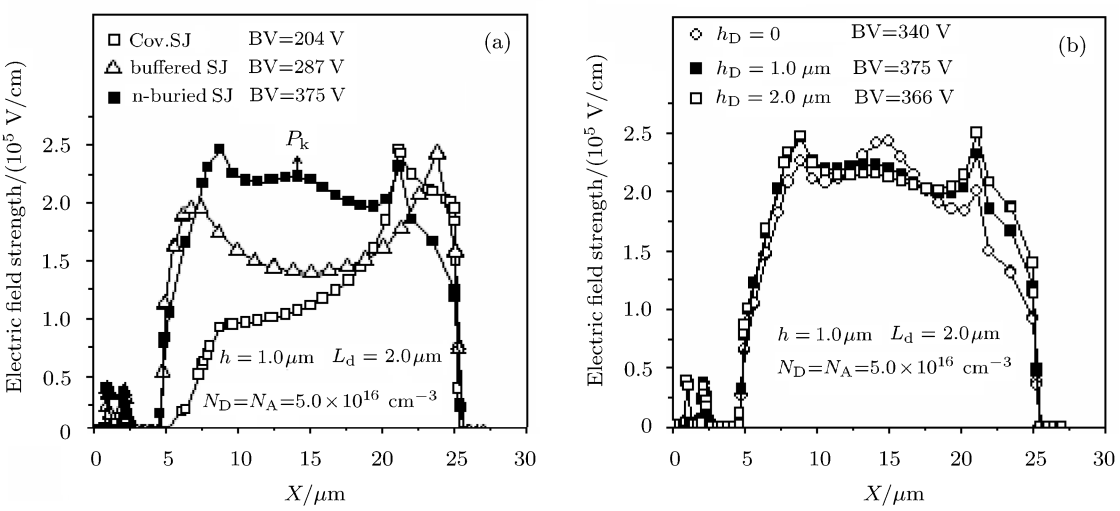


Fig.2. Lateral electric field distributions (a) for three kinds of SJ- LDMOSTs structures and (b) for n-buried SJ-LDMOST at different values of $h_{\rm p}$ with $L_{\rm n} = 1/2L_{\rm d}$.

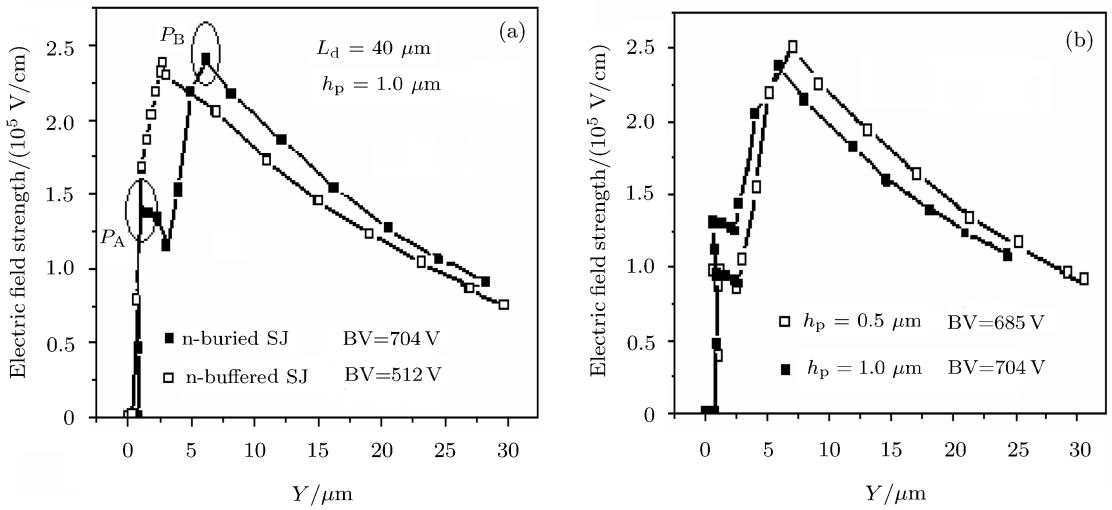


Fig.3. Vertical electric field distributions around the drain (a) for two kinds of SJ-LDMOST structures and (b) for n-buried SJ-LDMOST at different values of $h_{\rm p}$ with $L_{\rm n} = 1/2L_{\rm d}$.

The vertical electric field distribution around the drain was shown in Fig.3. Under the reverse bias condition, the electric field around the drain of n-buried SJ-LDMOST (Fig.3(a)) is divided into two parts (their peaks are denoted by P_A and P_B), which are produced by D_1 and D_2 junctions. In this way, the maximal electric field around the drain becomes lower than that of the buffered SJ-LDMOST. The heights of P_A and P_B can be modulated by parameter h_p, which is shown in Fig.3(b). The height of P_A is improved as h_p enhanced, increasing the vertical breakdown voltage. The height of P_B is the critical break electric field of silicon as n-buried SJ-LDMOS reaches its breakdown voltage. As a new peak P_k must be produced to optimize the surface electric field, h_p cannot be enhanced much enough to equate P_A with P_B.

Figure 4 shows the breakdown voltage as a function of L_n and N_n. It is shown from Fig.4(a) that the breakdown voltages are peaks when L_n is 1/2 L_d, which results from the uniform surface electric field when the location of P_k is at 1/2 L_d. So, in the following discussion, L_n is adopted by 1/2 L_d. The dependence of breakdown voltage on N_n is shown in Fig.4(b) for the different values of L_d. It is indicates that the breakdown voltages achieve their peaks when the condition of charges balance is satisfied. The h_n is the thickness of n-buried layer, which is 2 μm in this paper. The h_n will alter according to the process. However, the dose of n-buried larger, which is $h_n \times N_n$, is not changed.

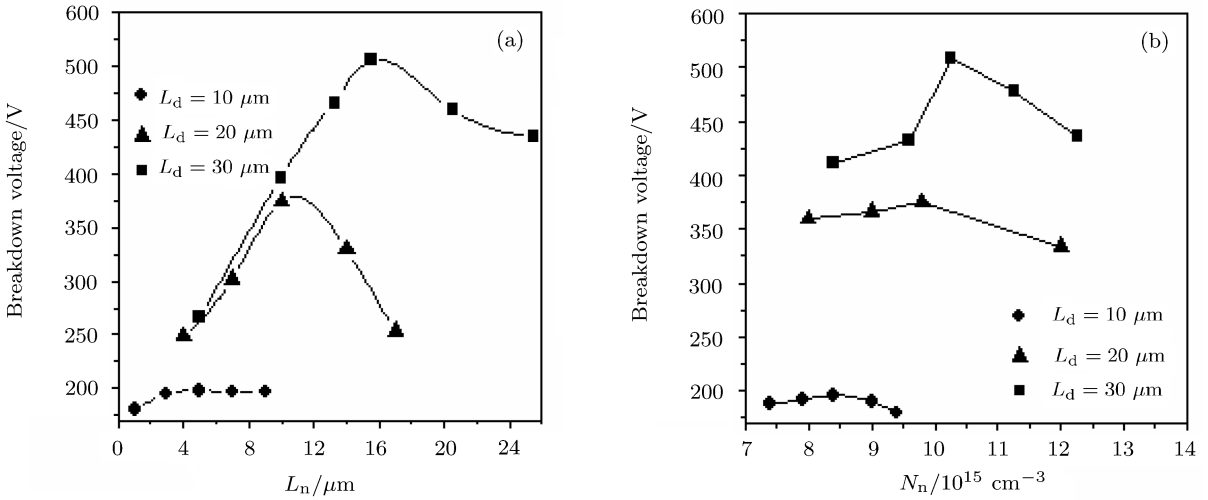


Fig.4. Breakdown voltage versus L_n (a) and N_n (b) in n-buried SJ- LDMOST with $N_A = N_D = 5.0 \times 10^{16}$ cm^{-3}, $h_n = 2$ μm; and $h_p = 1$ μm.

The dependences of breakdown voltage on the concentration of drift region are illustrated in Fig.5 with the different values of L_d in n-buried SJ-LDMOST. The concentration of drift region has an optimum one for different values of L_d when the 3D RESURF, which indicates an optimized surface electric field like Fig.2(a), is satisfied. The optimum dose for n-buried SJ-LDMOS, which is $N_D \times h$, is higher than the accepted double RESURF or Cool MOS dose of 2×10^{12} cm^{-2}. It is because that the additive electric field resulting from p-type substrate compensates the charges of n-type pillars compared with Cool MOS. Due to the absence of the electric field along the Z direction the dose of double RESURF is lower than that of n-buried SJ-LDMOS.

In general, the longer the drift region is, the higher the breakdown voltage will be. But it should be noted that the breakdown voltage of device can also be saturated due to the saturation of the vertical breakdown voltage. In the n-buried SJ-LDMOST structure, the saturation length of drift region is larger than that of the buffered SJ-LDMOST since the vertical breakdown voltage of n-buried SJ-LDMOST is higher than that of buffered SJ-LDMOST due to the REBULF effect. It can be seen from Fig.6 that the maximum breakdown voltage in n-buried SJ-LDMOST increases drastically by ΔV_2 compared with that of n-buffered SJ resulting from the REBULF effect. For a given drift region length, the breakdown voltage of n-buried SJ-LDMOST increases by ΔV_1 compared with that of buffered SJ-LDMOST due to more uniform surface electric field. It is easily obtained from Fig.6

that the maximum breakdown voltage of n-buried SJ-LDMOST reaches 756 volts while the maximum breakdown voltage in buffered SJ-LDMOST is 530 volts.

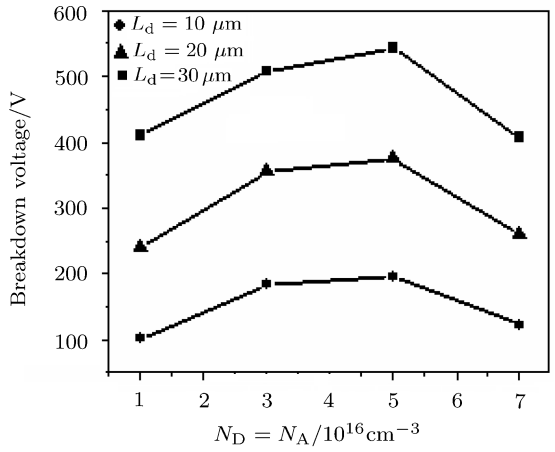


Fig.5. Breakdown voltage as a function of the concentration of drift regions for n-buried SJ-LDMOSTs with $L_n = 1/2\ L_d$, $h_n = 2\ \mu m$, and $h_p = 1\ \mu m$.

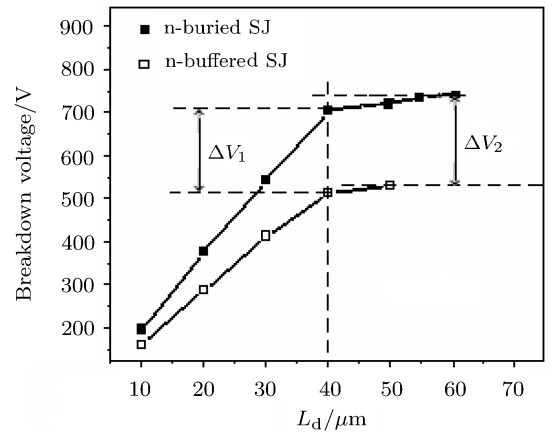


Fig.6. Breakdown voltage versus L_d for buffered and n-buried SJ-LDMOSTs with $h = h_p = 1\ \mu m$, and $N_A = N_D = 5.0 \times 10^{16}\ cm^{-3}$

The values of $R_{on,sp}$ of the n-buried and buffered SJ-LDMOSTs versus BV are compared in Fig.7. The comparison demonstrates the performance of the n-buried SJ is superior to that of the buffered SJ, especially it has a high BV, which is due to uniform surface electric field. Although the partial n-type buried layer in the n-buried SJ is smaller than the n-type buffer layer in the buffered SJ, the effect of the larger $\bar{E}_x$ mentioned above on the $R_{on,sp}$ due to the uniform surface electric field is stronger than that in the additive n-type conductive layer. Figure 7 shows the on-state $I_{DS} - V_{DS}$ characteristics of the n-buried and conventional SJ-LDMOSTs indicating that n-buried SJ-LDMOST has a lower on-resistance than the conventional SJ-LDMOST.

In practical implementation of the n-buried SJ-LDMOST, the additional steps needed to implement the device involve implanting the phosphor or arsenic into p-substrate to form the n-type buried layer and the substrate above the n-type buried layer generated by epitaxy, which is similar to the process of n-buffered SJ-LDMOS. Although the n-type buried layer may diffuse out due to the thermal cycle, its total dose can be kept from changing, which does not affect the condition of REBULF to suppress the substrate- assisted depletion effect.

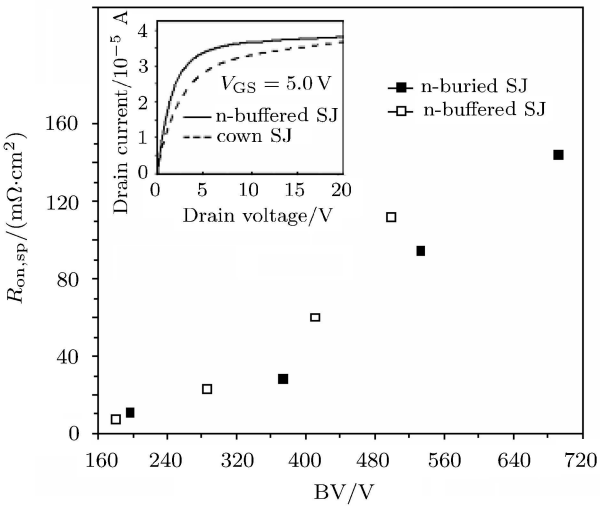


Fig.7. Values of $R_{on,sp}$ versus BV of n-buried and buffered SJ-LDMOST, and on-state characteristics of the conventional and n-buried SJ-LDMOSTs with $h = 1\ \mu m$, $h_p = 1\ \mu m$, and $N_A = N_D = 5.0 \times 10^{16}\ cm^{-3}$.

4. Conclusion

A new SJ-LDMOST structure, which has a partial n- type charge compensation layer implanted near the drain in p-substrate, is analysed. This structure eliminates the charges imbalance effect to achieves a high breakdown voltage while it maintains a lower on-resistance than the conventional SJ-LDMOST due to partial n-type charges. In addition, the lateral breakdown voltage of n-buried SJ-LDMOST is higher than that of buffered SJ-LDMOST resulting from more uniform surface electric field modulated by a new electric field peak produced by the pn junction between the partial n-type buried layer and p-type substrate. The vertical breakdown voltage is improved due to REBULF effect which reducing the high bulk electric field around the drain.

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