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Low voltage substrate current: a monitor for interface states generation in ultra-thin oxide n-MOSFETs under constant voltage stresses*

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The low voltage substrate current (I_b) has been studied based on generation kinetics and used as a monitor of interface states (N_{it}) generation for ultra-thin oxide n-MOSFETs under constant voltage stress. It is found that the low voltage I_b is formed by electrons tunnelling through interface states, and the variations of $I_b(\Delta I_b)$ are proportional to variations of N_{it} (ΔN_{it}). The N_{it} energy distributions were determined by differentiating $N_{it}(V_g)$. The results have been compared with that measured by using gate diode technique.

Keywords: interface states, substrate current, ultra-thin oxide, constant voltage stress
PACC: 7320A, 7340Q

1. Introduction

As one of the main sources of instability in metal–oxide–semiconductor field effect transistors (MOSFETs), interface state (N_{it}) generation has been an important reliability issue for over three decades.[1−18] An increase of N_{it} will not only degrade the threshold voltage and mobility, but also enhance subthreshold swing and noise. So, it is of importance to monitor it during reliability study. However, for ultra-thin oxide devices, a large direct tunnelling current makes the conventional measurement techniques, such as capacitance-voltage (C–V),[6] charge pumping (CP)[7,8] and direct current current–voltage (DCIV)[9] techniques unreliable or infeasible.

The low voltage stress-induced leakage current (LVSILC) was considered as a monitor of N_{it} generation for large area MOS capacitors[10,11] and long channel MOSFETs[12,13] in weak accumulation. However, in the case of small-dimension MOSFETs, LVSILC would not only result from the interface traps-assisted-tunnelling (TAT) so that this method is inaccurate.

This paper investigates the mechanism of low voltage stress-induced substrate leakage current in order to find its relation with N_{it}. Then, it is used as a monitor of N_{it} for ultra-thin oxide n-MOSFETs under a uniform stress.

2. Devices and experiments

The samples used in this work are n^+ polysilicon gate n-MOSFETs fabricated by standard 0.13 μm CMOS technology. The oxide films are thermally grown SiO_2 with physical thickness (t_{ox}) 1.9 nm measured by the high frequency C–V and quantum simulation method. The gate oxide area is 1.89×10^{-6} cm^2 with the ratio of channel width to channel length 10/0.3, and the substrate doping is 4×10^{17} cm^{-3}.

During degradation experiments, a constant voltage stress (CVS) was applied to the gate with the source, drain and substrate grounded. After each cycle of stress, current versus voltage (I–V), transfer characteristics and gate diode (GD) experiments were performed by HP4156B semiconductor analyser at 300 K.

3. Model

For a p-type MOS capacitor, LVSILC corresponds to electrons tunnelling from the gate into interface states where they recombine with the substrate majority carriers at $V_{FB} < V_g < 0$.[10] This is almost the case in long channel n-MOSFETs as source/drain current ($I_{s/d}$) is negligible in accumulation.[12] However, for short channel MOSFETs, the contribution

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of $I_{s/d}$ to I_g should not be ignored.[14] Figure 1(a) shows I–V curves for n-MOSFET in accumulation, the inset indicates the schematic diagram for current measurement. I_g equals approximately to $1.5I_b$ and $5I_{s/d}$(for symmetrical device, $I_s \approx I_d$), and the results are different from those in Ref.[12], in which I_g equals approximately to I_b. We believe the difference is due to the device dimension. For long channel devices, the source/drain extensions are negligible as compared with one of the channel, and the value of I_g is almost the same as that of I_b. However, with reducing channel length, the influence of $I_{s/d}$ on I_g should not be neglected. The $I_{s/d}$ is formed by gate electrons directly tunnelling into the drain/source conduction band at $V_{FB} < V_g < 0$, and it changes little with the stress level, the experimental data are shown in Fig.1(b).

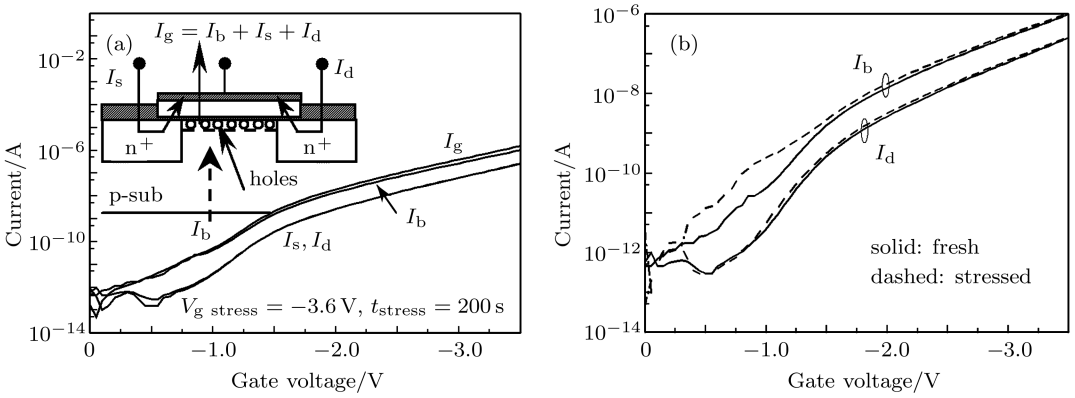


Fig.1. I–V curves of n-MOSFET in accumulation after CVS (a) and the stress induced current increment of I_b and I_d (b).

Therefore, the contribution of $I_{s/d}$ introduces an error if using LVSILC as a monitor for N_{it}. For investigating the current mechanism at low V_g, directly tunnelling simulation has been done. It was reported that I_g results from the electron tunnelling from the conduction band and I_b the electron tunnelling from the valence band.[15] However, Fig.2 shows this is not the case at low voltage, although good agreement is observed at high voltage.

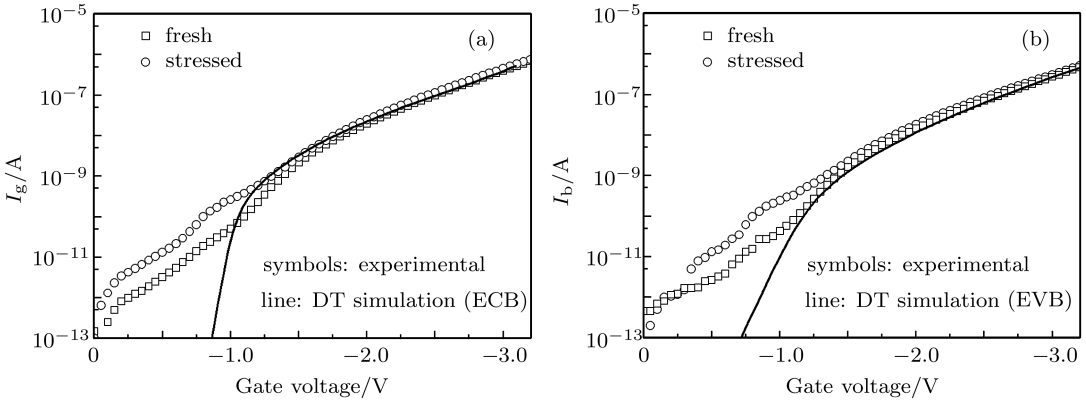


Fig.2. The direct tunnelling simulations of I_g (a) and I_b (b), with many discrepancies occurring at low voltages.

For short channel MOSFETs, the current tunnelling through interface states is I_g–I_d–I_s, which can be identified as I_b at $V_{FB} < V_g < 0$. It is proportional to the area of the channel (A_c), the interface state density (N_{it}) and the electron's tunnel probability (P_T).[10]

$$I_b \propto A_c N_{it} P_T, \tag{1}$$

where P_T is constant at the same V_g.

From Eq.(1), the I_b increment (ΔI_b) with stress voltage results from the variation of N_{it} at the same V_g, so I_b is regarded as a monitor of N_{it}:

$$\begin{aligned}\Delta I_b &= I_b - I_{b0} \propto A_c P_T (N_{it} - N_{it0}) \\ &\propto A_c P_T \Delta N_{it}, \end{aligned} \tag{2}$$

then we have

$$\Delta I_{\rm b}/I_{\rm b0} = \Delta N_{\rm it}/N_{\rm it0}. \quad (3)$$

When $V_{\rm g}$ varies from flat band, $V_{\rm FB} \approx -1\,{\rm V}$, to $0\,{\rm V}$, the gate Fermi level scans the Si–SiO_2 interface from the conduction band edge, $E_{\rm c}$, towards the Fermi level $E_{\rm F}$.[10] The tunnelling through $N_{\rm it}$ at $V_{\rm g} = V_{\rm FB}$ and $V_{\rm FB} < V_{\rm g} < 0$ are shown in Fig.3. As the current is proportional to $N_{\rm it}$ distribution below the gate Fermi level, $N_{\rm it}$ energy distribution ($D_{\rm it}$) can be extracted. Figure 3 (c) shows the gate to drain tunnelling at $V_{\rm FB} < V_{\rm g} < 0$. It does not involve the contribution of $N_{\rm it}$, but is included in $I_{\rm g}$.

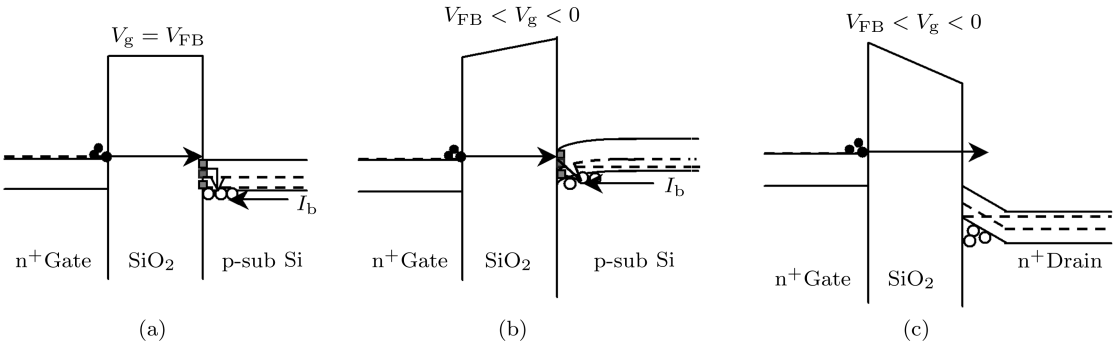


Fig.3. Schematic diagram illustrating the tunnelling through interface states and $I_{\rm b}$ formation reducing at $V_{\rm g} = V_{\rm FB}$ and (b) $V_{\rm FB} < V_{\rm g} < 0$; (c) the electron direct tunnelling from the gate–drain (GD) overlap region at $V_{\rm FB} < V_{\rm g} < 0$.

4. Results and discussions

Figure 4 shows the continuous evolution of $\Delta I_{\rm b}/I_{\rm b0}$ with stress time. Several peaks appear in the region from $V_{\rm g} = V_{\rm FB}$ to $V_{\rm g} = 0$. As discussed above, the peaks result from more $N_{\rm it}$ generation from which energy levels can be deduced by using the peak positions.

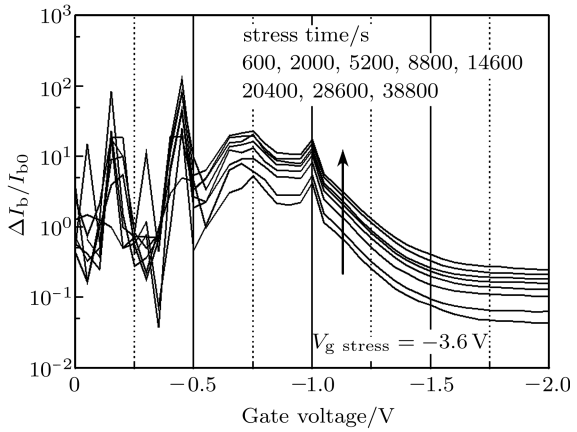


Fig.4. The relative variations of $\Delta I_{\rm b}$ with $V_{\rm g}$ measured after periodical CVS interruptions.

$\Delta I_{\rm b}$ kinetics is shown in Fig.5, and $\Delta I_{\rm b}/I_{\rm b0}$ follows a power law of stress time, t^{α}, with the exponent about 0.4. The power law likely corresponds to the interface or near interface oxide trap creation.[16] It should be pointed out that the generation kinetics is independent of the sensing voltage $V_{\rm g}$ at which the current is measured. Similar power exponents at different $V_{\rm g}$ mean that $N_{\rm it}$ generation at different energy levels follows almost the same rate.

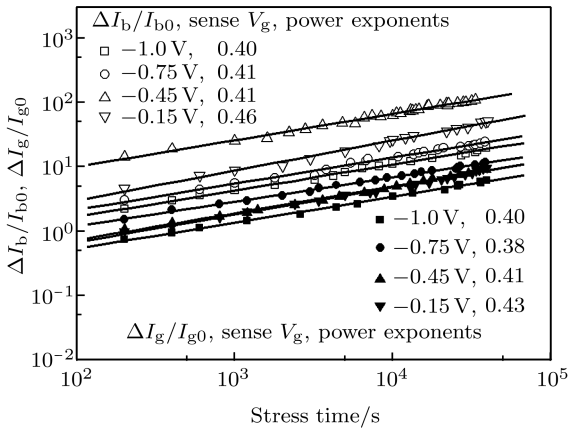


Fig.5. The relative $\Delta I_{\rm b}$ and $\Delta I_{\rm g}$ evolutions at different sensing voltage $V_{\rm g}$. A power law is found with a similar exponent.

On the other hand, $D_{\rm it}$ can be calculated by differentiating $N_{\rm it}(V_{\rm g})$ with respect to $V_{\rm g}$ at any stress time, of which the result is shown in Fig.6. A peak is found at the upper half of the silicon bandgap with $E - E_{\rm i} = 0.3$–$0.4\,{\rm eV}$, where $E_{\rm i}$ is the silicon intrinsic Fermi level. The results are similar to those given in Ref.[10] in which a peak appeared at $E - E_{\rm i} = 0.2\,{\rm eV}$, and we believe that the difference is due to the properties of samples, such as structure, and technology.

It is noted that only the relative $\Delta N_{\rm it}$ and $D_{\rm it}$ are obtained up to now, an accurate $I_{\rm b}$ formula is needed for obtaining the absolute values.

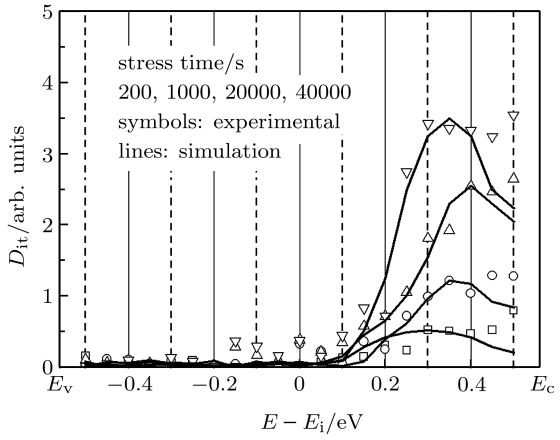


Fig.6. The energy profiles of interface states, $D_{\rm it}(E)$ at different stress times.

As mentioned above, for short channel n-MOSFETs at $V_{\rm FB} < V_{\rm g} < 0$, $I_{\rm s/d}$ cannot be ignored, $I_{\rm g} = I_{\rm s} + I_{\rm d} + I_{\rm b}$. The value of $I_{\rm s/d}$ is independent of channel $N_{\rm it}$ and changes little before breakdown (as shown in Fig.1(b)). So we have

$$\begin{aligned}\Delta I_{\rm g} &= I_{\rm g} - I_{\rm g0} = \Delta I_{\rm b} = A_{\rm c} P_{\rm T}(N_{\rm it} - N_{\rm it0}) \\ &= A_{\rm c} P_{\rm T} \Delta N_{\rm it}, \end{aligned} \tag{4}$$

$$\begin{aligned}\Delta I_{\rm g}/I_{\rm g0} &= A_{\rm c} P_{\rm T} \Delta N_{\rm it}/(A_{\rm c} P_{\rm T} N_{\rm it0} + I_{\rm d0} + I_{\rm s0}) \\ &= \Delta N_{\rm it}/(a + N_{\rm it0}), \\ a &= (I_{\rm s0} + I_{\rm d0})/A_{\rm c} P_{\rm T}. \end{aligned} \tag{5}$$

As we have $\Delta N_{\rm it} \sim t^{\alpha}$, in the log–log figure, Eqs.(3) and (5) have the similar power factor, but $\Delta I_{\rm g}/I_{\rm g0}$ is smaller than $\Delta I_{\rm b}/I_{\rm b0}$, meaning that LVSILC underestimates $N_{\rm it}$ generation. The results are compared in Fig.5, which gives smaller variations but a similar slope.

Figure 7(a) is the GD current evolution during stress versus the gate bias. The peak current is proportional to $N_{\rm it}$ in each region.[17] Under a uniform stress, the channel $N_{\rm it}$ dominates.[18] Figure 7(b) shows the channel $N_{\rm it}$ generation variation with GD peak current. A power law with $\alpha = 0.42$ means the same kinetics as obtained for $\Delta I_{\rm b}$. The GD current peaks around $V_{\rm g} = 0$ in Fig.7(a) show the maximal recombination current through the channel interface states and the calculated $N_{\rm it}$ is an average value. But the $\Delta I_{\rm b}/I_{\rm b0}$ peaks in Fig.4 give the local $N_{\rm it}$ increment and the locations where interface states generate easily. One can find that the values at different sensing voltages are different, which means the different generating rates at the silicon bandgap. So in Fig.7(b) the difference between $\Delta I_{\rm b}/I_{\rm b0}$ and $\Delta I_{\rm GD}/I_{\rm GD0}$ should result from the fact that the former one is the local result and the latter is the average value.

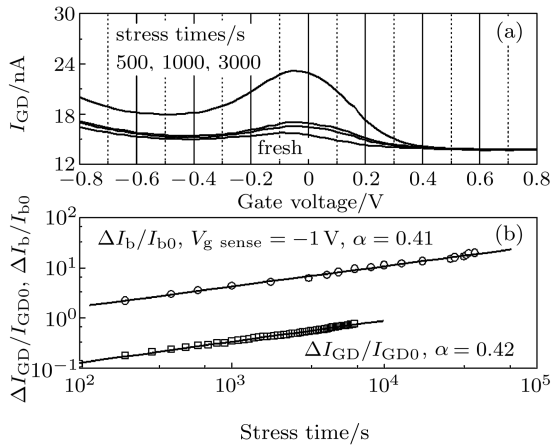


Fig.7. Variation of GD current with $V_{\rm g}$ (a) and the comparison between $\Delta I_{\rm b}/I_{\rm b0}$ and $\Delta I_{\rm GD}/I_{\rm GD0}$ (b).

The new method avoids the effect of $I_{\rm s/d}$ when taking $I_{\rm b}$ as a monitor of $N_{\rm it}$ generation. The interface states-assisted tunnelling current is the main ingredient of $I_{\rm b}$ at $V_{\rm FB} < V_{\rm g} < 0$. Unlike the CP and DCIV methods, of which signal currents are determined by recombination process, $I_{\rm b}$ is limited by the tunnelling process. The relative $\Delta N_{\rm it}$ is obtained only by measuring the I–V curves. However, the low voltage current mechanism would change when the oxide breakdown forms the percolation conduction paths, and then $I_{\rm b}$ will not be taken as the monitor of $N_{\rm it}$.

5. Conclusions

A monitor of $N_{\rm it}$ generation for small dimension n-MOSFETs under a uniform stress has been developed. It is found that the low voltage stress-induced $I_{\rm b}$ is sensitive to both the density of interface states and its energy distribution, and the LVSILC method underestimates the amount of $N_{\rm it}$ generation. The low voltage substrate current comes from interface trap-assisted-tunnelling process. By investigating $\Delta I_{\rm b}/I_{\rm b0}$ variation with stress time and gate voltage, $\Delta N_{\rm it}/N_{\rm it0}$ and $D_{\rm it}$ evolutions are obtained. The results are compared with that measured by GD technique.

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References

[1] DiMaria D J 1990 *J. Appl. Phys.* **68** 5234
[2] Liu H X, Hao Y, Hawkins I D and Peaker A R 2005 *Chin. Phys.* **14** 1644
[3] Ren H X and Hao Y 2001 *Chin. Phys.* **10** 189
[4] Li Z H, Liu H X and Hao Y 2006 *Chin. Phys.* **15** 833
[5] Liu H X, Zheng X F and Hao Y 2005 *Acta Phys. Sin.* **54** 1373 (in Chinese)
[6] Nicollian E H and Brews J R 1981 *MOS Physics and Technology* (Canada: Wiley)
[7] Brugler J S and Jespers P G 1969 *IEEE Trans. Electron Devices* **16** 297
[8] Masson P, Autran J L and Brini J 1999 *IEEE Eletron Device Lett.* **20** 92
[9] Neugroschel A, Sah C T, Han K M, Carroll M S, Nishida T, Kavalieros J T and Lu Y 1995 *IEEE Trans. Electron Devices* **42** 1657
[10] Andrea G, Sangiorgi E, Bude J, Sorsch T W and Weber G 2000 *IEEE Trans. Electron Devices* **47** 2358
[11] Nicollian P E, Rodder M, Grider D T, Chen P, Wallace R M and Hattangady S V 1999 *IEEE International Reliability Physics Symposium Proceedings* p400
[12] Bauza D, Rahmounce F, Laqli R and Ghibaudo G 2005 *Microelectron. Reliab.* **45** 849
[13] Lime F, Ghibaudo G and Guegan G 2001 *Microelectron. Reliab.* **41** 1421
[14] Zhao Y, Xu M Z and Tan C H 2006 *Chin. J. Semicond.* **27** 1264
[15] Lee W C and Hu C 2000 *Symposium on VLSl Technology* Digest of Technical Papers p198
[16] DiMaria D J and Cartier E 1995 *J. Appl. Phys.* **78** 3883
[17] Cai F and Sah C T 2000 *IEEE Trans. Electron Devices* **47** 576
[18] Schuegraf K F and Hu C 1994 *IEEE Trans. Electron Devices* **41** 761