Vol 16 No 10, October 2007
1009-1963/2007/16(10)/3114-06
Chinese Physics
© 2007 Chin. Phys. Soc.
and IOP Publishing Ltd

Comparison of hot-hole injections in ultrashort channel LDD nMOSFETs with ultrathin oxide under an alternating stress*

Chen Hai-Feng(陈海峰)†, Hao Yue(郝 跃), Ma Xiao-Hua(马晓华), Cao Yan-Rong(曹艳荣), Gao Zhi-Yuan(高志远), and Gong Xin(龚 欣)

School of Microelectronics, Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an 710071, China

(Received 22 November 2006; revised manuscript received 8 February 2007)

The behaviours of three types of hot-hole injections in ultrashort channel lightly doped drain (LDD) nMOSFETs with ultrathin oxide under an alternating stress have been compared. The three types of hot-hole injections, i.e. low gate voltage hot hole injection (LGVHHI), gate-induced drain leakage induced hot-hole injection (GIDLIHHI) and substrate hot-hole injection (SHHI), have different influences on the devices damaged already by the previous hot electron injection (HEI) because of the different locations of trapping holes and interface states induced by the three types of injections, i.e. three types of stresses. Experimental results show that GIDLIHHI and LGVHHI cannot recover the degradation of electron trapping, but SHHI can. Although SHHI can recover the device's performance, the recovery is slight and reaches saturation quickly, which is suggested here to be attributed to the fact that trapped holes are too few and the equilibrium is reached between the trapping and releasing of holes which can be set up quickly in the ultrathin oxide.

Keywords: lightly doped drain, hot hole injection, gate-induced drain leakage, trapping
PACC: 7340Q, 7340, 7360H

1. Introduction

As the MOSFET technology migrates into the ultra-deep submicron domain, the hot carrier effect has aroused great research interest because of its importance in device and circuit reliability.[1,2] The hot carrier effect induces the gate oxide damages including the oxide-trapped charge and interface state at the Si–SiO_2 interface.[3,4] As the gate oxides are continuously being scaled down, positive charges formed near the interface will become more important.[5] Several studies have been performed on the hot-hole injection (HHI) mechanisms for nMOSFETs.[6−12]

There are basically three different stressed conditions for HHI, i.e, low gate voltage HHI (LGVHHI),[6−9] gate-induced drain leakage induced HHI (GIDLIHHI),[10−12] and substrate HHI (SHHI). These studies of HHI have mainly focused on conventional nMOSFETs. However, there has been little attention paid to the investigation of the HHI in lightly doped drain (LDD) nMOSFETs so far, especially in ultrashort gate LDD nMOSFETs with ultrathin gate oxides, even though scaling LDD MOSFETs have gained widespread use in integrate circuits.

LDD MOSFET exhibits additional high lateral field peaks on the drain, thus aggravating hot-carrier injection and degradation problems,[13] and these peaks are related to avalanches and hot-carrier phenomena and increase with decreasing gate length and oxide thickness.[13] The LGVHHI resulting from impact-ionization and GIDLIHHI are both very closely related to the lateral electric field, and then the degradation phenomena of the two types of HHIs have changed much as the LDD nMOSFETs are scaled down. In addition, the mechanism of SHHI in the ultrathin gate oxide is also different from that in thick gate oxide. Therefore the insight into their mechanisms is necessary step toward a more complete understanding of HHI degradation phenomena in ultrashort gate LDD nMOSFETs with ultrathin gate oxide.

Distinguished from the previous work on HHIs,[6−12] this paper investigates three types of HHIs in the ultrashort gate (0.1 μm) LDD nMOSFETs with ultrathin gate oxide (1.4 nm). Through comparing the recoveries of devices damaged by different types of

*Project supported by the National Natural Science Foundation of China (Grant No 60376024).
†E-mail: heellor@163.com

HHIs, the characteristics of the three types of HHIs in the ultrashort gate LDD nMOSFETs with ultrathin gate oxides are dealt with. It is found that not all of HHIs can recover performances of hot-electron-damaged LDD nMOSFETs, and they were divided into two types in this paper based on these differences among the three types of HHIs. Furthermore, a new recovery mechanism of SHHI in ultrathin oxide is proposed. In addition, all of the relevant mechanisms are also presented in detail.

2. Devices and experiments

The devices used in this study were LDD nMOSFET with n^+ poly-Si gate fabricated by 90 nm complementary metal oxide semiconductor (CMOS) technology. The physical thickness (T_{ox}) of the gate oxide was 1.4 nm with decoupled-plasma-nitridation (DPN) treatment. The gate length (L) was 0.1 μm and gate width (W) 10 μm. The effective channel length (L_{eff}) was 75 nm. V_{th} was defined as the gate voltage for a drain current of 0.1 μA*W/L with $V_d = 0.05$ V, and V_{th} was 0.25 V.

Three types of HHIs were applied to the devices after HEI was performed on the devices. Four devices A, B, C and D which had the same geometric structures were utilized in this paper in order to compare the three types of HHIs. They were all applied to the HEI ($V_g = V_d = 2.0$ V) during period 1. Then during period 2 LGVHHI ($V_g = V_{th} = 0.25$ V, $V_d = 2.2$ V) was applied to device A, GIDLIHHI ($V_g = -2.2$ V, $V_d = 2.2$ V) was applied to device B, SHHI ($V_g = -2.5$ V) was applied to the device D. Other terminals were well grounded during the stresses above. Every period was 500 seconds. The HEI ($V_g = V_d = 2.0$ V) was always applied to Device C in the whole stress process for comparison.

During the comparison, the degradations of various device parameters such as threshold voltage V_{th}, linear maximum transconductance G_{max}, linear drain current I_{dlin}, and saturation drain current I_{dsat} were characterized as a function of stress time under the alternating stress. The roles of the hot holes in the devices degradation were clarified by investigating the relation among G_{max} degradation, V_{th} degradation, and the drain current degradation.

Both the source and the substrate were grounded during measurements. All stresses and measurements were performed by using HP4156B semiconductor parameter analyser at room temperature. In addition, Sivaco software was used to simulate the electric field under the stress condition.

3. Results and discussion

3.1. Experimental degradation characteristics

Figure 1 shows the V_{th} degradation as a function of stress time. Here the V_{th} shift is plotted for different alternating stress conditions. Electrons are injected into the devices during the first period for 500 s, followed by hole injection (period 2) for 500 s. Notice that the V_{th} degradations of devices A, B and D increase with stress time during period 1. During period 2 the shifts in V_{th} for devices A, B and D appear distinctly in different situations due to different types of HHIs. It is seen that the V_{th} degradations of devices A and B do not recover though holes are injected into the devices. On the contrary, the V_{th} degradation rates become enhanced as shown in Fig.1. Notice also that after SHHI (device D), the V_{th} degradation recovers, but the recovery quickly enters into a saturation region.

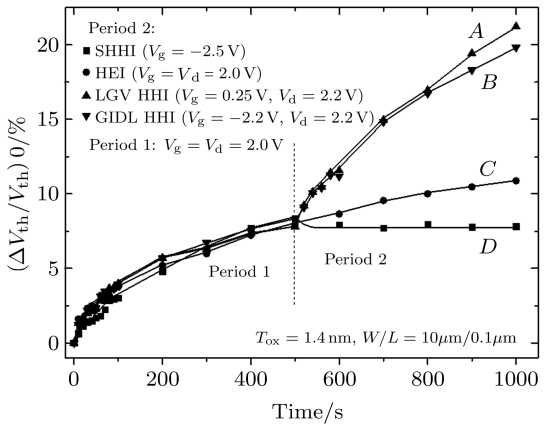


Fig.1. V_{th} degradation as a function of stress time measured under alternating stress conditions: 500 s, period 1 (HEI); 500 s, period 2 (HHI).

G_{max}, which is a measure of the ability of gate controlling the channel, is another important parameter in MOSFETs. The shift in G_{max} is plotted for alternating stress conditions in Fig.2. After 500 s HEI in period 1, the shifts in G_{max} for all devices become negative and their absolute values become larger as

the stress time increases. However, degradations in G_{max} are different for the devices A, B and D in the period 2. It can be seen that the degradations in devices A and B during period 2 become large in comparison with that of device C, but the degradation in device D recovers. Namely, LGVHHI and GIDLI-HHI weaken the ability of gate controlling the channel current further, while SHHI meliorates this ability.

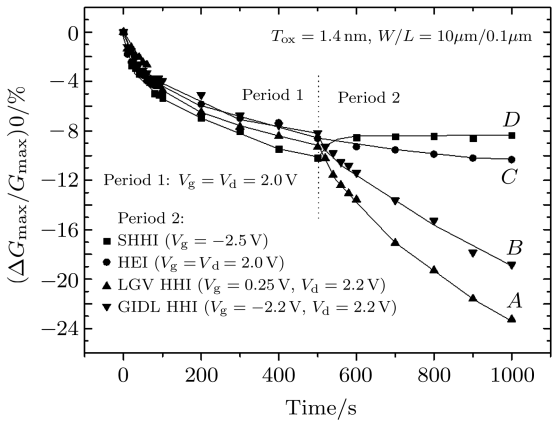


Fig.2. G_{max} degradation as a function of stress time measured under alternating stress conditions: 500 s, period 1 (HEI); 500 s, period 2 (HHI).

The other two corresponding parameters, I_{dlin} and I_{dsat} degradations of devices A, B, C and D for alternating stress conditions are shown in Figs.3 and 4, respectively. The situations for I_{dlin} and I_{dsat} degradations are similar to that for the G_{max} degradation in Fig.2. It can be also seen that the degradations in devices A and B during period 2 become large as compared with that of device C, but the degradation in device D recovers.

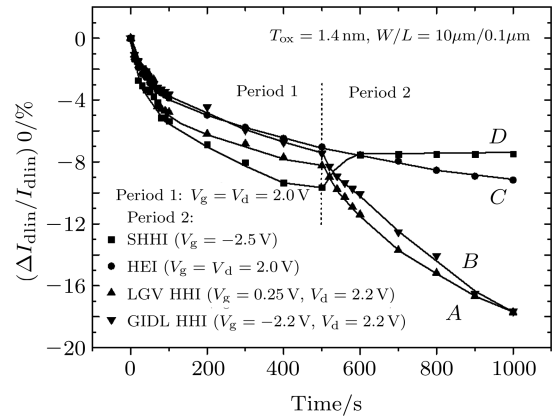


Fig.3. I_{dlin} degradation as a function of stress time measured under alternating stress conditions: 500 s, period 1 (HEI); 500 s, Period 2 (HHI).

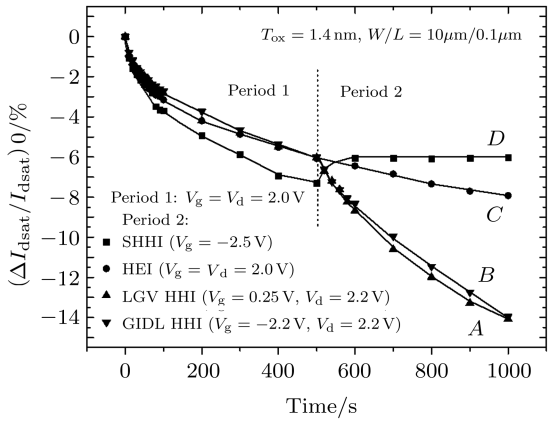


Fig.4. I_{dsat} degradation as a function of stress time measured under alternating stress conditions: 500 s, period 1 (HEI); 500 s, period 2 (HHI).

3.2. Mechanisms of degradation

3.2.1. Period 1: HEI

Figure 5 shows the lateral electric field under three stresses along with the channel. Notice that the maximum lateral electric field under $V_g = V_d = 2.0$ V lies in the LDD region. Since the impact-ionization site is closely related to the lateral electric-field, the maximum impact ionization occurs at the position where the peak lateral electric field lies. So the hot electrons produced by the impact-ionization are injected into the interface around LDD region, accompanied with creating interface states. The process is illustrated in Fig.6(a). In very short channel devices, the degradation is primarily due to the generation of interface state for the bias $V_g = V_d$.[14] Thus, electrons injecting into interface lead to an increase in parasitic

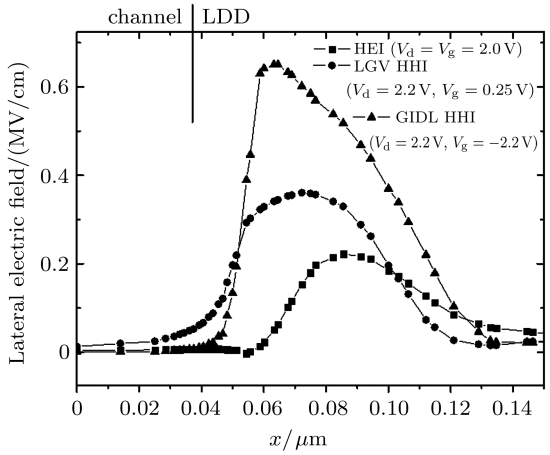


Fig.5. Lateral electric fields in the HEI, GIDL HHI, and LGV HHI, simulated by Sivaco software for LDD-nMOSFET(T_{ox} = 1.4 nm, L = 0.1 μm, L_{eff} = 75 nm).

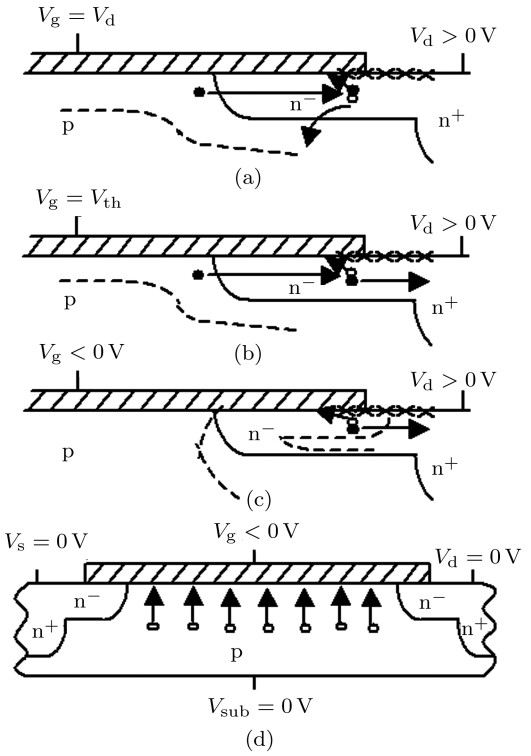


Fig.6. Illustrations of hot-carrier injection in LDD-nMOSFET under stress conditions: (a) HEI. (b) LGVHHI, (c) GIDLHHI and (d) SHHI. The open symbol represents hot holes and the solid circle represents hot electrons generated in the hot-carrier injection. × denotes created interface states.

LDD resistance[15] and a reduction in carrier mobility. Interface states increase with increasing stress time. Because transconductance decreases when the defect density increases,[16] G_{max} degradation becomes severe with increasing the stress time as shown in Fig.2. In addition, the resistance in LDD region and the reduction in the carrier mobility increase with stress time. Consequently, the drain current I_d (I_{dlin} & I_{dsat}) and G_{max} decrease as shown in Figs.2–4 during period 1. Since we use the constant current V_{th} extraction method, the V_{th} increases as shown in Fig.1 during period 1.

3.2.2. Period 2 in device *A*: LGV HHI

For the case of LGVHHI($V_g = V_{th} = 0.25\,V$ and $V_d = 2.2\,V$), the lateral electric field is shown in Fig.5. Similar to HEI stress, the hot holes from impact–ionization generation of electron-hole pairs by the channel hot electrons are injected into the interface around the LDD region with the help of the drain-to-gate voltage V_{dg}. The process is illustrated in Fig.6(b). In Refs.[7,9], it is shown that the V_{th} of nMOSFET increases after HEI, and the following LGVHHI injects positive charges accompanied with the masking of the interface traps, causing V_{th} to drop off correspondingly, which is contrary to the results of our experiments. This is because in our experiments these holes are injected into interface above the LDD region, though part of them neutralize the electron-charging traps created during period 1 in this region, they cannot shorten the channel to mask the influence of interface states like conventional nMOSFET. In addition, although the holes can be trapped in the oxide around the interface above the LDD region, their number is very small because they are very difficult to exist in the ultrathin gate oxide. Consequently, the effect of these few trapped holes on compensating the interface-states-induced increase in LDD resistance is little, which makes the interface-states-induced increase in LDD resistance dominate the damage process. At the same time, these hot-holes create many neutral-electron traps[17] at the interface. So as the stress time increases, the created interface states and neutralized traps do increase, which leads to the decrease in drain current. Because the ultrathin device degradation is mainly attributed to the LDD resistance, the degradation due to previous HEI cannot be recovered. Therefore, the V_{th} degradation becomes large continuously, and G_{max}, I_{dlin} and I_{dsat} degradations become large as shown in Figs.1–4.

3.2.3. Period 2 in device *B*: GIDLIHHI

In the case of GIDLIHHI, a negative voltage is applied to the gate and a positive voltage is applied to the drain. Under this condition, the gate-induced drain leakage (GIDL) current is formed due to the band-to-band tunnelling. Therefore, some holes created from band-to-band tunnelling in the deep-deletion region of the drain can be injected into the gate oxide in the overlap region as shown in Fig.6(c). The hole injection generates a lot of interface states and neutral-electron traps on interface in an overlap region. A simple qualitative model can be used to account for hot-hole injection effects on a device under a GIDL stress[10,12]

$$Q_T \propto Q_0 p(l) = Q_0 \exp(l), \tag{1}$$

$$l = -\frac{\Phi_B}{q\lambda_H E_M}, \tag{2}$$

where $p(l)$ is the probability that a hole travels a sufficient distance l to gain an energy Φ_B which is the

barrier energy at Si–SiO_2 interface without a collision. Q_0 is the total charge quantity created from GIDL. The number of injected holes is proportional to the created charges multiplied by $p(l)$. λ_H is the mean free path for holes, and Q_T is the charge quantity of holes trapped in the gate oxide due to B–B tunnelling. Here, E_M is the maximum lateral electric field.

The lateral electric field under the GIDL condition is shown in Fig.5. Because these holes created interface states and neutral-electron traps are also located in the interface above the LDD region, these holes play the same role as the hot holes under the LGVHHI stress. They cannot recover the device degradation resulting from the electrons previously injected into the overlap region. Moreover, they enhance the device degradation as shown in Figs.1–4.

3.2.4. Period 2 in device D: SHHI

SHHI provides uniform (rather than localized) hot holes in device. As shown in Fig.6(d), the holes are forced to be injected into the oxides above the channel by the vertical electric field under the SHHI condition. Figure 7 shows a schematic band diagram of behaviours of hot holes during SHHI. It is seen that the hot holes coming from the substrate are divided into three parts when they achieve the interface. One part of holes with enough energy (which are called 'luck-holes') surmount the barrier to arrive at the gate. Some part of holes directly tunnel into the oxide. The remaining part of holes are trapped in the interface states.

When carriers are trapped uniformly in the gate oxide, the trapped charge quantity Q_T can be described by[18] $Q_T \propto T_{ox}$. Because the gate oxides in the devices are only 1.4 nm thick, most of holes tunnel or surmount barrier to arrive at the gate, while very few holes can be trapped in the oxide (process ①). However the trapped holes are easy to release from the traps by tunnelling because of the ultra thin oxide (process ②). There can be reached an equilibrium between the trapping and releasing of holes in the ultra-thin oxide.

These trapped holes in the oxide above the channel lead V_{th} to decrease and make G_{max}, drain current large. Therefore, these holes compensate the degradation induced by the electron trapping in the LDD region under the HEI stress. Consequently, V_{th} shifts negatively after the SHHI and G_{max}, I_{dlin} and I_{dsat} have recovered.

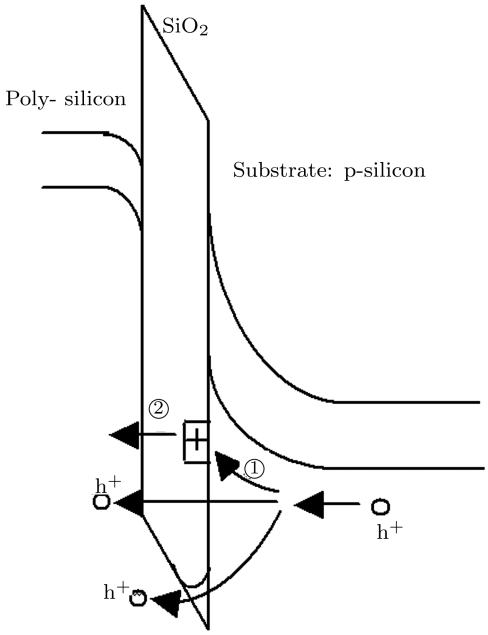


Fig.7. Schematic band diagram showing behaviours of hot holes during SHHI. ① is trapping process while ② is the release process for holes.

As the SHHI stress time increases, the recovery reaches the saturation quickly. This is because the equilibrium between the trapping and releasing of holes in the ultra-thin oxide are reached quickly and the number of trapped holes keeps almost constant. Therefore, the recovery due to SHHI after 100 s does not increase as shown in Figs.1–4. Meanwhile, bear in mind that the trapped holes are very few in the 1.4 nm thick gate oxide, which is mentioned above, though the substrate-to–gate V_{bg} is very large ($V_b - V_g = 2.5$ V). Few trapped holes result in a small compensation of electron trapping, and accordingly the recovery of degradation is small.

Based on the mechanisms mentioned above, we can explain the differences among the three HHI–induced degradation slopes in period 2 in Figs.1–4 as follows: trapped holes created during SHHI (applied on device D) in the oxide above the channel lead V_{th} to decrease and make G_{max}, drain current large. Therefore, these holes compensate the degradation induced by the electrons trapping in the LDD region under the HEI stress. Thus V_{th} shifts negatively after the SHHI and G_{max}, I_{dlin} and I_{dsat} have recovered. On the contrary, LGVHHI (applied to device A) and GIDLIHHI (applied to device B) cannot recover the device degradation resulting from the trapping electrons previously in the LDD region because these trapped holes during LGVHHI and GIDLIHHI

are also located in the interface above the LDD region. Moreover, they enhance the device degradation slopes due to the additional hot-hole-induced interface states in Figs.1–4. So during the period 2, compared with the device C, the absolute values of degradation slopes of the devices A and B are large and that of device D is small. Although the absolute value of degradation slope of device A is larger than that of device B, this difference between their degradation slopes just indicates that the degradation extents are different due to different stress conditions.

4. Conclusion

This paper discusses the behaviours of three types of hot-hole injections under an alternating stress in ultrashort channel LDD nMOSFET with ultrathin oxide, i.e. LGVHHI, GIDLIHHI, SHHI. On account of the different locations of hot-holes-created damages and their different influences on recovering the degradation induced by HEI, they can be divided into the following two types:

1) holes created in the HHI are located at the interface in the LDD region, i.e. LGVHHI and GIDLIHHI;

2) holes created in the HHI are located at the interface in the channel region, i.e. SHHI.

For LGV and GIDLIHHI it is found that they cannot recover the device degradations induced previously by the HEI ($V_{\rm g} = V_{\rm d}$) in the alternating process. On the contrary, they still make the device degenerate continuously. However, the trapped holes generated in the SHHI are located on the interface of the channel and they compensate the degradation resulting from the increase in LDD resistance and the reduction in carrier mobility during the HEI. So after SHHI, the device degradation can be recovered. But this recovery is small and the saturation is reached quickly due to the ultrathin gate oxide.

References

[1] Chen J H, Wong S C and Wang Y H 2001 *IEEE Trans. Electron Devices* **l48** 2746

[2] Ma X H, Hao Y, Wang J P, Cao Y R and Chen H F 2006 *Chin. Phys.* **15** 2742

[3] Cheng S M, Yih C M, Yeh J C, Kuo S N and Chung S S 1997 *IEEE Trans. Electron Devices* **44** 1908

[4] Liu H X, Hao Y, Hawkins I D and Peaker A R 2005 *Chin. Phys.* **14** 1644

[5] Zhang J F, Zhao C Z, Chen A H, Groeseneken G and Degraeve R 2004 *IEEE Trans. Electron Devices* **51** 1267

[6] Han K M and Sah C T 1998 *IEEE Trans. Electron Devices* **45** 1624

[7] Heremans P, Bellens R, Groesenken G and Maes H E 1988 *IEEE Trans. Electron Devices* **35** 2194

[8] Ang D S 2001 *IEEE Electron Device Letters* **22** 553

[9] Bellens R, Heremans P, Groesendken G and Maes H E 1988 *IEEE Electron Device Letters* **9** 232

[10] Ma Z J, Lai P T and Cheng Y C 1993 *IEEE Trans. Electron Devices* **40** 125

[11] Kim Y P, Kim S T, Moon J T and Kim S U 2001 *IEEE Transaction on Device and Materials Reliability* **1** 104

[12] Igura Y, Matsuoka H and Takeda E 1989 *IEEE Electron Device Letters* **10** 227

[13] Orlowski M K, Werner C and Klink J P 1989 *IEEE Trans. Electron Devices* **36** 375

[14] Li E, Rosenbaum E, Tao J, Yeap G C, Lin M R and Fang P 1999 *IEEE 99CH*36296. 37th *Annual International Reliability Physics Symposium* 253

[15] Yih C M, Wang C L, Chung S S, Wu C C, Tan W, Wu H J, PI S and G D H 1998 *Jpn. J. Appl. Phys.* **37** 1035

[16] Bouhdada A and Marrakh 2002 *Proc.* 23rd *International Conference on Microelectronics* **2** 471

[17] Doyle B S, Bourcerie M, Bergonzoni C, Benecchi R, Bravis A, Mistry K R and Boudou A 1990 *IEEE Trans. Electron Devices* **37** 1869

[18] Takeda E, Yang C Y and Hamada A M 1995 *Hot-Carrier Effects in MOS Devices* (San Diego: Academic) p138