Vol 16 No 1, January 2007
1009-1963/2007/16(01)/0240-05

Chinese Physics

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Schottky barrier MOSFET structure with silicide source/drain on buried metal*

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(Received 10 April 2006; revised manuscript received 22 May 2006)

In this paper, we propose a novel Schottky barrier MOSFET structure, in which the silicide source/drain is designed on the buried metal (SSDOM). The source/drain region consists of two layers of silicide materials. Two Schottky barriers are formed between the silicide layers and the silicon channel. In the device design, the top barrier is lower and the bottom is higher. The lower top contact barrier is to provide higher on-state current, and the higher bottom contact barrier to reduce the off-state current. To achieve this, ErSi is proposed for the top silicide and $CoSi_2$ for the bottom in the n-channel case. The 50 nm n-channel SSDOM is thus simulated to analyse the performance of the SSDOM device. In the simulations, the top contact barrier is 0.2e V (for ErSi) and the bottom barrier is 0.6 eV (for $CoSi_2$). Compared with the corresponding conventional Schottky barrier MOSFET structures (CSB), the high on-state current of the SSDOM is maintained, and the off-state current is efficiently reduced. Thus, the high drive ability (1.2 mA/μm at $V_{ds} = 1$ V, $V_{gs} = 2$ V) and the high I_{on}/I_{min} ratio (10^6) are both achieved by applying the SSDOM structure.

Keywords: Schottky barrier MOSFET, Schottky barrier, barrier height, silicide source/drain
PACC: 7330, 7340Q

1. Introduction

As the feature size of the metal-oxide-semiconductor field-effect-transistor (MOSFET) has been scaled down to several deca-nanometres, CMOS technologies face many challenges, such as the gate engineering, the source/drain issues and the short channel effect (SCE), etc.[1−3] The source/drain issues are involved with heavy doping, ultra-shallow junction, steep doping profile and low source/drain serial resistance. It is urgent to find a solution for technology nodes of 45 nm and beyond. Recently, the Schottky barrier source/drain MOSFET structure (SB-MOSFET) is proposed as an effective alternative to the conventional doped source/drain structures.

In 1999, Wang *et al* reported the experiments on 40 nm p-type SB-MOSFETs.[4] In the next year, Kedzierski *et al* further proposed 20 nm thin-body SB-MOSFET.[5] For the SB-MOSFETs, the silicons at the source/drain regions are silicided, and the source/drain doping and annealing processes are no longer needed. Without the high temperature processes, new materials, such as the metal gate and high-k dielectric stacks, can be feasibly employed for the future SB-MOSFET structures.[6,7] The germanide materials have also been studied for the future applications.[8,9] With the source/drain silicided rather than doped, the SB-MOSFET can feasibly be provided with ultra-shallow metallic source/drain and relatively low serial resistance, thus, can be made immune to the short channel effect effectively. According to the International Technology Roadmap for Semiconductors (ITRS'03),[10] the SB-MOSFET has been considered as a candidate for the future applicable structure.

In recent years, many researches have been worked out for the SB-MOSFETs. The theoretical and experimental studies have shown the Schottky barrier height at the source/drain has important impact on the device performance. It has been pointed out that the lower barrier materials (e.g. ErSi for n-channel and PtSi for p-channel) can help to increase the on-state current (I_{on}), and the mid-gap ones (e.g. $CoSi_2$ and NiSi) to decrease the off-state current (I_{off}). As a result, a tradeoff should be made between the lower I_{off} and the higher I_{on}. In addition, Saitoh *et al*[11] and Zhao *et al*[12] demonstrated the performance

*Project supported by the National Natural Science Foundation of China (Grant No 60506009).
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of SB-MOSFET could be optimized with silicon on insulator (SOI) substrate. It is found that I_{on} mainly is provided at the source contact in the region that is several nanometres below the gate oxide. The analytical work by Knoch and Appenzeller[13] proposed to use 10 nm ultra-thin body (UTB) substrate to improve the I_{on}/I_{off} ratio. However, while the silicon body thickness is thinned down to several nanometres, other parameters, such as the threshold voltage, will become sensitive to the thickness variation.[14] And the requirement of the UTB thickness uniformity is also rigorous for the real applications.

In this paper, we propose a novel SB-MOSFET structure with source/drain silicide on buried metal (SSDOM). The SSDOM can improve the drive performance and suppress the short channel effect more effectively. In the following sections, numerical simulations are carried out to compare the performance of SSDOM with those of the conventional SB-MOSFETs (CSBs).

2. Device structure and working principle

The schematic cross-section of the SSDOM is shown in Fig.1(a). The source/drain region consists of two layers of silicide materials. The top silicide material forms the lower barrier with the silicon channel, and the bottom silicide forms the higher barrier. For n-channel device, ErSi is proposed for the top silicide, and $CoSi_2$ for the bottom. The lower top contact is designed to provide higher I_{on}, and the higher bottom contact is to reduce the I_{off}.

The two-dimensional simulations of the n-channel SSDOM are performed to study the working principle of the SSDOM. The structure parameters in the simulations are given in Table 1.

The gate length (L_g) is 50 nm, and the equivalent gate oxide (EOT) is 1 nm thick, according to the requirement in ITRS'03.[10] The silicon channel is p-type doped at the concentration of 10^{16} cm^{-3}. The gate material is polysilicon, and the corresponding work function is 0.54 eV. The barrier height of the top contact is 0.2 eV (for ErSi), and the bottom barrier is 0.6 eV (for $CoSi_2$). The top contact vertical width (d_{top}) is 5 nm, and the bottom contact width (d_{btm}) is 25 nm. The horizontal extents of the source/drain are both 50 nm, and the buried oxide thickness (d_{box}) is 200 nm.

Table 1. Simulation parameters of n-channel SSDOM.

Gate length (L_g)	50 nm
Gate dielectric stack (EOT)	1 nm
Channel doping (N_A)	10^{16}cm^{-3}
Gate work-function	0.54 eV
Spacer material	SiO_2
Top contact barrier	0.2 eV
Bottom contact barrier	0.6 eV
Thickness of the TSL (d_{top})	5 nm
Thickness of the BSL (d_{btm})[a]	25 nm
Source–Drain bias (V_{ds})[a]	1 V
Gate bias (V_{gs})	−0.5 to 2 V

[a] TSL and BSL are the short form of top and bottom silicide layer, respectively.

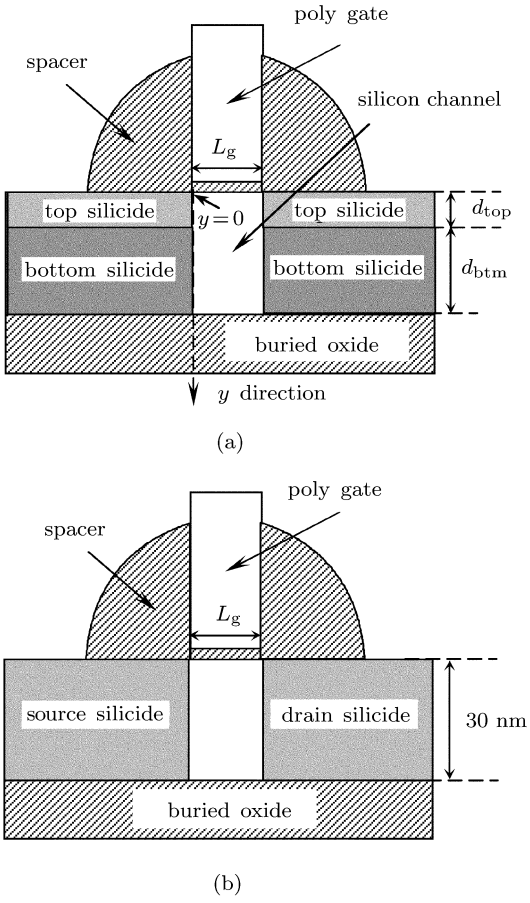


Fig.1. Schematic cross-section of: (a) the SSDOM, (b) the CSB. The source/drain region of SSDOM consists of two layers of silicide materials. The top silicide material (e.g. ErSi) forms the lower barrier with the silicon channel, and the bottom silicide (e.g. $CoSi_2$) forms the higher barrier.

The simulations are performed with the commercial simulator ISE/DESSIS.[15] The full-coupled and non-local tunnelling model[16] is self-consistently implemented in the simulator. The two major transport

mechanisms for the Schottky contacts, thermionic emission and barrier tunnelling, are considered in the device simulations. The tunnelling currents of the Schottky contacts are calculated based on the Wentzel–Kramers–Brillouin (WKB) approximation. The tunnelling probability $\Gamma_{\rm t}$, at the perpendicular distance r from the Schottky contact, can be described as[15]

$$\Gamma_{\rm t} = \exp\Big[-\frac{2}{\hbar}\int_0^r \sqrt{2m^*(E_{\rm c}(r') - E_{\rm c}(r))}{\rm d}r'\Big], \quad (1)$$

where $E_{\rm c}(r)$ is the band edge at the location r and m^* the tunnelling mass. Thus, the tunnelling current density $J_{\rm t}$ at a range of r is:

$$J_{\rm t} = J_{\rm t,s-m} - J_{\rm t,m-s}\,, \quad (2)$$

here $J_{\rm t,s-m}$ is the tunnelling current from silicon to silicide and can be expressed as[16]

$$J_{\rm t,s-m} = A^*T^2\int_{\varepsilon}^{\infty} \Gamma_{\rm t}(r(\varepsilon')) \times \ln\Big[\frac{1}{1+\exp(\varepsilon'-\varepsilon_{\rm F}/k_{\rm B}T)}\Big]{\rm d}\varepsilon'\,, \quad (3)$$

where ε is the carrier energy at location r, $\varepsilon(r) = E_{\rm c}(r)$, and $\varepsilon_{\rm F}$ the quasi Fermi-level in the silicon, A^* the effective Richardson constant, and T the carrier temperature. And $J_{\rm t,m-s}$ is the tunnelling current from silicide to silicon and expressed as[16]

$$J_{\rm t,m-s} = A^*T^2\int_{\varepsilon}^{\infty} \Gamma_{\rm t}(r(\varepsilon')) \times \ln\Big[\frac{1}{1+\exp(\varepsilon'-\varepsilon_{\rm Fm}/k_{\rm B}T)}\Big]{\rm d}\varepsilon'\,, \quad (4)$$

here $\varepsilon_{\rm Fm}$ is the Fermi-level in the silicide.

The performances of the CSB are also simulated for comparison. The schematic structure of the CSB is shown in Fig.1(b). In the simulations, the source/drain barrier heights for the CSB are 0.2 eV and 0.6 eV respectively, and the contact vertical width is 30 nm. The other parameters are the same as those of SSDOM.

3. Results and discussions

Figure 2 shows the transfer characteristics of the SSDOM and those of the corresponding CSB. For the CSB, the device drivability can be enhanced by about four times by using the lower source/drain barrier ($I_{\rm on}$ = 1.4 mA/μm for the CSB with 0.2 eV source/drain barrier and 0.2mA/μm for the CSB with 0.6 eV source/drain barrier, at $V_{\rm ds}$ = 1 V, and $V_{\rm gs}$ = 2 V).

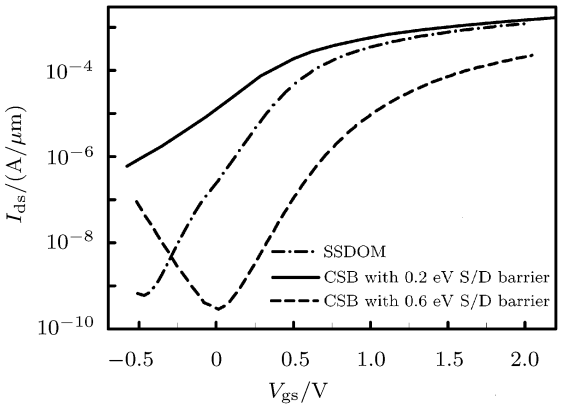


Fig.2. The transfer characteristics of the SSDOM and those of the CSB with the source/drain barrier heights of 0.2 eV and 0.6 eV respectively. The source–drain bias $V_{\rm ds}$ equals 1 V.

Furthermore, the leakage current of the CSB with 0.6 eV source/drain barrier can be reduced by five orders of magnitude compared with that of the CSB with 0.2 eV source/drain barrier ($I_{\rm off}$ = 0.2 nA/μm for the CSB with 0.6 eV source/drain barrier and 9 μA/μm for the CSB with 0.2 eV source/drain barrier, at $V_{\rm ds}$ = 1 V, and $V_{\rm gs}$ = 0 V). Thus, the lower barrier materials can be used for the high-performance application, and the mid-gap ones for low-operation-power case. Compared with the CSB, the SSDOM can maintain the benefits at both on-state and off-state. $I_{\rm on}$ of the SSDOM is almost the same as that of the CSB with 0.2 eV source/drain barrier (1.2 mA/μm for SSDOM and 1.4 mA/μm for CSB with 0.2 eV source/drain barrier, at $V_{\rm ds}$ = 1 V and $V_{\rm gs}$ = 2 V). In order to eliminate the influence of the threshold voltage, it is a better choice to study the minimum current $I_{\rm min}$ for the comparison of leakage currents. $I_{\rm min}$ of the SSDOM can be reduced to the same level as that of the CSB with 0.6 eV source/drain barrier ($I_{\rm min}$ = 0.7 nA/μm for SSDOM at $V_{\rm ds}$ = 1 V and $V_{\rm gs}$ = −0.4 V, and $I_{\rm min}$ = 0.2 nA/μm for the CSB with 0.6 eV source/drain barrier at $V_{\rm ds}$ = 1 V and $V_{\rm gs}$ = 0 V). As a result, the SSDOM can reach the highest $I_{\rm on}/I_{\rm min}$ ratio of 10^6.

For the explanation of the performance enhancement for the SSDOM, we analysed the on-state current density ($J_{\rm on}$) at $V_{\rm ds}$ = 1 V, $V_{\rm gs}$ = 2 V, and the off-state current density ($J_{\rm off}$) at $V_{\rm ds}$ = 1 V, $V_{\rm gs}$ = 0 V, along the source/channel interface from the top gate to the bottom oxide (shown as y-direction in Fig.1). The source/channel contact is divided into a number

of units, and the currents densities offered by each unit are calculated as nominal J_{on} and J_{off}. Then, the current density at $y = 0$ represents the current offered by the region of the source/channel contact that is just below the gate oxide, and that at $y = 30$ nm represents the current offered by the region just above the buried oxide.

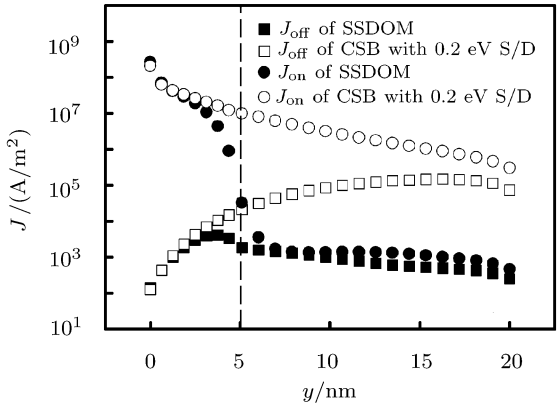


Fig.3. J_{on} (at $V_{ds} = 1$ V, $V_{gs} = 2$ V) and J_{off} (at $V_{ds} = 1$ V, $V_{gs} = 0$ V) along the source/channel interface (from top gate to bottom oxide), for the SSDOM and the CSB (0.2 eV source/drain barrier) respectively.

The simulation results of the SSDOM and the CSB with 0.2 eV source/drain barrier are shown in Fig.3. For the CSB, J_{on} decreases from $y = 0$ and becomes ten times lower at $y = 5$ nm ($J_{on} = 2\times10^8$ A/μm^2 at $y = 0$, and 10^7 A/μm^2 at $y = 5$ nm). As a result, the on-state current is mainly offered by the source/channel interfacial region, which is only 5 nm below the gate oxide. For the off-state, J_{off} increases from $y = 0$ and becomes nearly saturated (10^5 A/m^2) at $y = 10$ nm. This phenomenon can be explained with the drain-induced barrier tunnelling (DIBT) effect.[17,18] The electric field, which is penetrated from the drain, will make the source barrier thinner, and the barrier tunnelling current will increase even at $V_{gs} = 0$ V. For comparison, J_{on} of the SSDOM changes in the same way as that of the CSB with 0.2 eV source/drain barrier. The 5 nm top contact width is large enough to provide the main portion of the tunnelling current for the on-state. And the bottom contact can efficiently reduce J_{off}: J_{off} for SSDOM reaches the highest point (4×10^3 A/m^2) at $y = 3.75$ nm, and becomes lower than 2×10^3 A/m^2 for $y > 5$ nm. Then, I_{off} of the SSDOM can be expected to be two orders of magnitude lower than that of the CSB with 0.2 eV source/drain barrier.

In order to increase the device drive current, the studies of lower Schottky barrier materials were paid much attention. Tao *et al* reported to achieve 0.1 eV barrier height on n-type substrate by surface passivation with selenium.[19] The case of zero barrier height has also been studied for the future applications.[20,21] Here, the SSDOMs with the top contact barrier of 0 eV, 0.1 eV and 0.3 eV are simulated respectively. In the simulations, the bottom contact barrier is fixed at 0.6 eV and the device structure is the same as that in Fig.1(a). The simulated relations between the device performance and the top barrier height are shown in Fig.4. As the top contact barrier decreases from 0.3 eV to zero, I_{on} (at $V_{ds} = 1$ V, $V_{gs} = 2$ V) increases from 0.9 mA/μm to 1.5 mA/μm (nearly 60%). At the same time, I_{off} (at $V_{ds} = 1$ V, $V_{gs} = 0$ V) also increases from 0.03 μA/μm to 4 μA/μm (about 100 times). Then, the highest I_{on}/I_{off} ratio is achieved with 0.3 eV top barrier. As a result, the zero top barrier can be applied for the high performance application ($I_{on} = 1.5$ mA/μm at $V_{ds} = 1$ V, $V_{gs} = 2$ V), and the 0.3 eV top contact for low power ($I_{on}/I_{off} = 4 \times 10^3$) application respectively.

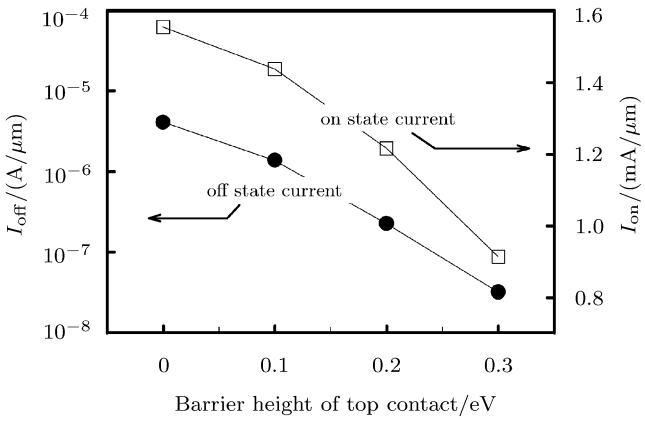


Fig.4. Dependence of I_{on} (at $V_{ds} = 1$ V, $V_{gs} = 2$ V) and I_{off} (at $V_{ds} = 1$ V, $V_{gs} = 0$ V) on the top contact barrier height. The barrier heights of the top contacts are 0, 0.1, 0.2 and 0.3 eV, and the bottom contact barrier is fixed as 0.6 eV.

Figure 5 shows the relationship between the top contact width d_{top} and the performance of the SSDOM. In the following simulations, the SOI thickness is fixed at 30 nm, then $d_{btm} = 30$ nm$-d_{top}$. It is shown in Fig.5 that d_{top} has made obvious impact on I_{off} (at $V_{ds} = 1$ V, $V_{gs} = 0$ V). I_{off} decreases about seven times at d_{top} is thinned down from 30 nm to 10 nm (from 8 μA/μm at $d_{top} = 30$ nm to 1.2 μA/μm at $d_{top} = 10$ nm). The decreasing of I_{off} becomes even faster as $d_{top} < 10$ nm (1.2 μA/μm at $d_{top} = 10$ nm to 0.1 μA/μm at $d_{top} = 3$ nm). As the bottom contact

width $d_{\rm btm}$ will increase at $d_{\rm top}$ decreases, the simulation results also demonstrate the bottom contact can efficiently reduce the leakage current.

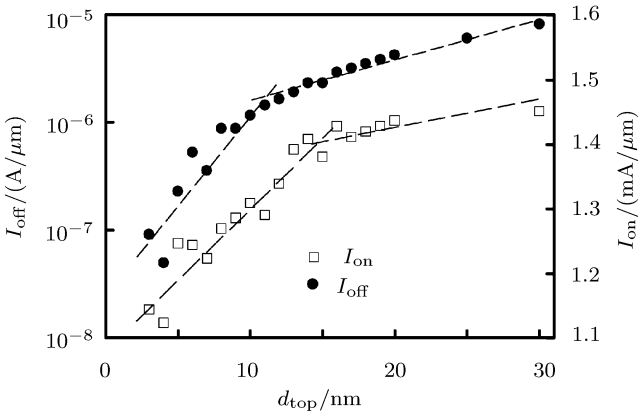


Fig.5. $I_{\rm on}$ (at $V_{\rm ds}$ = 1 V, $V_{\rm gs}$ = 2 V) and $I_{\rm off}$ (at $V_{\rm ds}$ = 1 V, $V_{\rm gs}$ = 0 V) of the SSDOM as functions of the top contact width $d_{\rm top}$ (the SOI thickness is fixed as 30 nm, and $d_{\rm top}$ range from 3 nm to 30 nm, then $d_{\rm btm} = 30\ {\rm nm} - d_{\rm top}$)

Moreover, $I_{\rm on}$ (at $V_{\rm ds} = 1$ V, $V_{\rm gs} = 2$ V) changes only by 4% while $d_{\rm top}$ varies from 30 nm to 15 nm (1.44 mA/μm at $d_{\rm top}$=30 nm, and 1.38 mA/μm at $d_{\rm top}$ = 15 nm). When $d_{\rm top}$ varies from 15 nm to 3 nm, $I_{\rm on}$ decreases faster (from 1.38 mA/μm at $d_{\rm top}$ = 15 nm to 1.14 mA/μm at $d_{\rm top}$ = 3 nm). The variation ratio of $I_{\rm on}$ is still less than 17%. Thus, decreasing $d_{\rm top}$ will contribute to the reduction of $I_{\rm off}$, while $I_{\rm on}$ is not much influenced.

4. Conclusions

In this paper, a novel SSDOM structure has been proposed for the nano-scale applications. The simulation results have shown that the SSDOM has a better performance than those of the CSB. The on-state current is almost the same as that of the CSB with 0.2 eV source/drain barrier. The off-state minimum current of the SSDOM can be reduced to the same level as that of the CSB with 0.6 eV source/drain barrier. The working mechanisms of the CSB and the SSDOM have been investigated by comparing the on-state current density and the off-state current density along the source/channel interface. The results show that the on-state current is mainly provided by the source/channel interfacial region, which is only 5 nm below the gate oxide. Also, the $J_{\rm off}$ increases from gate oxide/silicon channel interface, and becomes nearly saturated at y = 10 nm. Thus, the off-state current can be efficiently reduced by applying higher barrier for the bottom contact. The relation between the top contact width $d_{\rm top}$ and the performance of the SSDOM has also been studied. The device performance of the SSDOM can be enhanced by optimizing the top contact width.

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