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Electrical characteristics of MOS capacitor with HfTiON gate dielectric and HfTiSiON interlayer*

Chen Wei-Bing(陈卫兵)[a)†], Xu Jing-Ping(徐静平)[a)], Lai Pui-To(黎沛涛)[b)], Li Yan-Ping(李艳萍)[a)], Xu Sheng-Guo(许胜国)[a)], and Chan Chu-Lok(陈铸略)[b)]

[a)] *Department of Electronic Science & Technology, Huazhong University of Science and Technology, Wuhan* 430074, *China*

[b)] *Department of Electrical and Electronic Engineering, the University of Hong Kong, Pokfulam Road, Hong Kong*

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The paper reports that HfTiO dielectric is deposited by reactive co-sputtering of Hf and Ti targets in an Ar/O_2 ambience, followed by an annealing in different gas ambiences of N_2, NO and NH_3 at 600°C for 2 min. Capacitance–voltage and gate-leakage properties are characterized and compared. The results indicate that the NO-annealed sample exhibits the lowest interface-state and dielectric-charge densities and best device reliability. This is attributed to the fact that nitridation can create strong Si≡N bonds to passivate dangling Si bonds and replace strained Si–O bonds, thus the sample forms a hardened dielectric/Si interface with high reliability.

Keywords: metal-oxide-semiconductor capacitors, HfTiON, capacitance–voltage characteristics, leakage current, interlayer

PACC: 7300, 7340Q

1. Introduction

As metal-oxide-semiconductor field effect transistor (MOSFET) dimensions continue to scale into the sub-0.1-μm regime, reduction of SiO_2 thickness results in an increase of gate leakage current due to the direct tunnelling effect. From the viewpoints of power consumption and dielectric reliability, one solution for this problem is to replace SiO_2 with high-dielectric-constant (high-k) materials. Large gate capacitance can be obtained even for thicker films due to large k value, and so direct tunnelling of carriers can be effectively suppressed. Many materials included HfO_2,[1−10] ZrO_2,[11] HfSiO[12−14] and ZrSiO[14,15] have been intensively investigated as high-k gate dielectric to replace SiO_2. Recently, people placed interest onto a new high-k dielectric of HfTiO due to its good compatibility with Si, good thermal reliability and suitable k value.[16−18] So far, a lot of studies have been done on characteristics of the HfTiO material, including Ti content, micro- structure of materials and so on, but its interface properties with Si substrate were less involved.

In this study, HfTiO thin film is first deposited by reactive sputtering method and then annealed in different gases of N_2, NH_3 and NO to densify it (N_2 annealing) or transform it into HfTiON with a HfTiSiON interlayer (NO and NH_3 annealing). Measurement results show that the NO-annealed sample exhibits excellent interface and bulk properties, and low gate leakage due to formation of a HfTiSiON interlayer, which gives a SiON-like interface and thus low interface and near-interface trap densities. For the sake of clearly observing the interlayer and investigating its interface characteristics, a thicker film is deposited and a longer annealing time is used.

2. Experimental details

MOS capacitors were fabricated on (100)-oriented p-type Si substrate with a doping concentration of $8\times10^{15}\,cm^{-3}$. The wafers were cleaned by using the standard Radio Corporation of America (RCA) method followed by a 1-min dip in 5% hydrofluoric acid to remove the native oxide. HfTiO film was deposited by reactive radio frequency co-sputtering with 75-W and 35-W powers for Hf and Ti targets

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†E-mail: wbchen2006@gmail.com

respectively and a 133×20mPa pressure in 14.3% O_2 + 85.7% Ar ambience. The substrate temperature was 200°C. After deposition of the HfTiO film, rapid thermal annealing (RTA) was performed at 600°C for 2 min in N_2, NH_3 and NO ambiences respectively, denoted as the N_2, NH_3 and NO samples respectively. Finally, Al was thermally evaporated and patterned as the gate electrode of MOS capacitors with an area of $7.85\times10^{-5}\,cm^2$. The thickness of the as-deposited HfTiO film measured by ellipsometry was 16.7 nm.

High-frequency (HF, 1 MHz) capacitance–voltage (C–V) characteristics were measured at room temperature by using HP4284A precision inductance–capacitance–resistance (LCR) meter. Dielectric capacitance (hence dielectric thickness), flat-band voltage and dielectric-charge density were extracted from the HF C–V curve. Distribution of interface-state density was characterized by means of HF and quasi-static C–V method. High-field stress (7 MV/cm), with the capacitors biased in accumulation by HP 4156A precision semiconductor parameter analyser, was used to examine device reliability in terms of flat-band-voltage shift (ΔV_{fb}) and gate-leakage increase. All measurements were carried out under a light-tight and electrically-shielded condition.

3. Results and discussion

Figure 1 shows a transmission electron microscopy (TEM) image of the NO sample. Obviously a very flat interface between dielectric and Si is obtained, with the gate-dielectric thickness of ∼ 17.5 nm including an interlayer of ∼ 2 nm. The thickness is closely consistent with the result measured by ellipsometry. Increment of the thickness and formation of the interlayer should be attributed for a longer-time post-deposition annealing.

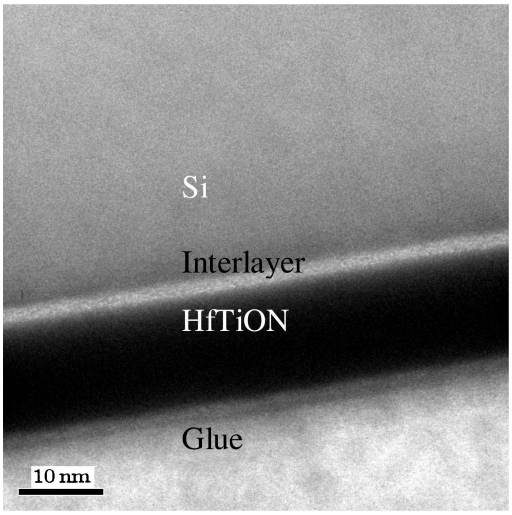


Fig.1. TEM image of the NO sample.

Figure 2 shows typical high-frequency C–V curves of the samples with various RTA conditions under dark condition at room temperature, scanned in both directions. The equivalent oxide thickness (EOT) and flat-band voltage V_{fb} extracted from the HF C–V curves are listed in Table 1. Figure 3 shows typical high-frequency and quasi-static C–V curves of the samples under dark condition at room temperature and interface-state density (D_{it}) extracted from them.[19] The interface-state density near midgap is the lowest with $4.58\times10^{11}\,cm^{-2}eV^{-1}$, $3.36\times10^{11}\,cm^{-2}eV^{-1}$ and $1.95\times10^{11}\,cm^{-2}eV^{-1}$ for N_2, NH_3 and NO sample respectively from Fig.3. The equivalent dielectric-charge density Q_{ox} is calculated as $-C_{ox}$ $(V_{fb}-\phi_{ms})/q$, where the work-function difference ϕ_{ms} between aluminium and Si is calculated to be –0.70 eV for p-type Si substrate. The slightly larger EOT of the NO sample should be due to oxidation role of NO. On the other hand, as can be seen from Fig.2, the NO sample has the minimum hysteresis (0.05 V), which indices that the NO annealing can effectively decrease the traps at/near the interface by incorporating nitrogen to form Si≡N bonds and passivate the structural defects near the interface.[20] For the other two samples, their hysteresis is obviously bigger than that of the NO sample (0.15 V and 0.21 V for the NH_3 and N_2 samples respectively). This indicates that the N_2 annealing cannot effectively decrease the structural defects near the interface.[18] Moreover, although the NH_3 annealing can also passivate the structural defects near the interface, hydrogen species from NH_3 decomposition create electron traps.[21] It is well known that nitridation can lead to formation of strong Si≡N bonds for passivating the dangling Si bonds and replacing strained Si—O bonds at the interface. Thus the NO and NH_3 annealing can transform HfTiO into HfTiON by nitrogen incorporation.[20–22] In addition, the NO annealing would also form a HfTiSiON interlayer and thus a SiON-like interface due to oxynitrided role of NO, giving smaller Q_{ox}, $|V_{fb}|$ as shown in Table 1. It is worth pointing out that the smallest Q_{ox} and thus $|V_{fb}|$ of the NH_3 sample probably arise from a compensation effect between

the negative charges of electron traps related to hydrogen and the positive fixed charges associated with nitridation.[21] The existence of a large amount of electron traps induced by the NH_3 annealing is supported by a large gate leakage current in the accumulation region, as shown in Table 2.

Table 1. Equivalent dielectric thickness, flat-band voltage and dielectric-charge extracted from HF C–V curve.

Sample	N_2	NH_3	NO
EOT/nm	7.9	7.9	8.2
V_{fb}/V	–1.14	–0.72	–0.78
Q_{ox}/cm^{-2}	12×10^{11}	0.6×10^{11}	2.2×10^{11}

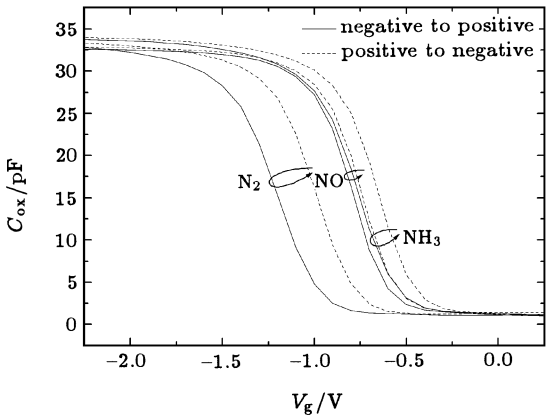


Fig.2. Typical high-frequency C–V curves of the samples under dark condition at room temperature.

Table 2. Gate leakage current density and its change at V_g=–1 V before and after a 1000-s stressing at 7 MV/cm.

Sample	N_2		NH_3		NO	
Condition	fresh	post-stress	fresh	post-stress	fresh	post-stress
$J_g/(10^{-7}A/cm^2)$	10.0	13.0	7.6	15.0	4.5	5.0
Increment/%		30		97		11

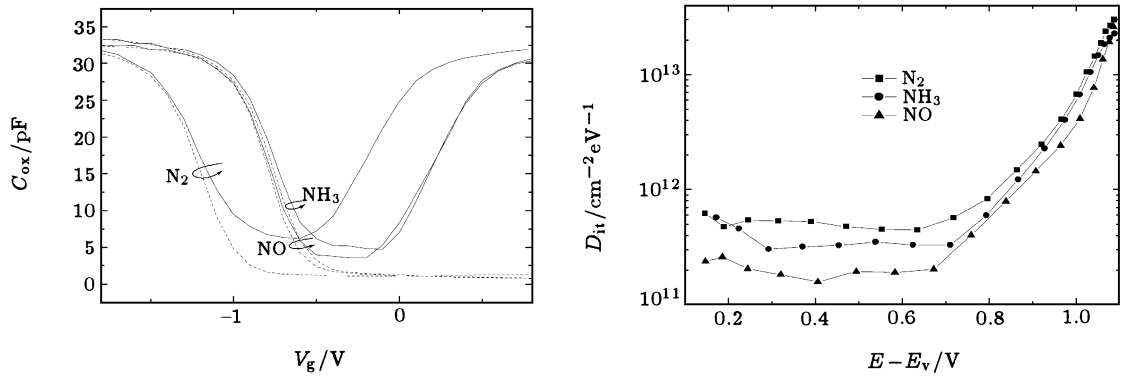


Fig.3. Typical high-frequency and quasi-static C–V curves of the samples under dark condition at room temperature and interface-state density D_{it} extracted from them.

Reliability of the samples is another major concern in device performances. For this, a high-field stressing (7 MV/cm), with the capacitors biased in accumulation at room temperature, is applied to evaluate the qualities of HfTiO/Si and HfTiON/Si interfaces by monitoring the flat-band voltage shift. As shown in Fig.4, the NO and NH_3 samples exhibit the minimum and maximum ΔV_{fb} respectively among the samples, implying a robust and less-strained interface in the NO sample, and many weak bonds near/at the interface related to hydrogen species from NH_3 decomposition in the NH_3 sample. Negative ΔV_{fb} means generations of donor-like interface states and near-interface hole traps in the dielectric. Excellent reliability of the NO sample shows that nitrogen incorporation can be effectively achieved near/at the HfTiON/Si interface and can create a large number of strong Si≡N bonds.

Table 2 listed in the gate leakage current and its change at V_g=–1V before and after a 1000-s stressing at 7 MV/cm. The fresh N_2 sample exhibits the largest leakage current because of a large trap-assisted tunnelling current associated with its large D_{it}. For the fresh NO sample, the gate leakage current is the lowest due to small D_{it} and also larger EOT (see Table 1). On the other hand, similar to the results in Fig.4, the NH_3 and NO samples have the maximum and minimum increments of gate leakage current after the stressing and further indicate a less-strained dielectric/Si interface for the NO-annealed sample.

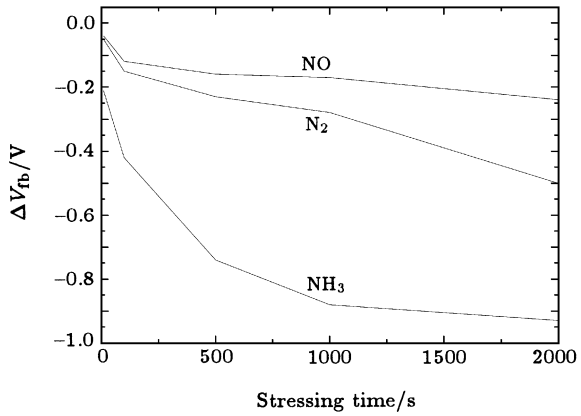


Fig.4. Flatband-voltage shift of the samples under high-field stress (7 MV/cm) at room temperature, with the capacitors biased in accumulation. Area of capacitors is 7.85×10^{-5} cm^2.

However, the NH_3 annealing introduces some hydrogen species whose bonds can be easily broken during high-field stressing, and as a result, the gate leakage current is greatly increased through the trap-assisted tunnelling mechanism.

4. Summary

HfTiO film is prepared by reactive RF co-sputtering, and the effects of RTA in different gas ambiences on electrical properties of MOS capacitors are investigated. The experimental results indicate that the NO annealing gives a HfTiON dielectric with a HfTiSiON interlayer, thus resulting in low interface-state/dielectric-charge densities and enhanced reliability. It is proposed that these improvements are likely associated with the passivation effects of N on the structural defects at/near the HfTiON/Si interface (formation of stronger Si≡N bonds). In summary, the co-sputtering of Hf and Ti targets in an Ar/O_2 ambience followed by a NO annealing could have high potential for preparing the high-k gate dielectric of advanced small-sized MOSFETs.

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