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Critical area computation for real defects and arbitrary conductor shapes*

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In current critical area models, it is generally assumed the defect outlines are circular and the conductors to be rectangle or the merger of rectangles. However, real defects and conductors associated with optimal layout design exhibit a great variety of shapes. Based on mathematical morphology, a new critical area model is presented, which can be used to estimate the critical area of short circuit, open circuit and pinhole. Based on the new model, the efficient validity check algorithms are explored to extract critical areas of short circuit, open circuit and pinhole from layouts. The results of experiment on an approximate layout of 4×4 shifts register show that the new model predicts the critical areas accurately. These results suggest that the proposed model and algorithm could provide new approaches for yield prediction.

Keywords: real defects, critical area model, mathematical morphology, yield estimation
PACC: 8116, 6630L, 8220W, 6780M

1. Introduction

Yield estimation is very important for the IC manufacturing industry.[1−3] The yield estimate can be used in production control, material management, timely product delivery and operations of planning tool and can be used to highlight designs that have much lower than expected yield, to determine the cost of new devices and their resource implications. It is also the focal point of the industry evolving from production of standard products such as the memories, to the production of application of specific integrated circuit (ASIC) and system on chip (SOC) products. Physical defects have always played an important role in integrated circuit (IC) yields, and the design sensitivity to these physical elements has continued to increase in today's nanometre technologies.[4] Among typical CMOS processes, the electrical fault caused by defects, is one of the factors leading to greatest loss of yield. In general,[5,6] the Poisson yield model is often used to predict the yield loss due to defects.

$$Y = \prod \mathrm{e}^{-\lambda_i}\,, \tag{1}$$

$$\lambda_i = A_i^{(\mathrm{c})} D_i\,, \tag{2}$$

where Y denotes yield, which is the product of all layer yields, λ_i is the average faults for layer i. $A_i^{(\mathrm{c})}$ is the critical area related to a layout for layer i, and D_i is the defect density for layer i, and $A_i^{(\mathrm{c})}$ is given by

$$A_i^{(\mathrm{c})} = \int_{R_{\min}}^{R_{\max}} A(R) h(R) \mathrm{d}\, R\,, \tag{3}$$

where $A(R)$ is the critical area with a diameter R, $h(R)$ is the size distribution of defects, $R_{\min}$ is the minimal diameter and $R_{\max}$ is the maximal diameter based on the circular model.

The relation of average critical areas to the chip area is expressed as

$$A_i^{(\mathrm{c})} = A_{\mathrm{chip}} \theta_i\,, \tag{4}$$

where θ_i is the average fault probability for layer i and A_{chip} is the area of the chip.

Equations (1)–(4) show that the model of real defect outlines and the features associated with conductor layouts are two main factors for critical area estimation. The real defect outlines that exhibit a great variety of defect shapes are usually modelled as circular ones,[7−12] which causes the errors in critical area estimation.[13−16] In addition, the conductor shapes on layouts related critical areas are assumed to be

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of the regular geometric form such as rectangles or their mergers.[17,18] However, due to the limitation of photolithography, in existing integrated circuit design-for-yield (DFY), the conductor shapes obtainable on layouts exhibit non-regular forms. For DFY, it is a puzzle to estimate the critical areas of a real defect with the non-regular conductor form on layouts.[19] In order to evaluate the yield accurately and optimize layout design, it is significant to study the model of the critical areas of a real defect with non-regular conductor forms on layouts.

2. Mathematical morphology and the core of a real defect

2.1. The fundamental operations of morphology

Mathematical morphology was developed in the 1970's by Serra.[20] It has several advantages over other techniques, especially when applied to image processing. There are four fundamental operations in morphology, which are dilation, erosion, opening and closing. The basic operations of binary morphology are defined as follows.

DILATION

$$\mathrm{DILATE}(S,E) = \cup \mathrm{TRAN}(E;i,j), (i,j) \in D_s\,; \tag{5}$$

EROSION

$$[\mathrm{ERODE}(S,E)](i,j) = \begin{cases} 1 & \text{if TRAN } (E;i,j) \cup S = S; \\ * & \text{otherwise;} \end{cases} \tag{6}$$

OPENING

$$\mathrm{OPEN}(S,E) = \cup\{\mathrm{TRAN}\ (E;i,j) : \mathrm{TRAN}(E;i,j) \cup S = S\}; \tag{7}$$

CLOSING

$$[\mathrm{CLOSE(S,E)}](p,q) = \begin{cases} 1 & \text{if for all } [\mathrm{TRAN}(E;i,j)](p,q) = 1, \\ & \text{and } \mathrm{TRAN}(E;i,j) \cap S \neq \Phi; \\ * & \text{otherwise.} \end{cases} \tag{8}$$

Here 1 denotes the known pixel of an image S, $*$ the unknown pixel, D_s represents the S domain which is a set of the known pixel positions of the image S, E is the structure element which is converted by S, generally. The TRAN $(E;i,j)$ is defined as placing the centre of E to the position (i,j) of image S and then copying the image. The symbols (i,j) in Eq.(6) and (p,q) in Eq.(8) are the positions of the results from $\mathrm{ERODE}(S,E)$ and $\mathrm{CLOSE}(S,E)$, respectively.

2.2. The core of a real defect

As critical area is defined as the region in which the core of a defect must fall in order to cause an electrical fault, it is necessary to character the core of a defect. The core of a defect can be obtained by using its boundary chain code, which begins with a starting point that has eight neighbouring-points with one point on the boundary at least. The boundary chain code prescribes the direction that must be used from the current boundary point to a next point.

Given $(X_{\mathrm{o}}, Y_{\mathrm{o}})$, for chain codes from (X_{j-1}, Y_{j-1}) to (X_j, Y_j), A_{jx} is the horizontal displacement, and A_{jy} the vertical displacement. Then, the coordinates of each point expressed by chain codes is (X_i, Y_i) and the area of a defect is AREA:

$$X_i = \sum_{j=1}^{i} A_{jx} + X_{\mathrm{o}}, \quad Y_i = \sum_{j=1}^{i} A_{jy} + Y_{\mathrm{o}}, \tag{9}$$

$$\mathrm{AREA} = \sum_{j=1}^{n} A_{jx} * \frac{1}{2}(Y_{j-1} + Y_j) * e^2, \tag{10}$$

where e is the unit of a distance determined by the manufacturing technology. If AREA is not zero, the core of a defect is obtained by finding the gravity cen-

tre of a defect. With its even density, the gravity centre of a defect is equal to the core. For a defect the first-moment matrix M_x of X axis and M_y of Y axis are:

$$M_x = -\sum_{j=1}^{n} \frac{1}{2} \times A_{jx}(Y_{j-1}^2 + A_{jy} \times (Y_{j-1} + A_{jy}/3)), \tag{11}$$

$$M_y = \sum_{j=1}^{n} \frac{1}{2} \times A_{jy}(X_{j-1}^2 + A_{jX} \times (X_{j-1} + A_{jx}/3)). \tag{12}$$

The core of a defect (X_c, Y_c) is:

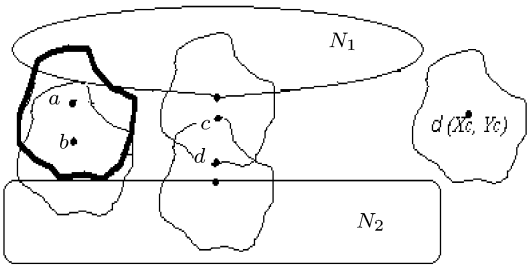
$$X_c = M_x/\text{AREA}, \qquad Y_c = M_y/\text{AREA}. \tag{13}$$

3. Critical area modelling

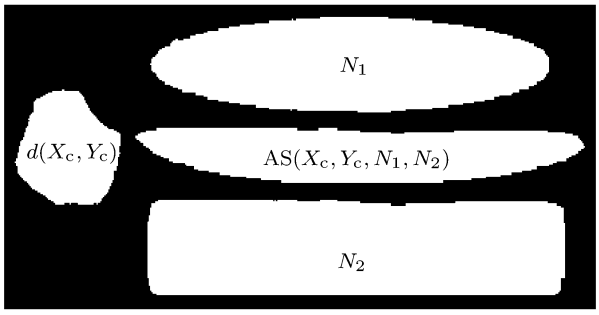
There are three main kinds of defects that have remarkable impact on the structure of a circuit for IC, the conductor extra defects, the conductor missing defects and pinhole defects. Accordingly, there are three kinds of critical areas: namely short circuit critical area, open circuit critical area and pinhole critical areas.

3.1. Short circuit critical area modelling

For a conductor $N_1(i_1, j_1)$ with row n_1 and column m_1, where $i_1 = 1, 2, \ldots, n_1$ and $j_1 = 1, 2, \ldots, m_1$, and another $N_2(i_2, j_2)$ with row n_2 and column m_2, where $i_2 = 1, 2, \ldots, n_2$ and $j_2 = 1, 2, \ldots, m_2$, the short circuit critical area is the region in which the centre of a real defect must fall in order to cause the conductor N_1 to be completely linked to N_2. For example, Fig.1(a) gives the points a, b, c and d on the boundary of the critical area, where the points a, b, c and d are the centres of defects.



(a)



(b)

Fig.1. (a) Short critical area for computation; (b) Short critical area of arbitrary conductor and real defect shapes.

Based on the definition of mathematical dilation operation and the concept of short circuit critical area, we put forward a short circuit critical area model. Associated with the real defect $d(X_c, Y_c)$ and the arbitrary conductor shapes N_1, N_2, ,the short circuit critical area $\text{AS}(X_c, Y_c, N_1, N_2)$ is composed of the intersection (see Fig.1(b)) which is caused by dilation of conductors N_1 and N_2 with a real extra defect $d(X_c, Y_c)$, and is expressed as

$$\text{ASD}(X_c, Y_c, N_1, N_2) = \text{DILATE}(N_1, X_c, Y_c) \cap \text{DILATE}(N_2, X_c, Y_c), \tag{14}$$

$$\text{SN}_1 = \text{ASD}(X_c, Y_c, N_1, N_2) \cap N_1, \tag{15}$$

$$\text{SN}_2 = \text{ASD}(X_c, Y_c, N_1, N_2) \cap N_2, \tag{16}$$

$$\text{AS}(X_c, Y_c, N_1, N_2) = \begin{cases} (\text{ASD}(X_c, Y_c, N_1, N_2) - \text{SN}_1 - \text{SN}_2) \cup N_1, & \text{if for all } (i_1, j_1) \text{ and } (i_2, j_2) \\ & \text{SN}_1 \neq 0 \text{ and } \text{SN}_2 \neq 0; \\ \text{ASD}(X_c, Y_c, N_1, N_2), & \text{otherwise.} \end{cases} \tag{17}$$

Here $d(X_c, Y_c)$ is the core of a defect and the origin of the structure element, DILATE(N_1, X_c, Y_c) denotes the dilating conductor N_1 by defect $d(X_c, Y_c)$, DILATE(N_2, X_c, Y_c) is the dilation of conductor N_2 with defect $d(X_c, Y_c)$, and ASD(X_c, Y_c, N_1, N_2) is the overlap between DILATE(N_1, X_c, Y_c) and DILATE(N_2, X_c, Y_c). If ASD(X_c, Y_c, N_1, N_2) is zero, then the critical area is zero, which corresponds to the situation that a small-sized defect will cause short circuit between conductors. If both SN_1 and SN_2 are zero, the critical area of a larger sized defect is obtained by using Eqs.(11) and (12), and can be shown by the region between N_1 and N_2 in Fig.1(b). If neither SN_1 nor SN_2 is zero, the critical area reaches its maximum, that is, the merger of N_1 and the region between N_1 and N_2.

3.2. Open circuit critical area modelling

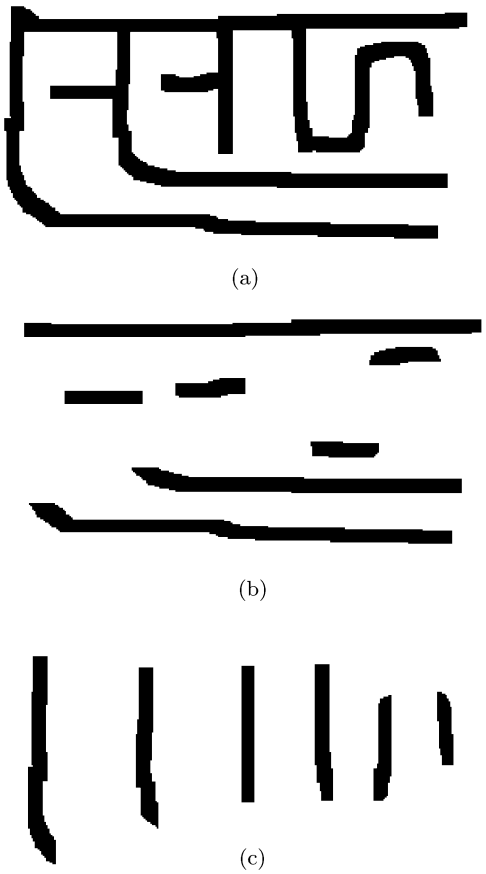


Fig.2. (a) Arbitrary conductor shapes; (b) Horizontally arbitrary conductor shapes; (c) Vertically arbitrary conductor shapes.

Now it is necessary to estimate the open circuit critical area of the complex-shaped conductor with real defects. Unfortunately, there has been no way of knowing the whole model by mathematical morphology processing. However, complex conductor shapes can be divided into many pieces of horizontal lines and vertical lines according to the local line width, as the layout shown in Fig.2(a) that can be divided into lines as in Figs.2(b) and 2(c). Then the open circuit critical areas can be treated as two parts, the model of the horizontal conductor and the model of vertical conductor.

For a conductor $N(i, j)$ with n rows and m columns, where $i = 1, 2, \ldots, n$, $j = 1, 2, \ldots, m$, the open circuit critical area is the region in which the centre of a real defect must fall in order to cause the conductor N to be completely broken. For example, Fig.3(a) gives the points a, b, c and d on the boundary of the critical area, where a, b, c and d are the centres of defects and all critical areas are shown in Fig.3(b).

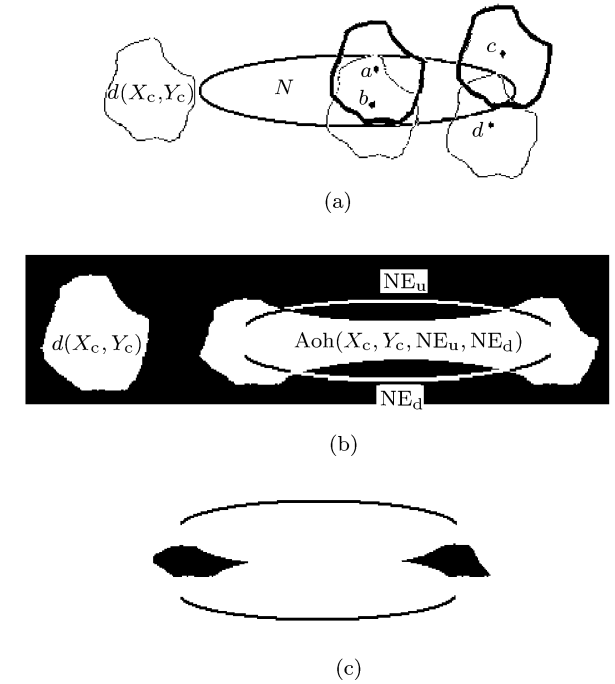


Fig.3. (a) Open critical area for computation; (b) Open critical area of arbitrary conductor and real defect shapes; (c) Open critical area caused large sized conductor and small sized defect.

Let us first determine the open circuit critical area for a conductor of $m > n$. According to the definitions of dilation computation in mathematical morphology and open circuit critical area, it is assumed that the structure element is the real defect $d(X_c, Y_c)$, in which the core of the defect and the origin position of the structure element are (X_c, Y_c). NE$((i_{min}, i_{max}), (j_{min}, j_{max}))$ is the bound-

ary of $N(i,j)$, where $i_{\min}$ is the minimum, $i_{\max}$ the maximum value, $j_{\min}$ the minimal column and $j_{\max}$ the maximum column. By this way NE can be divided into the upper $\mathrm{NE_u}$ and the lower $\mathrm{NE_d}$. Then, the intersection (see Fig.3(b)) of dilating real defect $d(X_\mathrm{c}, Y_\mathrm{c})$ with conductors $\mathrm{NE_u}$ and $\mathrm{NE_d}$, the open circuit critical area $\mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d})$ of the arbitrary defect $d(X_\mathrm{c}, Y_\mathrm{c})$ and conductor shapes $N(i,j)$ can be written as

$$\mathrm{NE}(i,j) = \begin{cases} 0 & \text{if } j = j_{\min} \text{ or } j = j_{\max}, \\ \mathrm{Edge}(N(i,j)) & \text{otherwise}, \end{cases} \tag{18}$$

$$\mathrm{NE} = \mathrm{NE_u} + \mathrm{NE_d}, \tag{19}$$

$$\mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d}) = \mathrm{DILATE}(\mathrm{NE_u}, X_\mathrm{c}, Y_\mathrm{c}) \cap \mathrm{DILATE}(\mathrm{NE_d}, X_\mathrm{c}, Y_\mathrm{c}), \tag{20}$$

where $\mathrm{DILATE}(\mathrm{NE_u}, X_\mathrm{c}, Y_\mathrm{c})$ is the dilation of NE_u to $d(X_\mathrm{c}, Y_\mathrm{c})$ and $\mathrm{DILATE}(\mathrm{NE_d}, X_\mathrm{c}, Y_\mathrm{c})$ is of the dilation of $\mathrm{NE_d}$ to $d(X_\mathrm{c}, Y_\mathrm{c})$. For Eq.(18), when $\mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d})$ is zero, it fits with the result of the minimal size of defects which will not cause the critical area. When $\mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d})$ is small, the critical area is the discontinuous area corresponding to smaller sized defects (see Fig.3(c)). When the defect is larger in size, the critical area is the maximum.

Next, we must determine the open circuit critical areas for a conductor of $m \leq n$. Similarly, according to the definitions of dilation computation in mathematical morphology and open circuit critical area, we then assume that the structure element is the real defect $d(X_\mathrm{c}, Y_\mathrm{c})$, and (X_c, Y_c) is the core of a real defect as well as the origin position of a structure element. $\mathrm{NE}((i_{\min}, i_{\max}), (j_{\min}, j_{\max}))$ is the boundary of $N(i,j)$, where $i_{\min}$ is the minimal row and $i_{\max}$ the maximum row while $j_{\min}$ the minimal column and $j_{\max}$ the maximum column. By this way the NE can be divided into the regions of left $\mathrm{NE_L}$ and right $\mathrm{NE_R}$. Then the intersection of dilating the real missing defect $d(X_\mathrm{c}, Y_\mathrm{c})$ by conductors $\mathrm{NE_L}$ and $\mathrm{NE_R}$, the open circuit critical area $\mathrm{Aov}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_L}, \mathrm{NE_R})$ of arbitrary defect $d(X_\mathrm{c}, Y_\mathrm{c})$ and conductor shapes $N(i,j)$ can be written as

$$\mathrm{NE}(i,j) = \begin{cases} 0 & \text{if } i = i_{\min} \text{ or } i = i_{\max}, \\ \mathrm{Edge}(N(i,j)) & \text{otrerwise}, \end{cases} \tag{21}$$

$$\mathrm{NE} = \mathrm{NE_L} + \mathrm{NE_R}, \tag{22}$$

$$\mathrm{Aov}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_L}, \mathrm{NE_R}) = \mathrm{DILATE}(\mathrm{NE_L}, X_\mathrm{c}, Y_\mathrm{c}) \cap \mathrm{DILATE}(\mathrm{NE_R}, X_\mathrm{c}, Y_\mathrm{c}). \tag{23}$$

From Eqs.(19)–(23), it is possible to express the open circuit critical area of the complex conductor shapes of real defects in terms of $\mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d})$ and $\mathrm{Aov}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_L}, \mathrm{NE_R})$, which can be described as

$$\mathrm{Ao}(X_\mathrm{c}, Y_\mathrm{c}, N) = \mathrm{Aoh}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_u}, \mathrm{NE_d}) + \mathrm{Aov}(X_\mathrm{c}, Y_\mathrm{c}, \mathrm{NE_L}, \mathrm{NE_R}). \tag{24}$$

3.3. Pinhole critical area model

Regarding the conductors N_1, N_2 with arbitrary shapes, which have overlapped area on adjacent layer

of the figure, it is assumed that the interlayer defect is of arbitrary shapes, as shown in Fig.4(a) and the vertical projection is $d(X_c, Y_c)$. So the pinhole critical area is the region in which the centre of a real defect must fall in order to cause the adjacent conductors to be completely linked. For example, Fig.4(b) gives the points a, b, c and d on the boundary of the critical area, where a, b, c and d are the centre of defects, and all critical areas $\mathrm{AP}(X_c, Y_c, N_1, N_2)$ are the region surrounded by dashed lines, as shown in Fig.4(c).

$$\mathrm{AP}(X_c, Y_c, N_1, N_2) = \mathrm{DILATE}(N_1 \cap N_2, X_c, Y_c), \quad (25)$$

where $N_1 \cap N_2$ is the overlap of conductors N_1 and N_2.

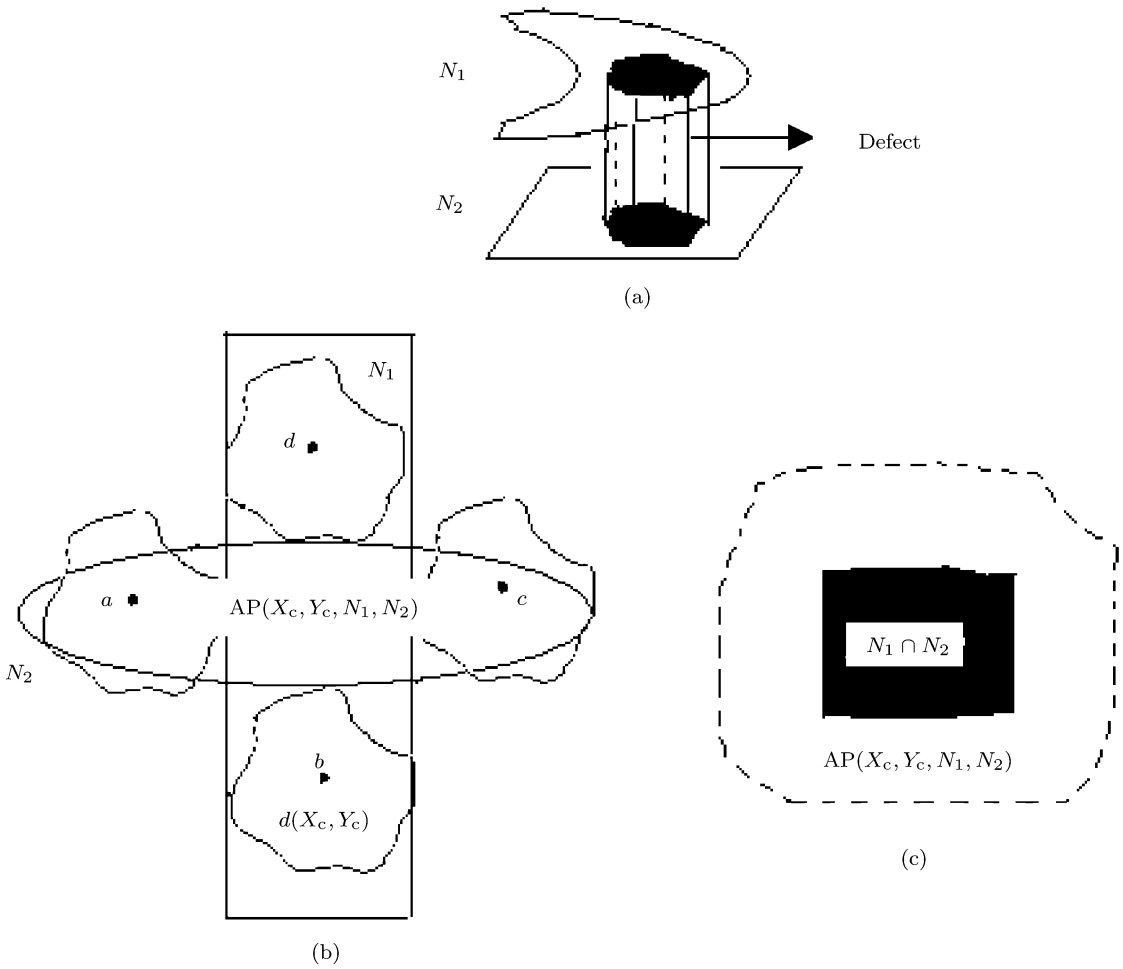


Fig.4. (a) Pinhole defect between conductors N_1 and N_2; (b) Pinhole defect critical area for computation; (c) Pinhole defect critical area.

4. Model validation and experimental result analysis

It is assumed that the defect shape is of arbitrary form, and the layouts, which are changed into the multi-layer plane figure, are of Caltech intermediate form (CIF) file format. To verify the new model, we design the realization algorithm corresponding to the new model and provide a group of operation results.

4.1. Extraction algorithm for short circuit critical area

For the layer of a conductor layout, we design an algorithm to extract the short circuit critical area as shown in Fig.5. With the algorithm, the counts c of conductors are labelled according to their columns firstly, and the critical area of each pair of conductors is extracted based on the short circuit critical area

model. The critical area at different layers can be obtained by iterating the algorithm.

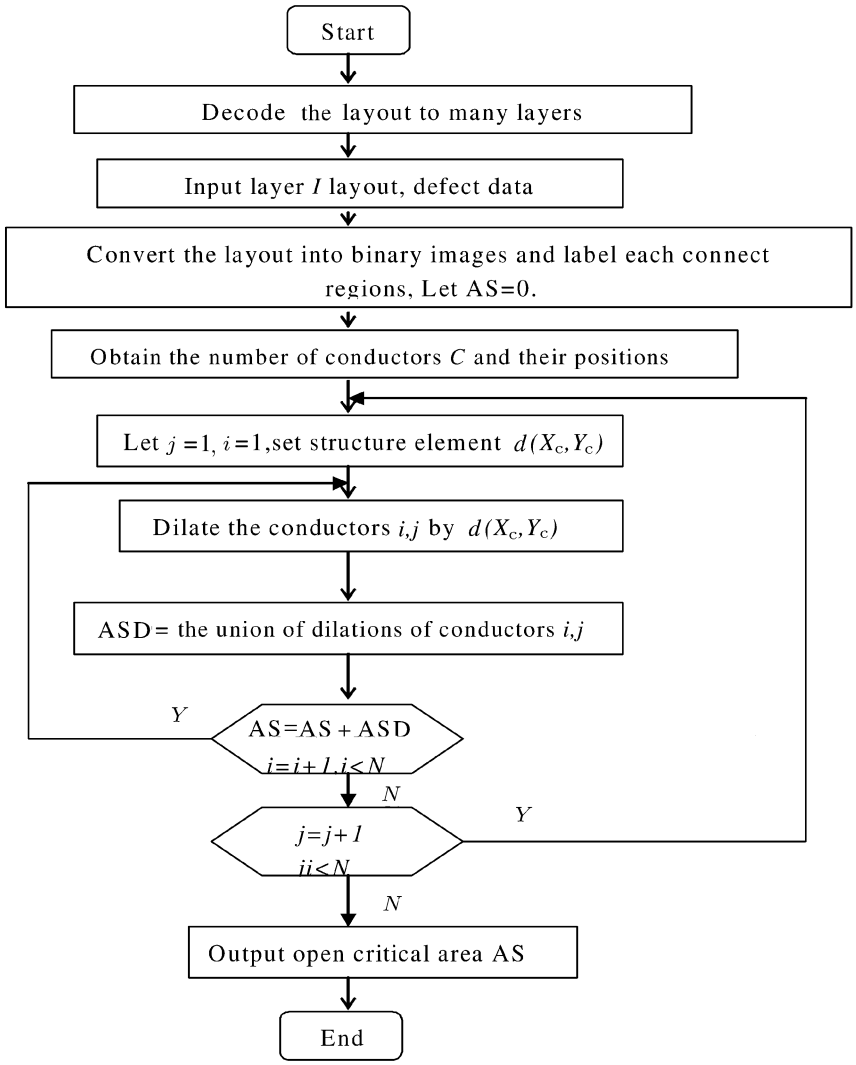


Fig.5. Flow chart to extract the short circuit critical area.

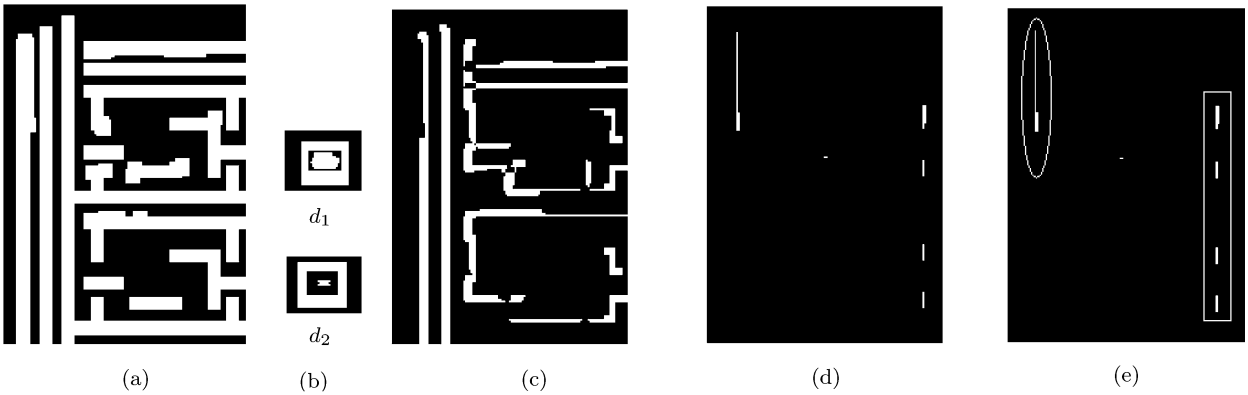


Fig.6. (a) Source layout; (b) Real defects; (c) Critical area produced by d_1; (d) Critical area produced by d_2; (e) Union of Fig.6(a) and Fig.6(d).

Some results of the algorithm in the experiment are shown in Fig.6. The local experimental layout consists of arbitrary conductor shapes, which is similar to 4×4 shift register layout (see Fig.6(a)). According to the features of the real layout, two defects with different sizes and shapes can be obtained, which are $d_1(6,8)$ and $d_2(2,3)$, respectively, (see Fig.6(b)), where (6,8) denotes the centre of defect d_1 as well as the origin position when d_1 is regarded as the structure element, and (2,3) denotes the centre of d_2 as well as the origin position of the structure element d_2. Then the critical area associated with Fig.6(a) produced by d_1 is shown in Fig.6(c), and also that by d_2 in Fig.6(d). In order to design yield expediently, Fig.6(e) shows the union of Figs.6(a) and 6(d). From Fig.6(e), it can be seen that the critical area with d_2 consists of the elliptic and rectangular regions. Altering the conductors in the two regions can decrease the critical areas and increase IC yield.

4.2. Extraction algorithm for open circuit critical area

For the layer of a conductor layout, the algorithm as in Fig.7 is explored to extract the open circuit critical area. Using mathematical morphology opening operations, the algorithm divides a layer layout into the vertical conductor layout and the horizontal one, then we can find and merge those critical areas. The open circuit critical areas at different layers can be obtained by iterating the algorithm.

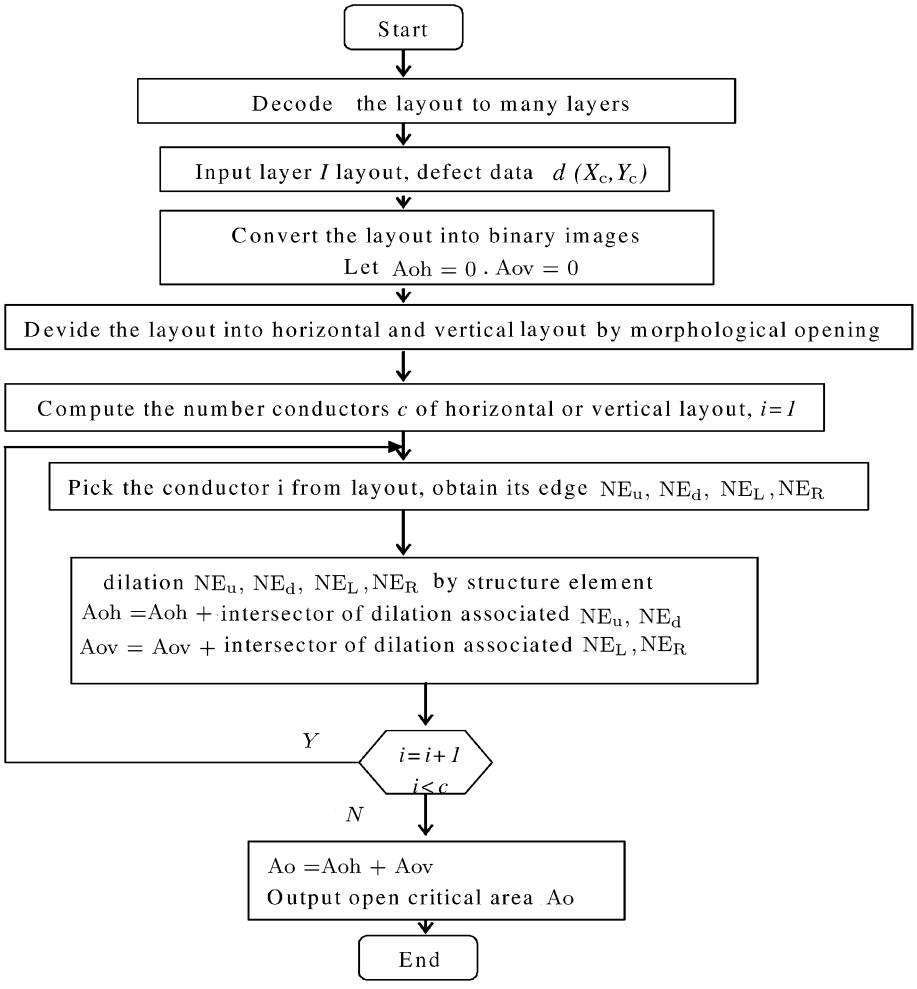


Fig.7. Flow chart to extract opening critical area.

Some results of the algorithm in the experiment are shown in Fig.8. The local experimental layout consists of arbitrary conductor shapes, similar to 4×4 shifts register layout (see Fig.8(a)). Figure 8(b) shows the

decomposed horizontal layout, including arbitrary conductor shapes. Let the real defect be $d(6,8)$, as shown in Fig.8(c), its open circuit critical area is shown in Fig.8(d). Similarly, Fig.8(e) shows the decomposed vertical layout, including arbitrary conductor shapes also. Real defect $d(6,7)$ is shown in Fig.8(f), and Fig.8(g) shows the union of Fig.8(e) and the open circuit critical area. Figure 8(h) is the union of Fig.8(a) and the source layout. From Fig.8(h), it can be seen that the algorithm can efficiently extract the open circuit critical area for arbitrary conductor shapes.

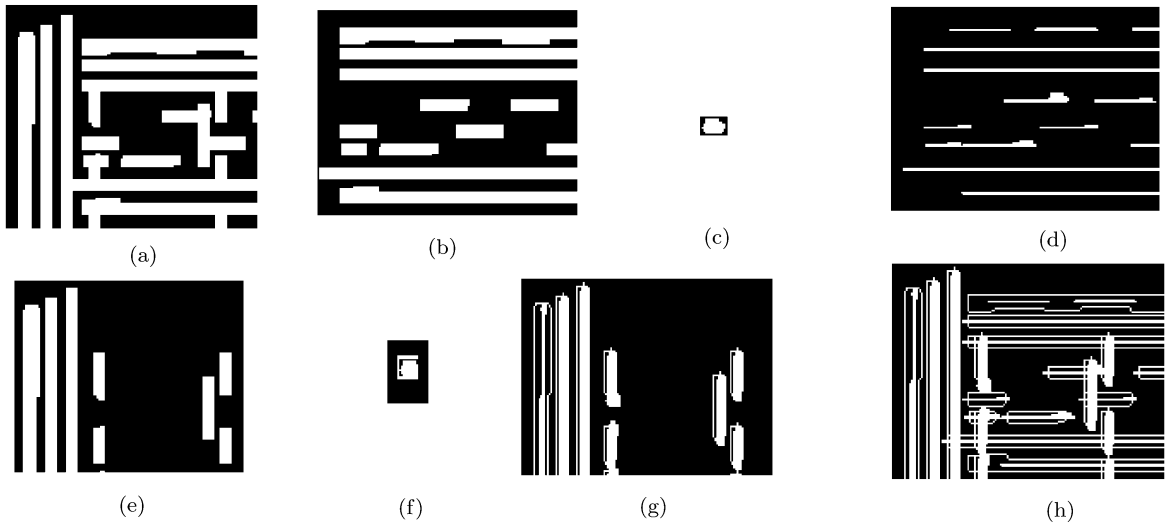


Fig.8. (a) Source layout; (b) Horizontal conductors: (c) Real defect; (d) Open critical area by Fig.6(c); (e) Vertical conductors divided by Fig.6(a); (f) Real defect; (g) Union of critical area and Fig.6(e); (h) Open critical area.

4.3. Extraction algorithm for pinhole critical area

For the adjacent layers in a conductor layout, the algorithm shown in Fig.9 is designed to extract the pinhole circuit critical area. The algorithm begins with gaining the intersection of two layers in a layout, and then the pinhole critical area is formed by the mathematical morphology dilation. The pinhole critical area at different adjacent layers can be obtained by iterating the algorithm.

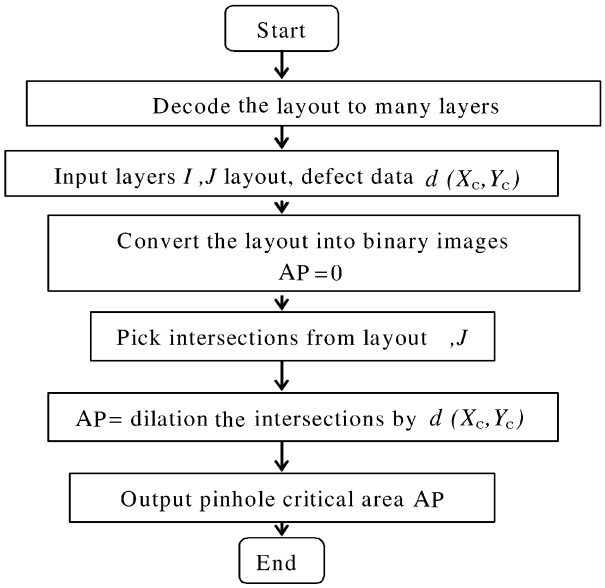
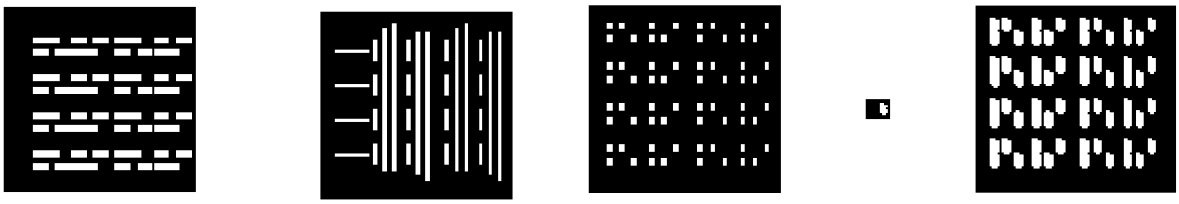


Fig.9. Flow chart to extract pinhole critical area.

Some results of the algorithm in the experiment are shown in Fig.10. Figure 10(a) and 10(b) are the adjacent layout layers, respectively, and their union intersection region is shown in Fig.10(c). Let the real defect be $d(5,3)$ shown in Fig.10(d), the pinhole critical area caused by $d(5,3)$ is shown in Fig.10(e).



(a) (b) (c) (d) (e)

Fig.10. (a) Layout layer N_1; (b) Layout layer N_2; (c) Union of N_1 and N_2; (d) Real defect; (e) Pinhole critical area.

5. Conclusion

Based on mathematical morphology, the new models and their algorithms for the open circuit critical area, the short circuit critical area and the pinhole critical area have been presented and implemented. Using real defects and arbitrary conductor shapes in our models, we show the accuracy and the general validity of the critical area estimations. The experimental results show the efficiency of the new models, which provide the reliable foundations for the optimization of layout design and yield accurate estimation.

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