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Novel vertical stack HCMOSFET with strained SiGe/Si quantum channel*

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A novel vertical stack heterostructure CMOSFET is investigated, which is structured by strained SiGe/Si with a hole quantum well channel in the compressively strained $Si_{1-x}Ge_x$ layer for p-MOSFET and an electron quantum well channel in the tensile strained Si layer for n-MOSFET. The device possesses several advantages including: 1) the integration of electron quantum well channel with hole quantum well channel into the same vertical layer structure; 2) the gate work function modifiability due to the introduction of poly-SiGe as a gate material; 3) better transistor matching; and 4) flexibility of layout design of CMOSFET by adopting exactly the same material lays for both n-channel and p-channel. The MEDICI simulation result shows that p-MOSFET and n-MOSFET have approximately the same matching threshold voltages. Nice performances are displayed in transfer characteristic, transconductance and cut-off frequency. In addition, its operation as an inverter confirms the CMOSFET structured device to be normal and effective in function.

Keywords: strained SiGe/Si, quantum well channel, heterostructure CMOSFET, poly-SiGe gate
PACC: 7360T, 7320D, 7340L

1. Introduction

The prediction of Moore's law has impelled semiconductor devices to be further scaled down. Nowadays, technologies leading complementary metal–oxide–semiconductor (CMOS) to scaling down are involved with both new materials and advanced MOSFET structures. The use of strained technique has attracted considerable attention to advanced MOSFET devices because of their enhancement in effective mobility of both the electrons and holes as compared with that of bulk Si. Different structures have been discussed in order to achieve high-performance CMOS devices.

Previous study has proposed several approaches to pursuing the integration of n- and p-channel strained Si/SiGe MOSFETs in various structures in order to implant these methods into high-performance CMOS technologies. One usually uses a strained silicon (SSi) channel as a p-channel to enhance the hole mobility. The parallel structures of HCMOSFET are illustrated in Refs.[1–6]. In Refs.[7] and [8], another promising structure of HCOMFET with buried SSi for n-channel and strained SiGe (SSiGe) for p-channel has been investigated, based on the same material layers, but unfortunately, on different substrates. It is difficult to integrate both n-channel and p-channel into a monolithic material layer.

In this paper, a novel heterostructure CMOSFET (HCMOS) configuration is investigated, in which the integration of the n-channel with the p-channel is based on exactly the same material layer structure. Therefore it is not necessary to fabricate n- and p-channels discriminatingly in device making, which significantly simplifies the processing and improves the device performance as well. The device with this structure is modifiable in threshold voltage and better in matching of the n-channel and p-channel. The rest of this paper is organized as follows. The contour of the HCMOS is briefly described in Section 2; Section 3 is devoted to discussing several key parameters of this device in detail for evaluating their influences; in Section 4 demonstrated are the simulation results in-

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cluding transfer characteristics, transconductance and cut-off frequency. Then an inverter is simulated to show the validity of function and applicability of the HCMOSFET. The conclusions drawn from the present study are given in Section 5.

2. Device structure and physics

The contour of the novel HCMOSFET is described in Fig.1. Several probable layout modes are demonstrated in Fig.1.(a). 50% of the layout area can be saved if the layout format on the top left corner is employed. Universal layout mode is also applicable to this device.

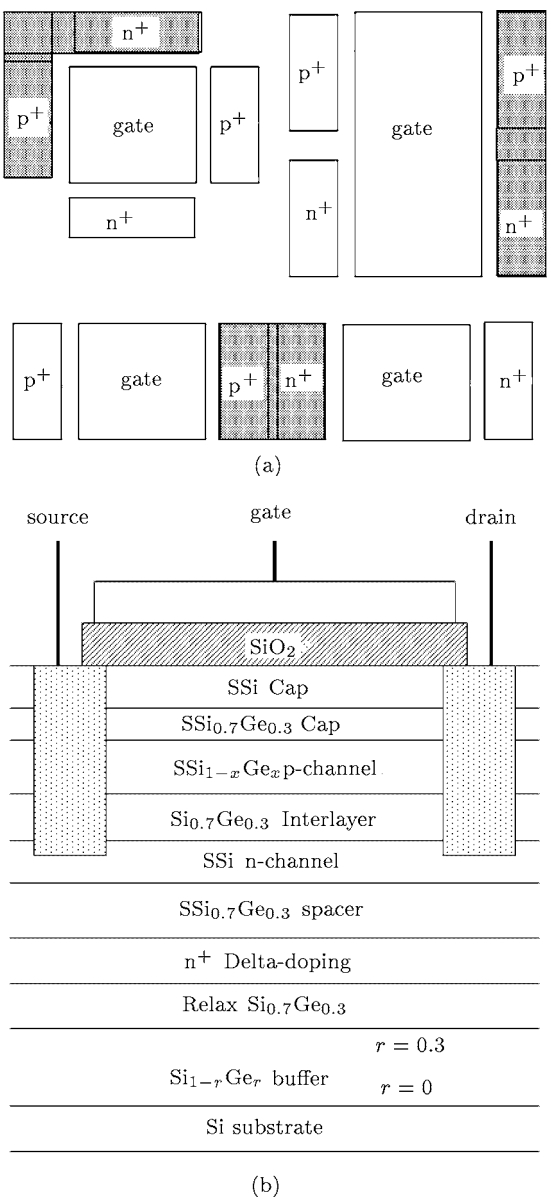


Fig.1. (a) Overlook of the HCMOS; (b) cross section of the HCMOS.

As illustrated in Fig.1(b), the cross section of the HCMOSFET shows the details of the layer structures and materials. A high-quality relaxed $Si_{0.7}Ge_{0.3}$ layer epitaxially grows up on the grading $Si_{1-r}Ge_r$ buffer layer with the r gradually changing from 0 to 0.3. Then a tensile SSi channel layer is fabricated following an n^+ type delta-doping layer providing electrons for the quantum well channel with a $Si_{0.7}Ge_{0.3}$ spacer layer that shields the ionized impurity from scattering. Through growing another relaxed $Si_{0.7}Ge_{0.3}$ interlayer, the critical thickness of SSi layer is increased and the interaction between the buried n-channel and the upper buried p-channel is bated. The strained $Si_{1-x}Ge_x$ ($SSi_{1-x}Ge_x$) layer is grown on the interlayer with the x increasing to 0.5. Accordingly, the high-Ge-content alloy layer is compressively strained due to the large lattice constant of $Si_{1-x}Ge_x$ compared with that of $Si_{0.7}Ge_{0.3}$, making the layer ideal for p-channel of high-mobility holes of a MOS device. Finally, strained $Si/Si_{0.7}Ge_{0.3}$ cap layers cover on the strata. The top Si cap layer is required to allow the formation of a high-quality gate oxide, since the oxidation of SiGe produces a high density of interface states. Standard processing steps could be used to complete the manufacture procedures as follows: oxidation, ion implantation, deposition and metallization. However, the gate material is replaced by p^+ poly SiGe instead of poly silicon or metal to make the threshold voltage modifiable by adjusting the Ge content.

Hitherto, the novel HCMOSFET structure, based on exactly the same material layers, has been exhibited. As the gate is positively biased, the lower SSi layer's conduction band declines, accordingly, electrons are pushed into the quantum well that has formed on the SSi side of interface between the SSi layer and the $Si_{0.7}Ge_{0.3}$ interlayer, thus generating an n-channel. On the contrary, the device presents a p-channel when the gate is negatively biased. Therefore, the holes are filled into the quantum well formed on the $Si_{1-x}Ge_x$ side of interface between the upper $SSi_{1-x}Ge_x$ layer and the $Si_{0.7}Ge_{0.3}$ cap layer. Transfer characteristics and other performances for both n- and p- channels are discussed in Section 4.

3. Band gap structure and analysis

The energy-band diagram of each layer in an equilibrium state at $T = 300$ K is described in Fig.2. In the case, the conduction bands of all semiconductor layers are still above the Fermi level while the valence bands below the Fermi level. Thus, although the band

discontinuity causes bands to bend up, there appear no palpable carriers' channels.

Having positively or negatively biased the gate, and considering $|V_{ds}| = 0.1$ V, the energy-band structure changes as illustrated in Fig.3 (a) and Fig.3(b), respectively. When $V_{gs} = 0.6$ V, the conduction bands decline toward the Fermi level, thus the electron quantum well channel begins to appear in the lower SSi layer, leaving the valence bands sink deeper beneath the Fermi level than their original ones. On the other hand, when the negative bias voltage $V_{gs} = -0.6$ V is applied, contrary to the conduction bands moving upward apart from Fermi level, the valence bands rise to even surmount the Fermi level, causing the hole quantum well channel to form in the $SSi_{1-x}Ge_x$ layer.

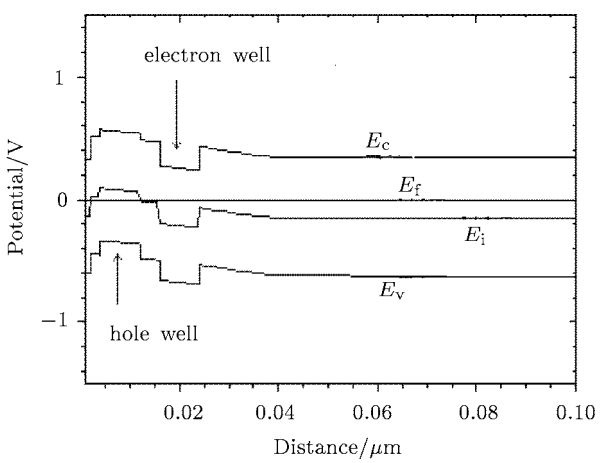


Fig.2. Energy-band diagram of each layer at $V_{gs} = 0$.

There are also many other material and structure parameters that have an effect on the energy-band structure, thus they can change the characteristics of CMOSFET. If p^+ poly SiGe is used as gate material then the gate work function in this HCMOSFET can be modified. Since the gate work function decreases as the Ge component of poly SiGe increases, the threshold voltage of n-channel decreases with the Ge component increasing while that of p-channel increases with the change of band structure. The Ge component of $Si_{1-x}Ge_x$ layer is another one of most fundamental factors in the sense of device performance. Considering the case where the Ge distribution is uniform, as the Ge component increases, the compressive strain strength acting on the $Si_{1-x}Ge_x$ layer rises, which brings up the hole mobility thus benefits significantly the transfer characteristic, transconductance and cut-off frequency.

In order to increase the electron density in the quantum well, a delta-doping layer is introduced, whose doping concentration plays an effective role. For the n-channel, it is true that increasing the doping dose can enhance the electron density in the quantum well, but in the case of overabundant doping only part of electrons can be pushed into the n-channel region, the remaining ones stay in the delta-doping layer. As a consequence, the leakage current rises when the gate voltage is not biased, and the effective electron mobility declines due to the effect of parasitic delta-doping layer channel. Hence, an appropriate doping concentration needs to be determined to meet the requirements for both subthreshold characteristic and mobility enhancement.

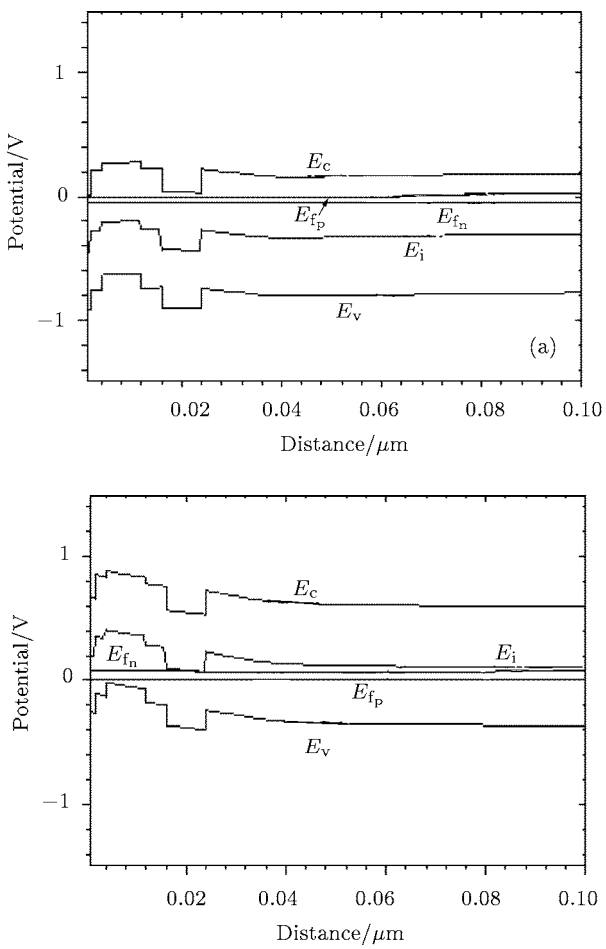


Fig.3. Band structure at $V_{gs} = 0.6$ V (a) and -0.6 V (b).

4. Simulation results

Before simulation, the carrier mobility model needs to be modified to meet the requirements for the new material as the mobility model is going out of date or even absent in the MEDICI programme. Because a creditable theoretic model for carrier mobil-

ity in the quantum well is hard to make, and moreover, the experiment-extracted mobilities are remarkably diverse from each other, here universal body mobility models of strained Si and strained SiGe are chosen as the effective mobility models in the simulation of this device. Although the simulation result may be not excellent, it definitely can verify the validity in function and correctness in device theory. The characteristics such as cut-off frequency and transconductance are expected to be improved tremendously while the mobility is altered by adjusting some experiment-extracted value reported in some papers. Now the universal electron mobility models for the strained Si and strained SiGe are demonstrated as follows.

Consider the silicon at $T = 300$ K, $N_{\rm tol}$ is the doping density and x is the Ge fraction in $Si_{1-x}Ge_x$ on which the silicon grows up. Then the electron mobility of SSi can be described as

$$\mu_{\rm n}(x) = \mu_{\rm n,min}(x) + \frac{\mu_{\rm n,max}(x) - \mu_{\rm n,min}(x)}{1 + (N_{\rm tol}/1.072 \times 10^{17})^{0.73} + (N_{\rm tol}/1 \times 10^{30})^3}\,. \tag{1}$$

If $0 \le x \le 0.15$, then

$$\mu_{\rm n,min}(x) = 55.3(1 + 7.969x - 10.90x^2), \tag{2}$$

$$\mu_{\rm n,max}(x) = 1430(1 + 7.969x - 10.90x^2)\,. \tag{3}$$

And if $0.15 < x \le 0.4$, then

$$\mu_{\rm n,min}(x) = 98.93(1 + 0.9547x - 1.489x^2), \tag{4}$$

$$\mu_{\rm n,max}(x) = 2558.3(1 + 0.9547x - 1.489x^2)\,. \tag{5}$$

Consider the silicon, $T = 300$ K, $N_{\rm tol}$ is the doping density and x is the Ge fraction in $Si_{1-x}Ge_x$. Then the hole mobility of $SSi_{1-x}Ge_x$ is given by

$$\mu_{\rm p}(x) = \mu_{\rm p,min}(x) + \frac{\mu_{\rm p,max}(x) - \mu_{\rm p,min}(x)}{1 + (N_{\rm tol}/1.43 \times 10^{17})^{0.625} + (N_{\rm tol}/1 \times 10^{30})^3}. \tag{6}$$

Considering $SSi_{1-x}Ge_x$, which grows up on the $Si_{0.7}Ge_{0.3}$, and x to be substituted by x-0.3 in Eq.(7),[9,10] then

$$\mu_{\rm p} = \mu_{0\rm p} \times (1 - 0.5x + 27.87x^2 - 25.52x^3), \qquad (0 < x < 0.4). \tag{7}$$

Thus we have the hole mobilities:

$$\mu_{\rm p,min}(x) = 69.34(1 - 3.829x + 7.826x^2), \qquad (0.3 < x \le 0.7). \tag{8}$$

$$\mu_{\rm p,max}(x) = 1083.36(1 - 3.829x + 7.826x^2), \qquad (0.3 < x \le 0.7). \tag{9}$$

After modifying the mobility models, and comprehensively considering all influential factors mentioned in Section 3, the material and structure parameters are determined as shown in Table 1.

Table 1. Material and structure parameters of the HCMOSFET.

parameters	w (Gate)/eV	t (SiO_2)/nm	t (SSi cap)/nm	t (SiGe cap)/nm	t ($SSi_{1-x}Ge_x$ channel)/nm	x (Ge)/nm
values	4.85	15	2	2	8	0.5

parameters	t (SiGe interlayer)/nm	t (SSi channel)/nm	t (SiGe spacer)/nm	t (δ doping)/nm	$N_D(\delta)/cm^{-3}$
values	4	8	8	4	1×10^{18}

In Table 1, w stands for the work function, t for the length, x for the Ge fraction and N_D for the delta-doping concentration. With the channel length being 1um and the source/drain diffusion depth being 25 nm, simulation results about transfer characteristics, transconductance and cut-off frequency are shown in Fig.4(a), Fig.4(b) and Fig.4(c), respectively.

From the illustration in Fig.4 (a) it is clear that n- and p- channels have a good matching of gate threshold voltage, whose absolute value is approximately 0.2 V. It is also noticeable that the p-channel has a smaller saturation current than the n-channel under the condition of the same absolute value gate voltage and source/drain voltage applied. This phenomenon can be partly explained by the fact that the mobility of holes is lower than that of electrons. As a result, the higher mobility of electron also makes the n-MOSFET have better transconductance and cut-off frequency characteristics as shown in Fig.4(b) and Fig.4(c).

What should be pointed out is that the cut-off frequency and transconductance can be significantly improved to a high level as long as the quantum well mobility is taken into account. Some reports involved with the quantum well mobility indicate that the electron mobility can be enhanced to 10^4 – 10^6 cm^2 V^{-1}s^{-1},[11,12] which is significant in mobility enhancement compared with universal body strained Si electron mobility. The enhancement also happens to the holes mobility.[13–18] The channel length is another fundamental parameter that influences the cut-off current and transconductance. If the channel length reduces to a deep-submicron level, characteristics of the CMOS will be definitely improved.

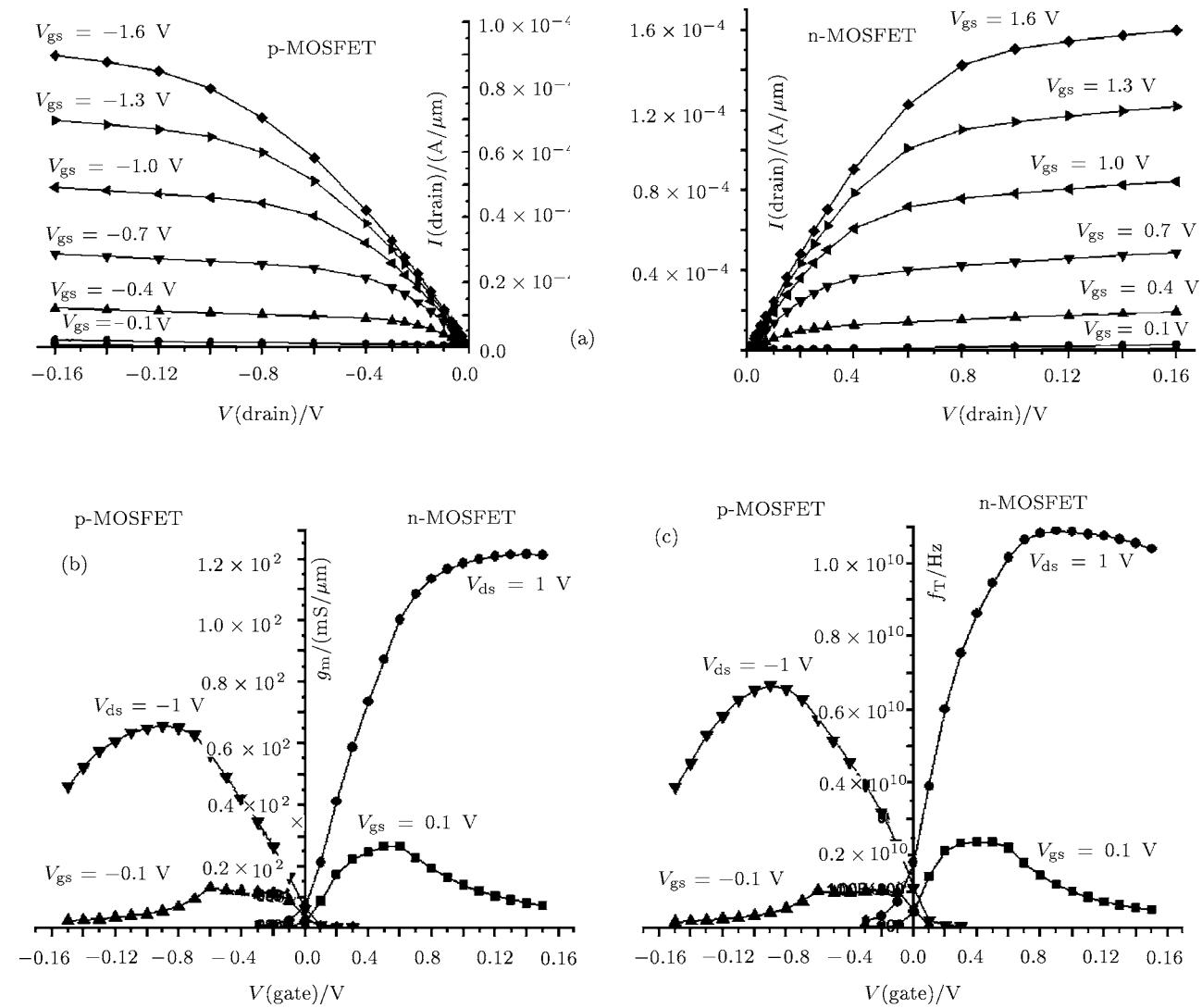


Fig.4. (a) I_D versus V_{ds}, (b) transconductance versus gate voltage, (c) cut-off frequency versus gate voltage.

In order to evaluate the function validity of the CMOS, an inverter is simulated with a square wave stimulation signal. The output voltage and current are demonstrated in Fig.5(c) and Fig.5(d), respectively.

Figure 5(a) illustrates the inverter circuit with elements such as resistance, capacitance and D.C. power supply. The stimulation signal has a period $T = 5$ ns, pulse amplitude $V = 1$ V, duty ratio being 60% and rising time and decay time both being 10 ps. the results show that the CMOS can present the correct logic function and low power consumption especially.

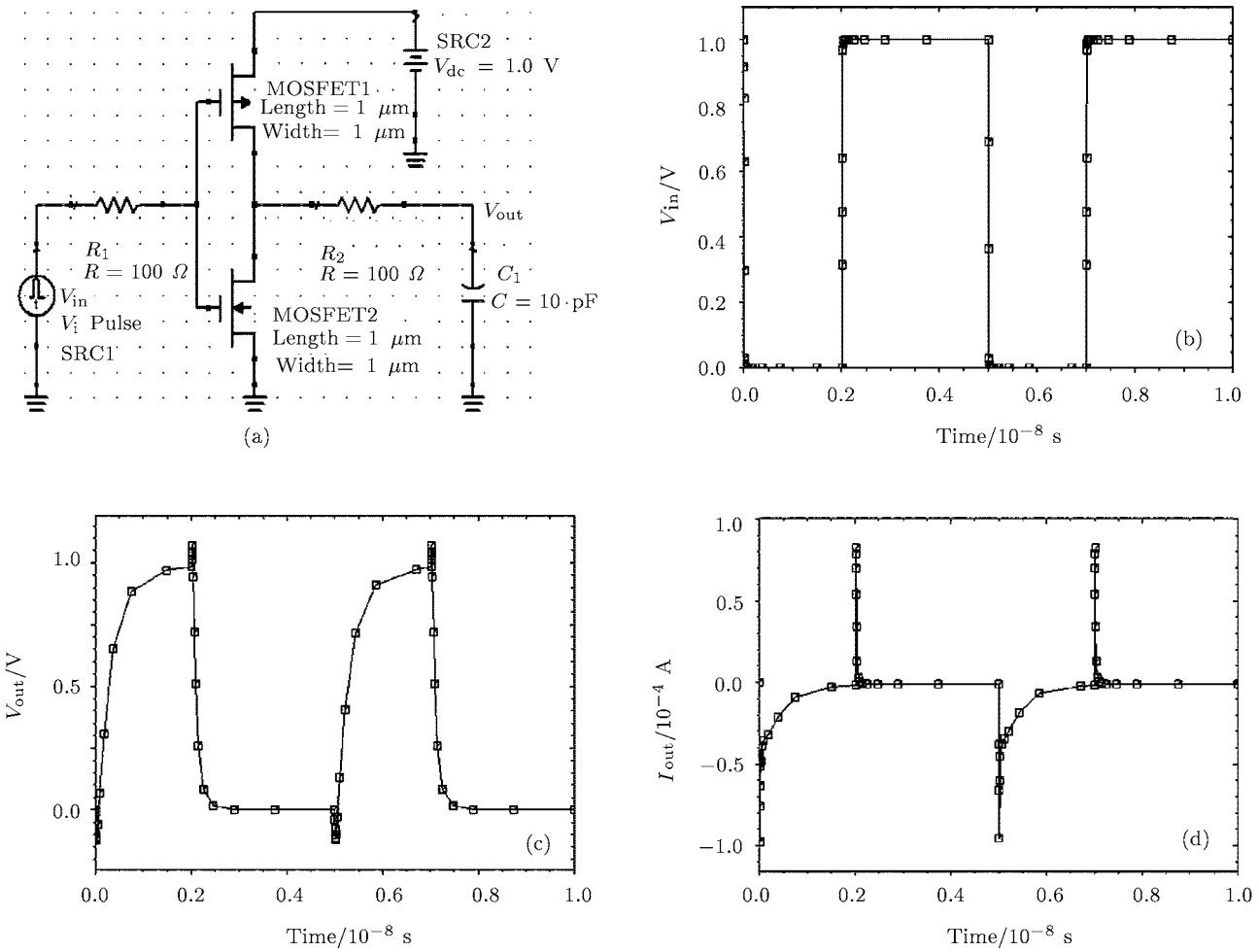


Fig.5. (a) Inverter circuit; (b) square wave stimulation signal versus times; (c) output voltage V_{out} versus times; (d) output current I_{out} versus time.

5. Conclusions

A novel architecture of HCMOS has been investigated in this paper and the highlights of material and structure parameters have also been detailed. Through adopting a compressively strained $Si_{1-x}Ge_x$ layer for the p-channel and tensile trained Si layer for the n-channel, the CMOSFET realizes the integration of n-MOSFET and p-MOSFET based on the same material layer structure. Moreover, the p^+poly SiGe gate material makes the threshold voltage modifiable by adjusting the Ge content. Nevertheless, this study demonstrates that HCMOS has an excellent matching of threshold voltage and a good matching of transfer characteristic compared with conventional CMOSFETs with the same ratio of width to length. Thus technologies involved in this work have been verified to be applicable and are also expected to be capable of improving the device performance gains.

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