Vol 15 No 4, April 2006
1009-1963/2006/15(04)/0792-06
Chinese Physics
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Improvement of total-dose irradiation hardness of silicon-on-insulator materials by modifying the buried oxide layer with ion implantation*

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(Received 20 June 2005; revised manuscript received 18 October 2005)

The hardening of the buried oxide (BOX) layer of separation by implanted oxygen (SIMOX) silicon-on-insulator (SOI) wafers against total-dose irradiation was investigated by implanting ions into the BOX layers. The tolerance to total-dose irradiation of the BOX layers was characterized by the comparison of the transfer characteristics of SOI NMOS transistors before and after irradiation to a total dose of 2.7 Mrad(SiO_2). The experimental results show that the implantation of silicon ions into the BOX layer can improve the tolerance of the BOX layers to total-dose irradiation. The investigation of the mechanism of the improvement suggests that the deep electron traps introduced by silicon implantation play an important role in the remarkable improvement in radiation hardness of SIMOX SOI wafers.

Keywords: separation-by-implanted-oxygen, silicon-on-insulator, total-dose irradiation effect, ion implantation

PACC: 6180C, 6170T, 7340Q

1. Introduction

Silicon-on-insulator (SOI) technology has been developing rapidly for its advantages in all kinds of radiation environment compared to the bulk silicon technology. However, the buried oxide limits the total dose radiation tolerance of SOI materials. For SIMOX wafers, adjustment of implantation and annealing conditions have been explored to reduce radiation-induced charge trapping. For instance, buried oxides formed by supplemental[1−5] and multiple[6] implantations and annealing show less radiation-induced degradation than buried oxides formed with a single implantation. Both the number of radiation-induced interface traps and the concentration of oxide-trapped charges were significantly reduced for buried oxides formed with multiple implantations.[6] Lowering the oxygen implantation dose and nitrogen implantation have also been suggested as methods for hardening SIMOX buried oxides.[7−10] For the nitrogen annealed buried oxides, the improvement in hardness has been attributed to the formation of an interfacial oxynitride layer.[10] Lowering the implantation dose and energy leads to thinner buried oxides and smaller back-gate voltage shifts. For higher back channel doping concentrations, the back-gate threshold voltages are higher, and larger radiation induced back-gate threshold voltage shifts can be tolerated.

However, the effect of the modification with silicon ions implantation and annealing of BOX layers on the total dose radiation hardness has been little studied. The mechanism of the radiation hardness im-

*Project supported by the National Fund for Distinguished Young Scholars (Grant No 59925205), the Basic Research Program of Shanghai (Grant No 02DJ14069), and the National Natural Science Foundation of China (Grant No 10305018).
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provement by silicon ion implantation still needs more investigation.

In this paper, the BOX layers of SIMOX SOI wafers were modified by silicon ion implantation and subsequent annealing. SOI NMOS transistors were fabricated both on the control SIMOX SOI and modified wafers, and irradiation experiments were performed with the same gate bias to characterize their tolerance to total-dose radiation effects.

2. Experiment

The SOI wafers used in this work were standard SIMOX SOI wafers with the top silicon thickness of 200 nm and the BOX layer thickness of 380 nm. The substrate of the SIMOX SOI wafers were p-type with the resistivity of 15–20Ω·cm. The modification process was performed by implanting silicon ions into the BOX layers. The implantation was carried out with a dose of 1E15 cm^{-2} at the energy of 180 keV. Subsequently, the annealing was carried out in O_2 ambient at 800°C.

NMOS transistors were fabricated on the wafers with channel length of 3μm. The irradiation experiments were performed on these transistors using an ARACOR Model 4100 Semiconductor 10-keV x-ray Irradiator. During the irradiation, these transistors were biased in OFF-state with a drain bias of 5 V and the other electrodes grounded. The total-dose range is from 0.09 to 2.7 Mrad(SiO_2) with the dose rate of 450 rad(SiO_2)/second. All the irradiations were performed at room temperature. Bias was removed from the transistors after irradiation, and I-V measurements were made using the HP4155 semiconductor parameter analyser. Both top-gate and back-gate threshold voltages were measured. The back-gate transistor consists of the bottom of the substrate (gate), the buried oxide, and the source, drain, and body contacts of the top-gate transistor. All measurements were made with a drain bias of 0.1 V.

3. Results and discussion

Pre- and post-irradiation I_{ds}-V_{gs} curves for back-gate transistors with n-channel and irradiated in the OFF-state are shown in Fig.1. It can be seen from Fig.1 (a) and (b) that the I_{ds}-V_{gs} curves shift to the negative along the V_{gs} axis for both modification and control sample, which is resulted from radiation-induced positive charge in the BOX layer. Comparing Fig.1(a) with Fig.1(b), it can be found that the pre-irradiated drain current is larger for control sample than that for the modified sample, and the threshold voltage shifts is much more to the negative at the same total-dose radiation. Moreover, the drain currents in subthreshold region do not increase with the increasing total-dose radiation for modified sample. It illustrates that the modification process can restrain the back channel from introducing leakage current perfectly, and the modified SOI material has advantages over control sample in total dose irradiation.

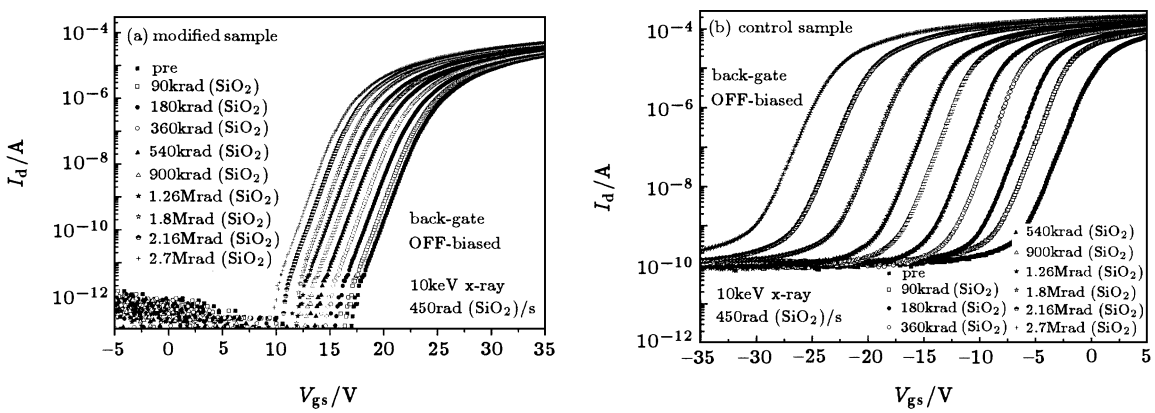


Fig.1. Series of pre- and post-irradiation I-V curves for back gate transistors with n-channel fabricated both on modified (a) and control sample (b). The transistors were irradiated in the OFF-state.

Table 1. Back-gate threshold voltage shifts ($\delta V_{\rm th}$), increase of oxide- and interface-trapped charge density in the BOX ($\delta N_{\rm ot}$) and the interface of BOX/Si ($\delta D_{\rm it}$), respectively, for the transistors fabricated on both control and modified SIMOX wafers at different irradiation total dose.

irradiation total dose	control sample			modified sample		
/rad(SiO_2)	$\delta V_{\rm th}$/V	$\delta N_{\rm ot}$/cm^{-2}	$\delta D_{\rm it}$/ cm^{-2}eV^{-1}	$\delta V_{\rm th}$/V	$\delta N_{\rm ot}$/cm^{-2}	$\delta D_{\rm it}$/ cm^{-2}eV^{-1}
900k	–12.5	5.75×10^{12}	2.21×10^{11}	–5.8	2.57×10^{12}	0
1.26M	–13.6	6.20×10^{12}	4.43×10^{11}	–6.9	3.08×10^{12}	2.21×10^{10}
1.8M	–16.2	7.85×10^{12}	7.08×10^{11}	–8.25	3.67×10^{12}	2.21×10^{10}
2.16M	–19.1	9.40×10^{12}	9.47×10^{11}	–9.45	4.21×10^{12}	3.10×10^{10}
2.7M	–23.5	1.14×10^{13}	9.74×10^{11}	–10.80	4.83×10^{12}	4.87×10^{10}

The shifts of the back-gate threshold voltage ($\delta V_{\rm th}$) for the transistors irradiated with different total doses are shown in Fig.2, which are extracted from the curve of $I_{\rm ds}$-$V_{\rm gs}$ characteristic at a drain current of 1μA in Fig.1. As seen from Fig.2, the back-gate threshold voltage of the transistor fabricated on the modified sample shifts much less than that on the control sample under the same irradiation conditions with the same total dose irradiation. When the irradiation total dose reaches 900 krad (SiO_2), for instance, the $\delta V_{\rm th}$ for the control sample is –12.5 V, while it is only –5.8 V for the modified sample. What's more, when the transistors are irradiated by a total dose of 2.7 Mrad (SiO_2), the $\delta V_{\rm th}$ for the control sample is –23.5 V, while it is only –10.8 V for the modified sample. The detail is shown in Table 1.

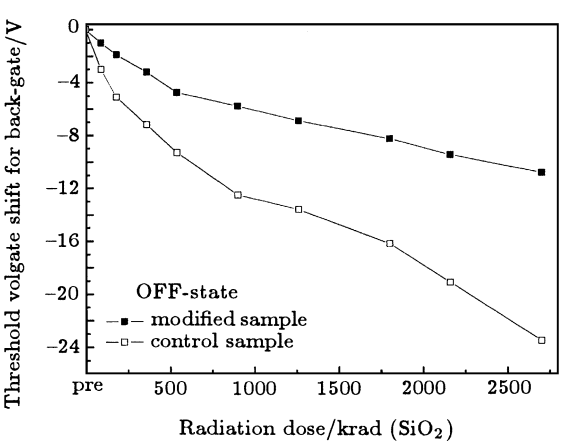


Fig.2. Back-gate threshold voltage shift versus irradiation dose. The back-gate threshold voltage is extracted from $I_{\rm ds}$-$V_{\rm gs}$ characteristics at a drain current of 1μA.

Using the subthreshold I–V technique developed by Winokur and McWhorter[11,12] which separates the oxide- and interface-trapped charges in the back-gate transistors,

$$\delta V_{\rm th} = \delta V_{\rm ot} + \delta V_{\rm it}, \qquad (1)$$

where $\delta V_{\rm ot}$ is the threshold voltage shift introduced by oxide-trapped charges and $\delta V_{\rm it}$ is the threshold voltage shift introduced by interface-trapped charges. As the interface traps are approximately neutral when the Fermi level is at midgap, one can estimate the contribution of the oxide-trapped charge to $\delta V_{\rm th}$ from the change in the midgap voltage.[13] Hence

$$\delta V_{\rm ot} = (V_{\rm mg})_i - (V_{\rm mg})_0, \qquad (2)$$

where the subscripts i and 0 indicate the initial and final values, respectively. From Equation (1) and (2), $\delta V_{\rm it}$ can be extracted. According to the equations $\delta N_{\rm ot}$=$\delta V_{\rm ot} * C_{\rm ox}/q$ and $\delta D_{\rm it} = \delta V_{\rm it} * C_{\rm ox}/q$, the changes in the density of oxide-trapped charge ($\delta N_{\rm ot}$) and interface-trapped charge ($\delta D_{\rm it}$) can be obtained. In the equations, $C_{\rm ox}$ and q denote the capacitance of the BOX layer and the electronic charge, respectively. The calculation results for trapped charges in the transistors are given in Table 1. It can be seen that both the oxide-trapped charge density in the BOX ($\delta N_{\rm ot}$) and the interface-trapped charge density of BOX/Si ($\delta D_{\rm it}$) increase after irradiation for both modified and control sample. The $\delta N_{\rm ot}$ and $\delta D_{\rm it}$ for the modified sample are much less than those for the control sample after total dose irradiation. When the irradiation total dose reaches 2.7Mrad(SiO_2), for example, $\delta N_{\rm ot}$ and $\delta D_{\rm it}$ for the control sample are 1.14×10^{13} cm^{-2} and 9.74×10^{11} cm^{-2}eV^{-1}, respectively, while those for the modified sample are only 4.83×10^{12} cm^{-2} and 4.87×10^{10} cm^{-2}eV^{-1}, respectively. It also suggests that the modification process can restrict the increase of oxide- and interface-trap charge in SIMOX SOI transistors, which will improve the tolerance of the SIMOX wafers to total dose radiation.

The pre- and post-irradiation $I_{\rm ds}$-$V_{\rm gs}$ characteristics for top-gate transistors are presented in Fig.3. The leakage current in the subthreshold region for the modified sample maintains at the level of 1–10 pA after the irradiation total dose as high as 2.7 Mrad(SiO_2), while the leakage current for the control sample increases sharply to an unacceptable level after only a

low irradiation total dose of 180 krad(SiO_2). On the other hand, negative shift of the I_{ds}-V_{gs} curves is much smaller for the modified sample than that for the control sample. The relation of top-gate threshold voltage shift versus irradiation dose is presented in Fig.4. The results prove that, for the modified sample, the radiation induced leakage currents, both between field oxide and the transistor and in the back channel, are too small to influence the characteristics of the top-gate channel obviously. It further suggests that the modification process can improve the tolerance of the SIMOX wafers to total dose radiation.

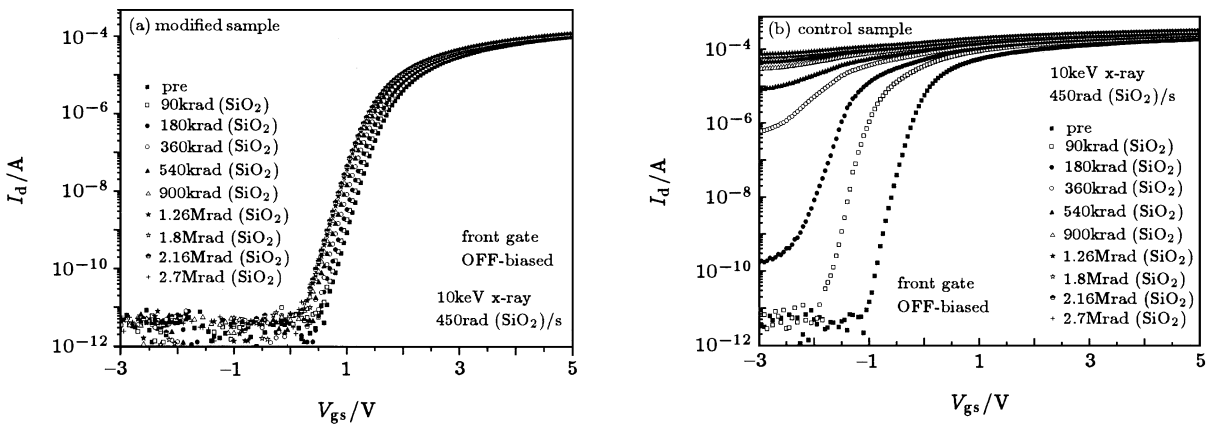


Fig.3. Series of pre- and post-irradiation I-V curves for top-gate transistors with n-channel fabricated both on modified (a) and control sample (b). The transistors were irradiated in the OFF-state.

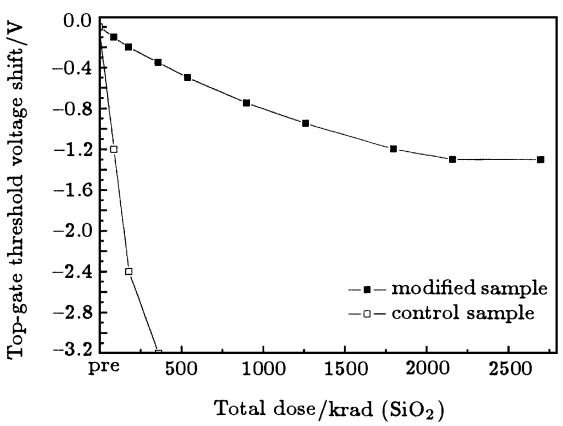


Fig.4. Top-gate threshold voltage shift versus radiation dose. The data of threshold voltage is extracted from I_{ds}-V_{gs} characteristics at a drain current of 1μA.

The results of I_{ds}–V_{gs} characteristics for back- and top-gate convincingly illustrate the remarkable improvement produced by the modification. The mechanism of the improvement is discussed in the following.

It is well known that, during the fabrication of SIMOX wafers, high temperature annealing causes oxygen to out-diffuse from the buried oxide, leaving behind numerous oxide defects.[14,15] These defects can lead to enhanced radiation-induced charge trapping. It has also been shown that implanting damage can cause significant radiation-induced degradation in the gate and field oxides.[16–18] Thus, it is natural to expect that the very high-fluence implantations used to fabricate SIMOX substrates may cause numerous implantation-related defects that might result in enhanced radiation-induced charge trapping in the buried oxide. According to previous studies, the E' defect-centre, which is a hole-trap with a high capture cross-section, plays a significant role in BOX charge trapping.[14–19] Previous work has also shown that almost up to 100% of the radiation-generated holes that escaped initial recombination are trapped in the bulk of the oxide at deep trap sites close to their point of origin. Once trapped, some of the holes are slowly neutralized by thermal emission of electrons from the oxide valence band at room temperature.[20–24] In addition to the hole-trapping, electrons can also be trapped throughout the bulk of the BOX in shallow levels.[20,25] Most of these shallow-trapped electrons are thermally detrapped within 1s after a pulse of radiation. After the electrons are detrapped, the net charge is dominated by a high concentration of trapped holes, causing negative threshold voltage shifts of the back-gate transistors, as is shown in Fig.1(a), Fig.1(b), and Fig.2. Similarly, the trapped holes in the gate oxide will cause threshold voltage of the top-gate transistors to shift to the negative, as shown in Fig.3 and Fig.4.

The modification conditions could also influence the properties of the SOI devices.[26] For the implanta-

tion energy, we chose 180 keV to ensure that the silicon ions are implanted into the BOX layer. On one hand, if the dose of silicon ions implanted into the SIMOX SOI wafer was too high, e.g. for the dose higher than $1\times10^{17}\,\mathrm{cm}^{-2}$, a very large number of defects would be created in the top silicon and BOX layer of the wafer, which could not be recovered during the related annealing. These defects could badly impair the original properties of the devices fabricated on the materials, and reduce their radiation tolerance. On the other hand, if the implantation dose was too low, e.g. for the dose below $5\times10^{10}\,\mathrm{cm}^{-2}$, the radiation hardening modification does not work. So we chose the implantation dose of $1\times10^{15}\,\mathrm{cm}^{-2}$, at a middle level. The detailed mechanism of the rad-hard from this technique is as follows.

The modification of the BOX layers with a proper dose of silicon ion implantation can create a large number of electron traps deeply within the BOX layer to compensate the positive trapped charge.[27,28] According to Nicklaw,[26] when a proper dose of silicon ions are implanted into the BOX layers of the SIMOX wafers, a number of silicon nanocrystals (clusters) will be formed and embedded in the SiO_2 matrix after a proper annealing. These silicon nanocrystals, being structural defects introduced by silicon ion implantation, have ground and excited energy states that lie within the energy gap of amorphous SiO_2. Theoretically, the formations of the defects are mainly $\equiv$Si—O—Si—Si$\equiv$, $\equiv$Si—Si—Si$\equiv$, the $\equiv$Si—O—O—Si$\equiv$ with $\equiv$Si—Si—Si$\equiv$ and the $OSi_2 \equiv$ Si.[25] These artifact defects are deep electron traps which can capture electrons deeply in the BOX layers during the irradiation to compensate the positive charge trapping. As a result, the threshold voltage of the back-gate transistors fabricated on the modified samples have much less negative shifts than that on the control sample. A larger threshold voltage makes inversion of the silicon near the back channel more difficult, which prevents the formation of the conducting back channel. Thus, the leakage current from back-channel can still be very small after a very high irradiation dose of 2.7 Mrad(SiO_2), as is shown both in Fig.1 and Fig.3.

4. Conclusion

In this work, radiation hardness improvement of the BOX layers in SIMOX SOI material was successfully achieved by silicon ions implanted into the BOX layers. The experimental results show that the implantation of silicon ions can improve the tolerance of the BOX layers to total-dose irradiation remarkably. The deep electron-traps introduced by silicon implantation play an important role for the remarkable improvement in radiation hardness of SIMOX SOI wafers. The hardening process of silicon ions implanted into BOX layers will be a promising hardening method for SOI material and devices.

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