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# Investigation of the characteristics of GIDL current in 90nm CMOS technology*

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A specially designed experiment is performed for investigating gate-induced drain leakage (GIDL) current in 90nm CMOS technology using lightly-doped drain (LDD) NMOSFET. This paper shows that the drain bias $V_{\rm D}$ has a strong effect on GIDL current as compared with the gate bias $V_{\rm G}$ at the same drain–gate voltage $V_{\rm DG}$. It is found that the difference between $I_{\rm D}$ in the off-state $I_{\rm D}-V_{\rm G}$ characteristics and the corresponding one in the off-state $I_{\rm D}-V_{\rm D}$ characteristics, which is defined as $I_{\rm DIFF}$, versus $V_{\rm DG}$ shows a peak. The difference between the influences of $V_{\rm D}$ and $V_{\rm G}$ on GIDL current is shown quantitatively by $I_{\rm DIFF}$, especially in 90nm scale. The difference is due to different hole tunnellings. Furthermore, the maximum $I_{\rm DIFF}(I_{\rm DIFF,MAX})$ varies linearly with $V_{\rm DG}$ in logarithmic coordinates and also $V_{\rm DG}$ at $I_{\rm DIFF,MAX}$ with $V_{\rm F}$ which is the characteristic voltage of $I_{\rm DIFF}$. The relations are studied and some related expressions are given.

**Keywords:** GIDL, 90nm CMOS technology, band-to-band tunnelling
**PACC:** 7340G, 7300, 7360J, 7340Q

## 1. Introduction

As MOSFETs are scaled down to the ultra deep-sub-micron region, many problems are encountered, such as punch-through and short-channel effects.[1] Among these problems, the gate-induced drain leakage (GIDL) effect, which is attributed to band-to-band tunnelling, has become a crucial reliability issue. It constitutes a serious constraint in scaled down CMOS devices for dynamic random-access memory (DRAM) and/or electrically erasable programmable read only memory (EEPROM) applications.[2] GIDL has reportedly become one of the most limiting factors on advanced double-oxide devices and one major factor determining the data retention time of 80nm recess channel array transistor (RCAT) technology.[3,4] Although efforts have been made in the study of GIDL, it is far from a complete understanding of the phenomena associated with GIDL. In various studies of GIDL, a dominant GIDL current model is widely used. It is given by[2,5]

$$I_{\rm D} = A \times E_{\rm S} \times \exp(-B/E_{\rm S}), \tag{1}$$

$$E_{\rm S} = (V_{\rm DG} - 1.2)/3T_{\rm OX}, \tag{2}$$

where $I_{\rm D}$ is the GIDL current, $E_{\rm S}$ is the vertical electric field at silicon surface in the gate to drain overlap region, and $T_{\rm OX}$ is the oxide thickness. A is a pre-exponential constant and $B$=21.3MV/cm. It is shown from Eq.(1) that the GIDL current $I_{\rm D}$ depends on drain–gate voltage $V_{\rm DG}$ only. Since $V_{\rm DG} = V_{\rm D} + |V_{\rm G}|$, $V_{\rm D}$ and $V_{\rm G}$ have the same effect on $V_{\rm DG}$ and they are symmetrical in mathematics. In this way the dominant model fails to interpret the difference between the influences of $V_{\rm D}$ and $V_{\rm G}$ on GIDL current. As MOSFET is scaled down to 90nm level, the difference of the influences increases greatly and the GIDL current no longer keeps constant at an invariable $V_{\rm DG}$. This deviation appears just because of the difference between the influences of $V_{\rm D}$ and $V_{\rm G}$ on GIDL current. Obviously, the difference of the influences has reduced

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the accuracy of the dominant model markedly (Eq.(1)) in the calculation of the GIDL current. So the investigation of this kind of difference is helpful to establish a more accurate GIDL current model. However, this problem has not received enough attention by far.

In this paper, it is our intention to investigate the difference between the influences of $V_D$ and $V_G$ on GIDL current at the same $V_{DG}$ in 90nm CMOS technology using lightly-doped drain (LDD) NMOSFET. The related mechanisms and some expressions are presented in detail.

## 2. Device and experiments

The device used in this paper is LDD NMOSFET fabricated by 90nm CMOS technology. The oxide is about 1.4nm thick with decoupled plasma nitridation (DPN) process. The LDD NMOSFET is a surface device with an $N^+$ poly-Si gate. The channel length is 0.13$\mu$m and its width is 3$\mu$m. All measurements are carried out under light-tight and electrically-shielded condition at room temperature, using an HP 4156B precision semiconductor parameter analyser.

## 3. Results and discussion

Figures 1(a) and 1(b) present the $I_D - V_G$ characteristics and the $I_D - V_D$ characteristics in off-state respectively. Figures 1(c) and 1(d) show the variation of $I_D$ with $V_{DG}$ extracted from Figs.1(a) and 1(b) respectively. In Fig.1(c) $I_D$ increases with increasing $V_D$. However, it decreases with increasing $|V_G|$ in Fig.1(d).

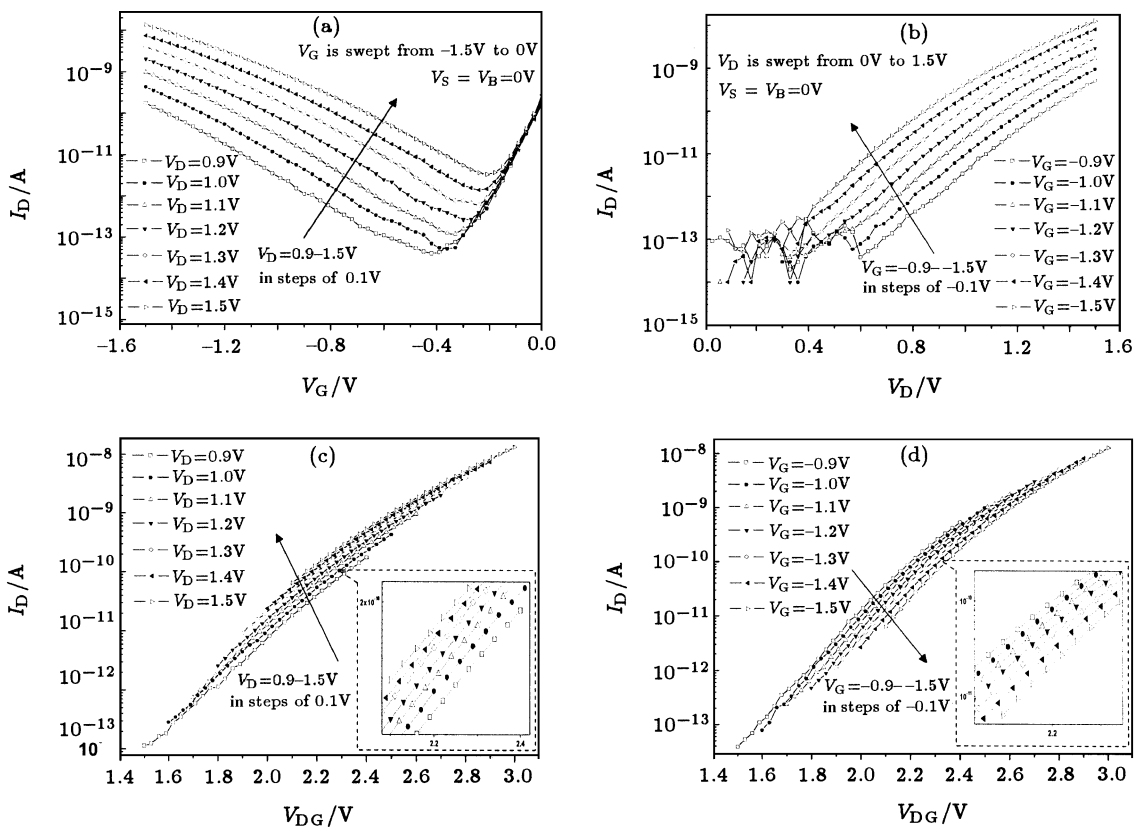



**Fig.1.** (a) and (b) $I_D$ as functions of $V_G$ and $V_D$ in off-state respectively. (c) and (d) $I_D$ as a function of $V_{DG}$ extracted from Fig.1(a) and 1(b) respectively.

Figure 2 shows the comparison between $I_D$ measured at $V_D$=1.4V in Fig.1(c) and $I_D$ measured at $V_G$=–1.4V in Fig.1(d) with the same $V_{DG}$. When $V_{DG}$ <2.8V, $I_D$ at $V_D$=1.4V is larger than that at $V_G$=–1.4V, and when $V_{DG}$ >2.8V, the latter is larger than the former. The comparisons between $I_D$ at other $V_D$ in Fig.1(c) and $I_D$ at the corresponding $V_G(|V_G|=V_D)$ in Fig.1(d) are made also by the above method. It is found that the $V_D/V_{DG}$ at every point in the upper $I_D$ curve always has $V_D/V_{DG} > 1/2$, and the $|V_G|/V_{DG}$ for the lower curve always satisfies $|V_G|/V_{DG} > 1/2$. Hence, it is concluded that $V_D$ has a stronger effect on GIDL current than $V_G$ does.

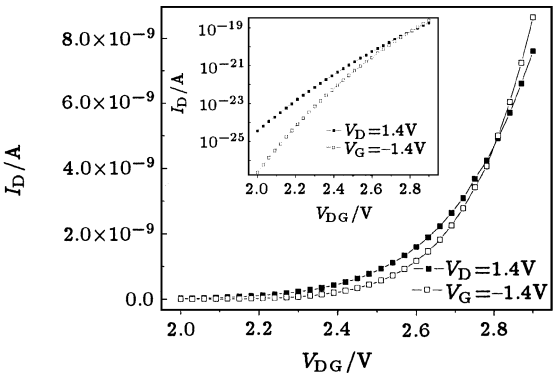



**Fig.2.** Comparison of $I_{\rm D}$ measured at $V_{\rm D}$=1.4V in Fig.1. (c) with $I_{\rm D}$ measured at $V_{\rm G}$=–1.4V in Fig.1(d) with the same $V_{\rm DG}$.

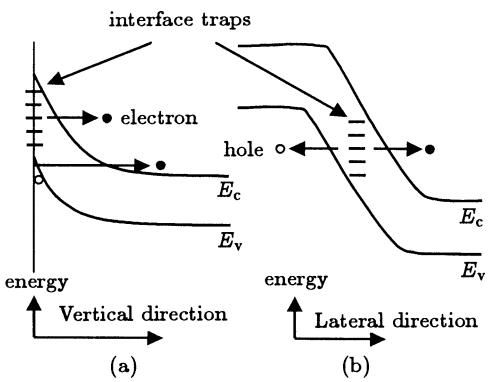



**Fig.3.** Band diagrams of NMOSFET in the gate-to-LDD overlap region (a)in the vertical direction and (b) in the lateral direction.

This phenomenon can be explained as follows: there exist intrinsic interface states in the fresh device and then the tunnelling assisted by traps (band–trap–band tunnelling) takes place with band-to-band tunnelling simultaneously. The density of this intrinsic interface states is around $10^{10}{\rm cm}^{-2}$, so the band–trap–band tunnelling cannot be ignored. Figures 3(a) and 3(b) show the band diagram of NMOSFET around the gate-to-LDD overlap region in the vertical direction and in the lateral direction respectively. In the vertical direction, electrons tunnel into the conduction band from the valence band or from traps in the gap due to the band bending. Meanwhile, in this direction the energy band of Si terminates at the top surface of bulk Si and therefore the hole tunnelling from traps to valence band is forbidden. In the lateral direction, holes tunnel from traps to the valence band while electrons tunnel into the valence band. In balance electron tunnelling is assisted by the whole field $\varepsilon$ induced by $V_{\rm DG}$, and hole tunnelling is assisted only by the lateral field $\varepsilon_{\rm L}$ induced by $V_{\rm D}$. The time constants for the electron and hole tunnelling ($\tau_{\rm e}$, $\tau_{\rm h}$) are formulated as follows:[6]

$$\tau_{\rm e} = \tau_{0\rm c}\exp[8\pi/h(2m_{\rm e})^{1/2}(E_{\rm c} - E_{\rm t})^{3/2}/3q\varepsilon], \quad (3)$$

$$\tau_{\rm h} = \tau_{0\rm v}\exp[8\pi/h(2m_{\rm h})^{1/2}(E_{\rm t} - E_{\rm v})^{3/2}/3q\varepsilon_{\rm L}], \quad (4)$$

where $\tau_{0\rm c}$ and $\tau_{0\rm v}$ are effective transit times in the conduction band and in the valance band respectively. $m_{\rm e}$ and $m_{\rm h}$ are effective masses for electrons and holes, while $E_{\rm v}$ and $E_{\rm c}$ are energy levels of valence band and conduction band respectively. $E_{\rm t}$ is the energy level of interface states.

From Eqs.(3) and (4), we can obtain expressions of the rates for electron and hole tunnelling ($r_{\rm e}$ and $r_{\rm h}$). They are given by:

$$r_{\rm e} = 1/\{\tau_{0\rm c}\exp[-8\pi/h(2m_{\rm e})^{1/2}(E_{\rm c} - E_{\rm t})^{3/2}/3q\varepsilon]\}, \quad (5)$$

$$r_{\rm h} = 1/\{\tau_{0\rm v}\exp[-8\pi/h(2m_{\rm h})^{1/2}(E_{\rm t} - E_{\rm v})^{3/2}/3q\varepsilon_{\rm L}]\}, \quad (6)$$

The lateral field $\varepsilon_{\rm L}$ is induced by $V_{\rm D}$, and so $V_{\rm D}$ determines the hole tunnelling in the direction parallel to the $Si/SiO_2$interface. Since the MOS device's channel length is around 90nm, the lateral field $\varepsilon_{\rm L}$ is so strong that the hole tunnelling is enhanced greatly. At the same $V_{\rm DG}$, the electron tunnelling remains constant due to the same rate of electron tunnelling ($r_{\rm e}$). In this case, the larger the $V_{\rm D}/V_{\rm DG}$, the larger the rate of hole tunnelling ($r_{\rm h}$), and therefore the whole tunnelling becomes stronger. On the contrary, the larger the $|V_{\rm G}|/V_{\rm DG}$, the smaller the $r_{\rm h}$, and the whole tunnelling becomes weaker. From the above analysis, $V_{\rm D}$ influences the GIDL current much stronger than $V_{\rm G}$.

For further clearness, $I_{\rm DIFF}$ is defined as below:

$$I_{\rm DIFF}|_{V_{\rm F}=c_1,V_{\rm DG}=c_2} = I_{\rm D}|_{V_{\rm D}=c_1,V_{\rm DG}=c_2} - I_{\rm D}\,|_{|V_{\rm G}|=c_1,V_{\rm DG}=c_2}\,, \quad (7)$$

where $c_1$ and $c_2$ are both given constants. $V_{\rm F}$ is the characteristic voltage of $I_{\rm DIFF}$. Figure 4 shows $I_{\rm DIFF}$ vs $V_{\rm DG}$ at different $V_{\rm F}$ values. In Fig.4 $I_{\rm DIFF}$ rises with increasing $V_{\rm F}$ from 0.9 to 1.5V, and appears obviously in the shape of peaks.

$I_{\rm DIFF}$ figures out the difference between the influences of $V_{\rm D}$ and $V_{\rm G}$ on GIDL current quantitatively. $I_{\rm DIFF}$ shows further the difference of the hole tunnelling current at fixed $V_{\rm D}$ from the hole tunnelling current at fixed $V_{\rm G}$, while $V_{\rm D}/V_{\rm DG} = |V_{\rm G}|/V_{\rm DG}$ at the same $V_{\rm DG}$. Based on the above argument, $I_{\rm DIFF,MAX}$, the peak point, shows the maximum difference between the two hole tunnelling currents under the above conditions.

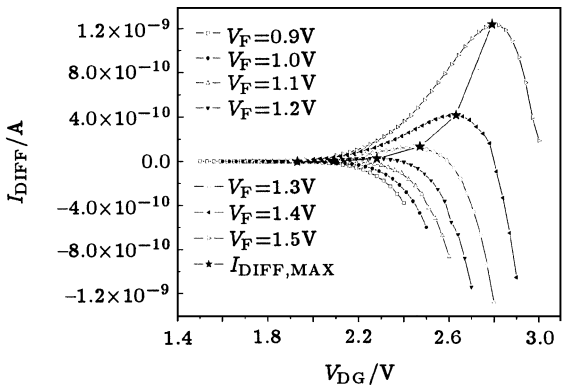



**Fig.4.** $I_{DIFF}$ vs $V_{DG}$ at $V_F$=0.9–1.5V in steps of 0.1V.

Figure 5(a) shows that $I_{DIFF,MAX}$ varies linearly with $V_{DG}$ in semi-logarithmic coordinates. Figure 5(b) shows that $V_{DG}(I_{DIFF,MAX})$ also varies linearly with $V_F$. The fitting expressions are given by:

$$I_{DIFF,MAX} = \exp(a_1 + a_2 \times V_{DG}), \quad (8)$$

$$V_{DG}(I_{DIFF,MAX}) = b_1 + b_2 \times V_F, \quad (9)$$

where $a_1$, $a_2$, $b_1$, $b_2$ are the coefficients. $V_{DG}$ $(I_{DIFF,MAX})$ is the very $V_{DG}$ at $I_{DIFF,MAX}$. To the device used in this work, the coefficients are given as $a_1$ =–42, $a_2$=7.79, $b_1$=0.18, $b_2$=1.75.

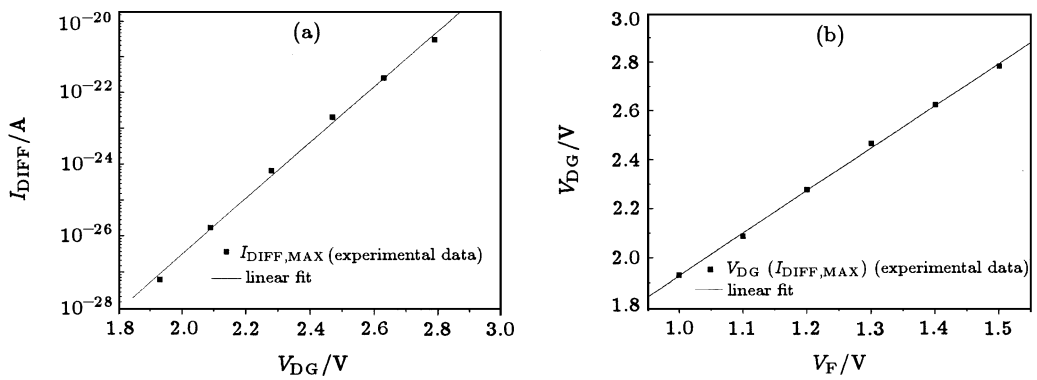



**Fig.5.** Relations between: (a) $I_{DIFF}$ and $V_{DG}$ $(I_{DIFF,MAX})$ and (b) $V_{DG}$ $(I_{DIFF,MAX})$ and $V_F$.

The above law can also be used for the other devices (different W/L) with 1.4nm-thick gate dielectric. These relations among $I_{DIFF,MAX}$, $V_{DG}$ and $V_F$ are shown in Table 1. It is found that $a_2$ is about 8 and $b_2$ is about 1.8 for these devices.

**Table 1.**

| $W/L$ | $I_{DIFF,MAX}$ | $V_{DG}(I_{DIFF,MAX})$ |
|---|---|---|
| 3$\mu$m /0.10$\mu$m | exp(–41.55+7.64$V_{DG}$) | –0.02+1.90$V_F$ |
| 5$\mu$m /0.10$\mu$m | exp(–44.12+8.89$V_{DG}$) | 0.338+1.86$V_F$ |

# 4. Conclusion

The GIDL current remains no longer the same while $V_{DG}$ is invariable in 90nm CMOS technology with LDD NMOSFET. This situation occurs just because of the difference between the influences of $V_D$ and $V_G$ on GIDL current. In this paper, this kind of difference has been investigated in detail. It is found that $V_D$ has a strong effect on GIDL current as compared with $V_G$, and the curve $I_{DIFF}$ vs $V_{DG}$ shows a peak. $I_{DIFF}$ can indicate quantitatively the difference between the influences of $V_D$ and $V_G$ on GIDL current due to the different hole tunnellings. Moreover, $I_{DIFF,MAX}$ varies linearly with $V_{DG}$ in semi-logarithmic coordinates, and $V_{DG}(I_{DIFF,MAX})$ also varies linearly with the characteristic voltage $V_F$.

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