Vol 15 No 11, November 2006
1009-1963/2006/15(11)/2751-05

Chinese Physics

© 2006 Chin. Phys. Soc.
and IOP Publishing Ltd

Silicon-on-nothing MOSFETs fabricated with hydrogen and helium co-implantation*

Bu Wei-Hai(卜伟海)[a], Huang Ru(黄 如)[a]†, Li Ming(黎 明)[a], Tian Yu(田 豫)[a], Wu Da-Ke(吴大可)[a], Chan Man-Sun(陈文新)[b], and Wang Yang-Yuan(王阳元)[a]

[a] *Institute of Microelectronics, Peking University, Beijing* 100871, *China*

[b] *Department of Electrical & Electronic Engineering, Hong Kong University of Science & Technology, Hong Kong, China*

(Received 6 April 2006; revised manuscript received 26 June 2006)

In this paper, a method to fabricate Silicon-on-Nothing (SON) MOSFETs using H^+ and He^+ co-implantation is presented. The technique is compatible with conventional CMOS technology and its feasibility has been experimentally demonstrated. SON MOSFETs with 50nm gate length have been fabricated. Compared with the corresponding bulk MOSFETs, the SON MOSFETs show higher on current, reduced leakage current and lower subthreshold slope.

Keywords: Silicon-on-Insulator (SOI), SON, hydrogen and helium co-implantation
PACC: 7850G, 7340Q, 6180J

1. Introduction

As the channel length of MOSFETs is reduced to below 100nm, the short channel effects (SCE) become very serious which prevents the further scaling of devices to the decanano-metric dimensions. Silicon-on-Nothing (SON) MOSFET has been proposed as a possible alternative structure for sub-50nm MOSFETs.[1,2] Some experimentally fabricated SON MOSFETs[3−5] have demonstrated $I-V$ characteristics that are strongly immune to SCE when compared with other structures. However, most methods used to fabricate SON MOSFETs required some complicated processing technique such as selective epitaxy[3,4] and empty space in silicon,[5] making them impractical for large scale device fabrication.

Fichter *et al* have reported that bubbles can be formed in the silicon substrate by implantation of helium at high dose and subsequent annealing in nitrogen ambient.[6] Using a similar approach, Agarwal *et al* have observed that hydrogen and helium co-implantation results in a reduction of the total ion implantation dose necessary for formation of void layer,[7−9] While the properties of silicon with void formed by helium bubbles have been studied in detail, no transistors characteristics based on such material is reported. In this paper, we propose to use the top silicon film on the void layer to fabricate SON MOSFETs with the conventional CMOS technology and study the characteristics of the fabricated devices.

2. Device Structure and Fabrication

The schematic cross-section of a SON MOSFET is shown in Fig.1 which possesses a bubble void layer underneath the MOSFET. As the void region consists of no solid material, it can be considered as 'nothing'. The device fabrication starts with the formation of the void layer.

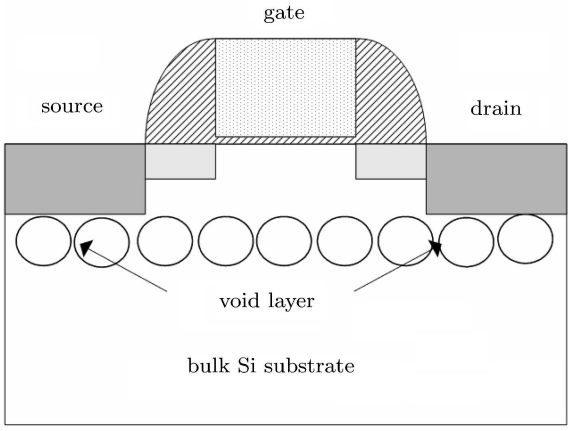


Fig.1. The schematic cross sectional view of a SON MOSFET.

*Project supported by National Natural Science Foundation of China (Grant No 90207004) and State Key Fundamental Research Project of China.

†Corresponding author. E-mail: huangr@ime.pku.edu.cn

In this work, a (100) oriented p-type bulk silicon wafer with resistivity of $20-40\Omega\cdot$ cm was used as substrate. The key steps in device fabrication are shown in Fig.2.

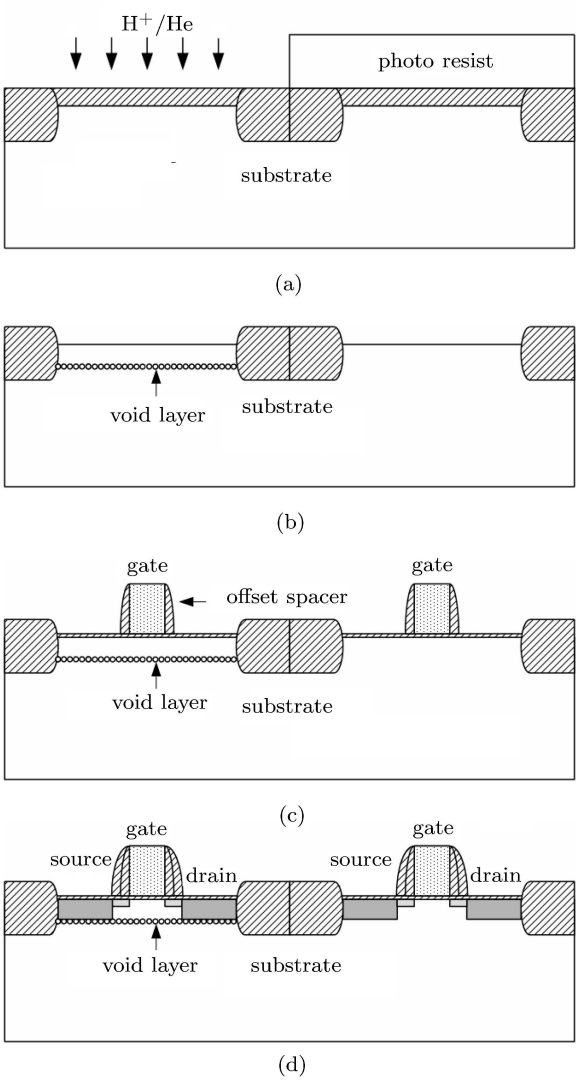


Fig.2. Key fabrication steps of the n-channel SON transistor and bulk silicon transistor on the same wafer. (a) H^+/He^+ co-implanting to the exposed region, (b) void layer formation after annealing, (c) gate stack and off-set spacer formation, and (d) source and drain formation.

After defining the active region of a MOSFET with local oxidation of silicon, the active regions covered with 200nm low-temperature-oxide (LTO) were exposed and H^+/He^+ were implanted to the exposed region where the void layer was to be formed as shown in Fig.2(a). The implantation was performed at room temperature with H^+/He^+ at energy of 40 keV. The doses of H^+ and He^+ were $1\times10^{15}/cm^2$ and $5\times10^{16}/cm^2$ respectively. After the implantation, the substrate was annealed for 30 minutes at 1180 C° in N_2. After the annealing, a dense void layer was formed beneath the surface of the substrate as shown in Fig.2(b). The depth of the void layer in the substrate was determined by the H^+/He^+ implantation energy and the pattern of the photoresist. In this work, the depth was targeted to be around 80nm. A transmission electron microscope (TEM) image of the formed SON structure is shown in Fig.3.

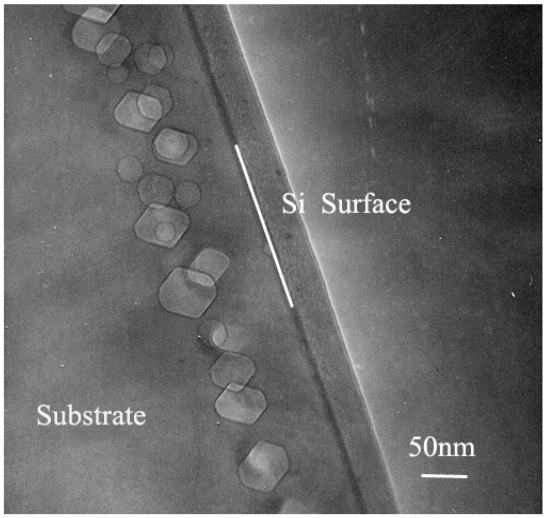
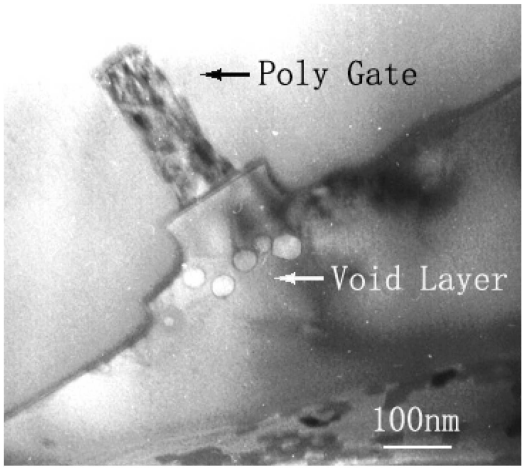


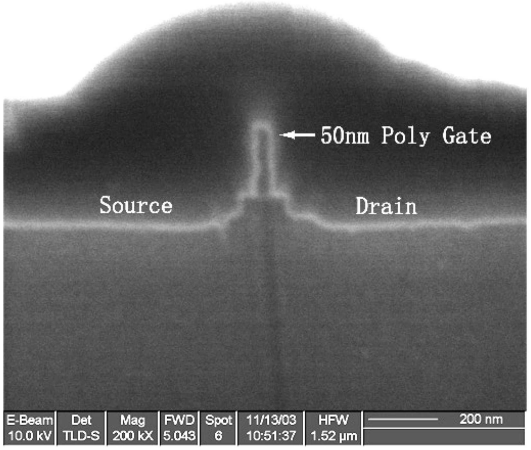
Fig.3. TEM image of SON material samples implanted with H^+/He^+ and subsequently annealed in N_2.

The formation of the void layer using the H^+/He^+ implantation method did not affect the surface topology, which was advantageous in comparison with other reported process for subsequent transistor fabrication steps. The SON MOSFETs were fabricated using conventional CMOS process. Boron implantation with the dose of $2\times10^{13}/cm^2$ and the energy of 35keV was used for threshold voltage adjustment. The gate oxide thickness used was 5nm with thermally grown oxide. The 50nm gate length was defined by electron-beam lithography. After the etching of the poly-gate, 12nm oxide was deposited and etched to form off-set spacer for the source and drain extension implantation as shown in Fig.2(c). 120 nm oxide was deposited and etched to form gate spacer for the deep source/drain region as shown in Fig.2(d). After source and drain implantation, back-end steps including contacts opening and metallization were performed to complete the process. The final structure is shown in the SEM and TEM image in Fig.4. The gate length as defined by the polysilicon width is measured to be 50nm. Together with the SON MOSFET fabrication, bulk MOSFETs

are fabricated for comparison with exactly the same process steps but without the void formation by the H^+/He^+ implant.



(a)



(b)

Fig.4. Cross-sectional images of SON MOSFET, (a) TEM image of SON structure, and (b) SEM image of 50nm gate length SON MOSFET (the void layer cannot be detected by SEM method).

3. Characterization results and discussion

The turn-on characteristics of a n-channel SON MOSFET are shown in Fig.5(a) together with the bulk MOSFETs. It is observed that the SON MOSFETs exhibit higher on current and lower off current and about one order higher on/off current ratio than the bulk MOSFETs, especially when the drain voltage is high ($V_{ds} = 1.0$ V).

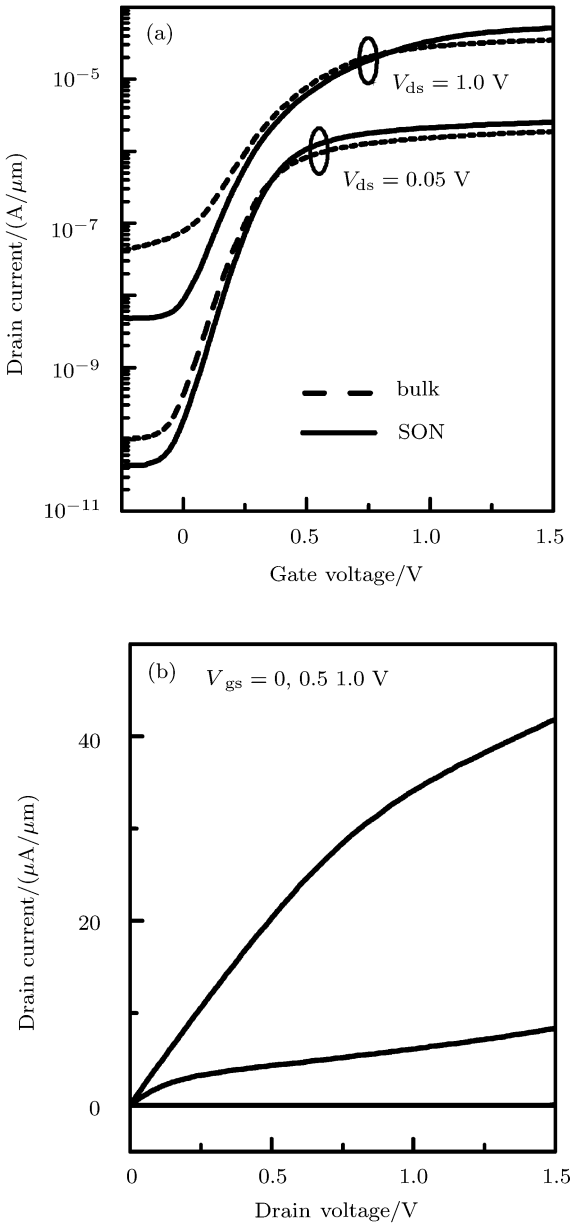


Fig.5. (a) Transfer characteristics of 50nm gate length SON nMOSFET and the corresponding bulk silicon nMOSFET. (b) Output characteristics of 50nm gate length SON nMOSFET.

The advantages of lower off current and higher on/off current ratio in the SON MOSFETs are due to the void layer which reduces the leakage path between source and drain and does not influence the on current simultaneously. Improved subthreshold slope of 94mV/dec is achieved with the SON structure when it is compared with the 99mV/dec of bulk MOSFETs. The output characteristic of the SON MOSFET is shown in Fig.5(b), indicating that a reasonable characteristic with sufficient breakdown voltage is achieved.

Furthermore, the void layer formed by discrete voids in the partially depleted SON transistors brings some other advantages. The discrete void layer makes such silicon-on-insulator-like devices free from self-heating. For SON device with higher scalability, silicon film can be relatively thick. Simulated results show that the device can achieve higher tolerance to small variation of the void location or size in Fig.6.[10]

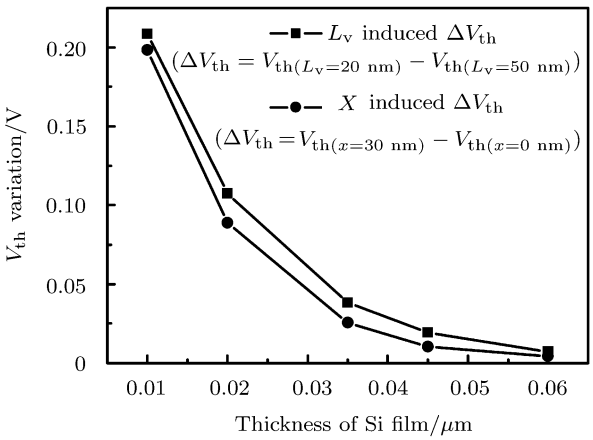


Fig.6. The dependence of threshold voltage shift induced by L_v and X on the thickness of silicon film. L_v and X means the void size variation and location variation respectively. $X = 0$ is defined when the centre point of one void is right under the centre point of channel.

To study the SCE, the threshold voltage (V_{th}) with different gate length is shown in Fig.7. The V_{th} is extracted with linear extrapolation at low drain voltage of 0.05 V. As inherent from the Silicon-on-Insulator (SOI) structure, the SON MOSFET shows a smaller V_{th} roll-off in comparison with that of the bulk MOSFETs. It indicates that the void layer can effectively reduce the two-dimensional electric field coupling from the drain to the channel through the buried layer. This advantage is achieved from the lower dielectric constant void layer, and it can be seen as a vacuum layer if the voids grow to a single layer. Actually, the improvement of V_{th} roll-off due to the void layer in SON MOSFET is more effective than in SOI MOSFET, which is proved with simulation by Integrated-Simulation-Environment (ISE), as shown in Fig.8.[11] The difference of performance of SON device between Fig.7 and Fig.8 is because the parameters of simulated device has been optimized and ignored some parasitic effects such as source and drain contact resistance.

One concern on the device performance using the high dose ion implantation is the quality of top silicon film, which may reduce the electronic mobility. No obvious defects are seen in the top silicon film as shown in Fig.3. Furthermore, no mobility degradation due to the high dose ion implantation is observed as shown from the measured data in Fig.9. The mobility comparison demonstrates that H^+/He^+ co-implantation does not induce the mobility degradation. It is because that H^+ and He^+ are both light ions and their co-implantation does not bring effective damages to the silicon film. Even there are some light damages from co-implantation, they will be recovered during the post annealing. So the implanted silicon film exhibits relatively good quality for device fabrication.

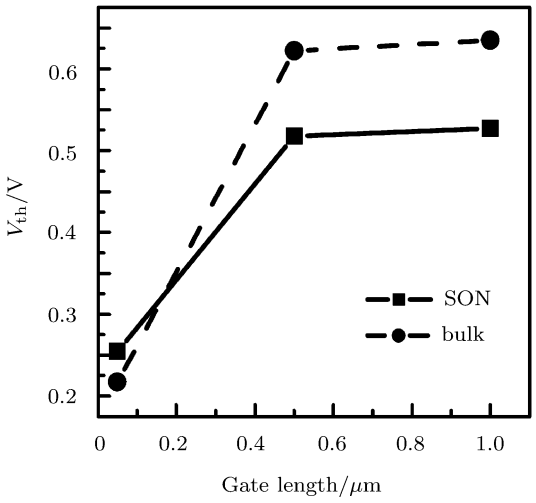


Fig.7. Threshold voltage with difference gate length of the SON transistors and the corresponding bulk transistors.

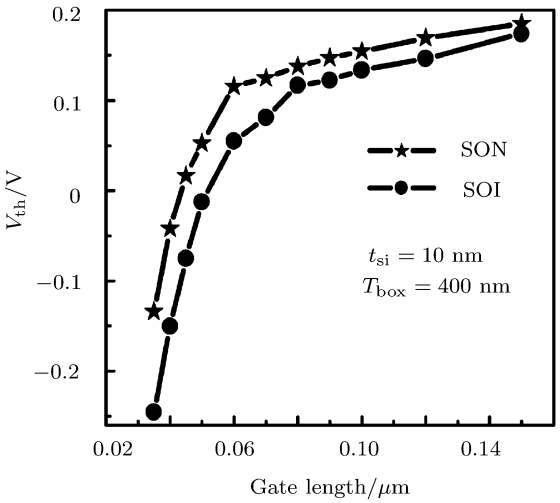


Fig.8. The simulation results of threshold voltage as a function of the gate length for SON MOSFETs and ultra-thin-body SOI MOSFETs.

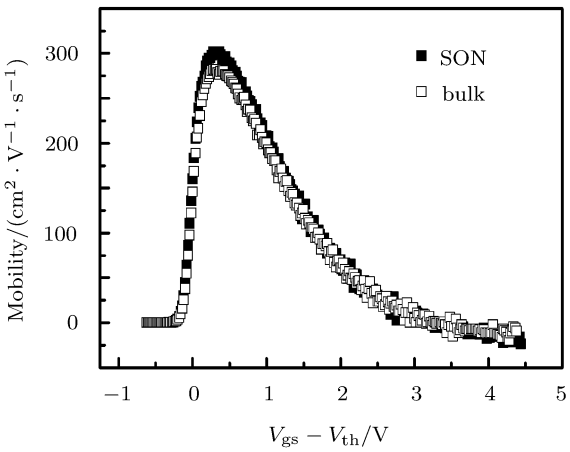


Fig.9. Comparison of electron mobility in the inversion layer of the SON MOSFET and the corresponding bulk silicon MOSFET.

4. Conclusion

In this work, we have successfully developed a process to fabricate SON MOSFETs by using H^+ and He^+ co-implantation. 50nm n-channel SON MOSFETs have been fabricated with the process. Experimental results show that the SON MOSFETs can exhibit higher on current, lower off-leakage current, higher on/off current ratio, and better SCE immunity. The mobility of the device has also been measured and no degradation due to the high dose implantation was observed.

Acknowledgments

The authors would like to thank Chen B Q and the Microfabrication Laboratory staff of Peking University for their support in device fabrication and would also like to thank Sun L for fruitful discussions.

References

[1] Koh R 1999 *Jpn. J. Appl. Phys.* **38** 2294
[2] Jurczak M, Skotnicki T, Paoli M, Tormen B, Martins J, Regolini J L, Dutartre D, Ribot P, Lenoble D, Pantel R and Monfray S 2000 *IEEE Trans. Electron Devices* **47** 2179
[3] Monfray S, Skotnicki T, Morand Y, Descombes S, Paoli M, Ribot P, Talbot A, Dutartre D, Leverd F, Lefriec Y, Pantel R, Haond M, Renaud D, Nier M E, Vizioz C and Louis D 2001 *IEDM* p645
[4] Monfray S, Skotnicki T, Tavel B, Morand Y, Descombes S, Talbot A, Dutartre D, Jenny C, Mazoyer P, Palla R, Leverd F, Le Friec Y, Pantel R, Haond M, Charbuillet C, Vizioz C, Louis D and Buffet N 2002 *IEDM* p263
[5] Sato T, Nii H, Hatano M, Takenaka K, Hayashi H, Ishigo K, Hirano T, Ida K, Aok Ni, Ohguto T, Ino K, Mizushima I and Tsunashima T 2001 *IEDM* p809
[6] Fichtner P F P, Kaschny J R, Yankov R A, Mücklich A, Kreißig U and Skorupa W 1997 *Appl. Phys. Lett.* **70** 732
[7] Agarwal A, Haynes T E, Venezia V C, Holland O W and Eaglesham D J 1998 *Appl. Phys. Lett.* **72** 1086
[8] Luo Z, Lin X Y, Lin S H, Yu C Y, Lin K X, Yu Y P and Tan W F 2003 *Chin. Phys.* **12** 169
[9] Li Z H, Liu H X and Hao Y 2006 *Chin. Phys.* **15** 833
[10] Wu D K, Tian Y, Bu W H and Huang R 2005 *Chin. J Semicond.* **26** 1401
[11] Tian Y, Bu W H, Wu D K, An X, Huang R and Wang Y Y 2005 *Semicond. Sci. Technol.* **20** 115