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New aspects of HCI test for ultra-short channel n-MOSFET devices*

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Hot carriers injection (HCI) tests for ultra-short channel n-MOSFET devices were studied. The experimental data of short channel devices (75–90 nm), which does not fit formal degradation power law well, will bring severe error in lifetime prediction. This phenomenon usually happens under high drain voltage ($V_{\rm d}$) stress condition. A new model was presented to fit the degradation curve better. It was observed that the peak of the substrate current under low drain voltage stress cannot be found in ultra-short channel device. Devices with different channel lengths were studied under different $V_{\rm d}$ stresses in order to understand the relations between peak of substrate current ($I_{\rm sub}$) and channel length/stress voltage.

Keywords: HCI, n-MOSFET, short channel

PACC: 7750，7360H，7340Q

1. Introduction

Hot carrier injection (HCI) has long been one of the most important reliability issues for MOSFET devices. Several HCI degradation models have been proposed to accurately predict lifetime of devices under operation voltage, and the results obtained are in good agreement with experimental data.[1−8] With MOSFET device continuously scaling down (75 nm channel length or even shorter), some changes were observed, such as degradation saturation of drain saturation current ($I_{\rm dsat}$), peak missing of substrate current ($I_{\rm sub}$), etc.

In this paper, we report some experimental data of short channel devices (75–90 nm), which do not fit well with the former models, and provide some new ideas about how to change the methodology of HCI to predict the lifetime of devices more accurately. Firstly, in our HCI experiments, operation voltage for core devices were decreased to about 1 V, therefore the stress voltages of drain and gate decreased to 1.4–2.0 V. Under some stress conditions, shift saturation of on-state current ($I_{\rm on}$) can be observed, which shows that $I_{\rm dsat}$ or drain linear current ($I_{\rm dlin}$) shift does not fit linearly with stress time. This phenomenon happens mostly under high $V_{\rm d}$ stress condition. In this paper, we try to explain it with Si/SiO_2 interface passivation model. Secondly, there are some changes in $I_{\rm sub}$ peak when channel length is ultra-short. Our data showed that $I_{\rm sub}$ peak becomes weak and close to $V_{\rm d}$ or even disappears under normal testing method ($V_{\rm d}$ is constant, $V_{\rm g}$ ramps from 0 to $V_{\rm d}$) when the length and the gate oxide thickness becomes small enough.

2. Devices and experiments

For studying HCI degradation of devices, n-MOSFETs with channel length from 75 nm to 0.35 μm and width of 10 and 5 μm were tested. Gate oxide thicknesses of the devices were about 1.4 and 4 nm with decoupled plasma nitridation (DPN) process.

Hot carrier stress was applied with $V_{\rm g}$ adjusted to achieve the worst degradation case ($V_{\rm g} = V_{\rm d}$ for 75 nm channel length device). Operation voltage of the device was 1.0 V. $I_{\rm dsat}$, $I_{\rm dlin}$, $I_{\rm dsatR}$ ($I_{\rm dsat}$ with source–drain reversed) and $I_{\rm dlinR}$ ($I_{\rm dlin}$ with source–drain reversed) were recorded with Agilent4156 semiconductor parameter tester and Cascade S1901 probe station.

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3. HCI degradation saturation

Normally, drain current degradation with stress time obeys a power law, so it will be easy to predict time to fault (TTF) by extrapolating to a certain $I_{\rm d}$ shift value. But in our short channel device data, we found a kind of violation from original curve. Figure 1 shows $I_{\rm dsat}$ and $I_{\rm dlin}$ degradations versus stress time of n-MOSFET device with 75 nm channel length. It shows that reverse $I_{\rm dsat}$ and $I_{\rm dlin}$ degradations are more severe than that of $I_{\rm dsat}$, because reverse $I_{\rm dsat}$ and $I_{\rm dlin}$ are influenced more severely by Si/SiO_2 interface traps.[4,5] The degradation of $I_{\rm dlin}$ is compared with that of $I_{\rm dsat}$. Carriers are easier to be trapped by the interface traps when $V_{\rm d}$ lies in a linear region, thus $I_{\rm dlin}$ degrades more severely than $I_{\rm dsat}$. Therefore, $I_{\rm dlin}$ degradation is considered to be due to the defect trap generation in the whole channel region.[6]

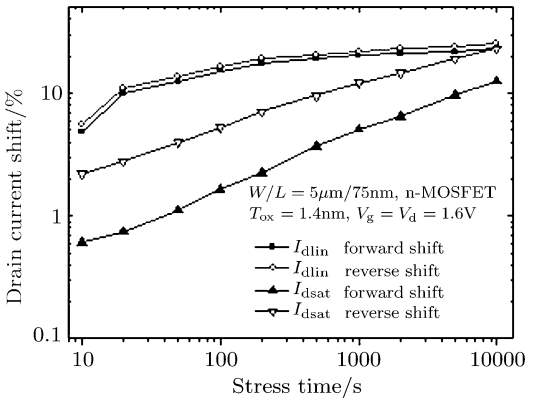


Fig.1. Degradation of saturation and linear drain current versus stress time.

In Fig.2, $I_{\rm dsat}$ degradation curves are compared at different stress drain and gate voltages. It can be found that the saturation tends to happen under high stress voltage.

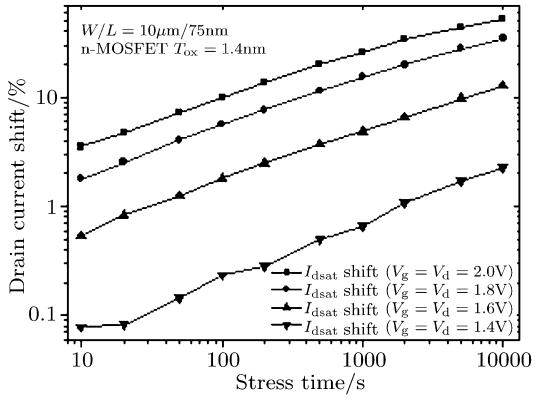


Fig.2. Saturation drain current degradation versus stress time at different stress voltages.

Under the same stress condition, drain current degradations of the devices with different channel lengths and gate oxide thicknesses are presented in Fig.3. It also shows that the degradations of devices with short channel and thin gate-oxide tend to be saturated.

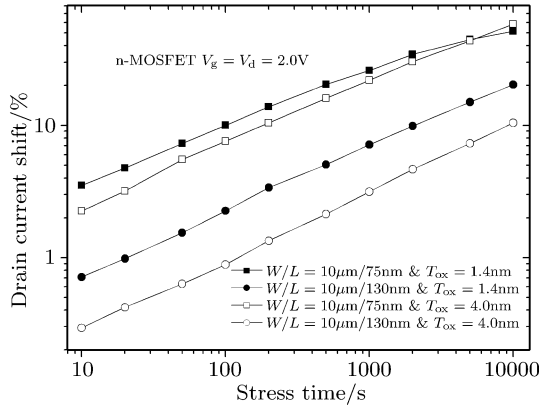


Fig.3. Drain current degradation for different channel lengths.

Based on the stress degradation curves, it is suggested that the original power law of degradation should be modified. We present here a new model

$$\Delta I_{\rm d} \propto t^n - C.$$

Here n and C are constants to be determined by using the degradation curves. In this experiment, the model fits the degradation curves well.

4. Condition for HCI stress in the worst case

The worst-case condition for HCI stress has been studied for many years.[7] It is commonly accepted that $V_{\rm g}$ at $I_{\rm sub}$ peak is the worst condition for n-MOSFET degradation. With a constant drain voltage, the substrate current of devices with different channel lengths versus gate voltage is presented in Fig.4(a). In our experiment, it was found that in some cases, the $I_{\rm sub}$ peak cannot be found for short channel devices.

Figure 4(b) shows the short channel device's $I_{\rm sub}$ curves versus gate voltage, which are compared at different drain voltages. The $I_{\rm sub}$ peak can be found at higher drain voltage, but cannot be found at low $V_{\rm d}$. The experimental data shows that for different channel lengths, different values of drain voltage are needed to find the $I_{\rm sub}$ peak again. We also find the relationship, according to Fig.5, between the maximum of substrate current ($I_{\rm sub}$ peak for long channel device or $I_{\rm submax}$ for short) and drain voltage of different channel lengths devices accords with power rule.

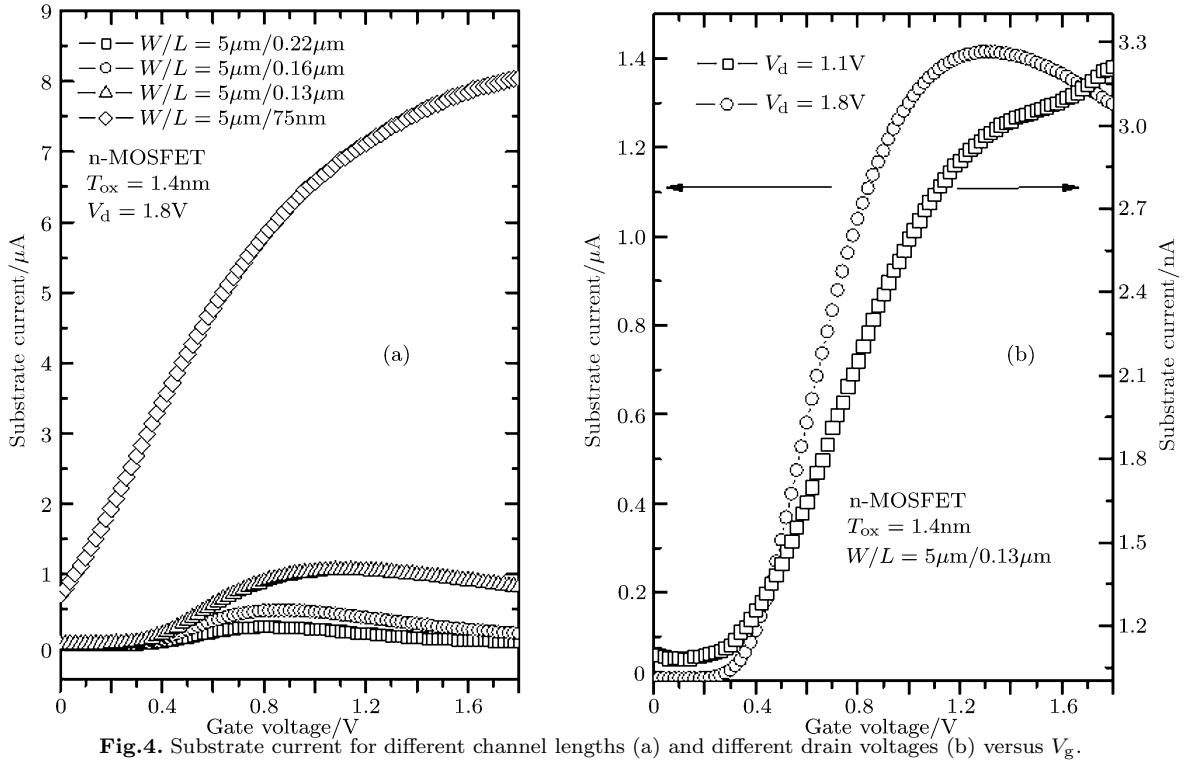


Fig.4. Substrate current for different channel lengths (a) and different drain voltages (b) versus V_g.

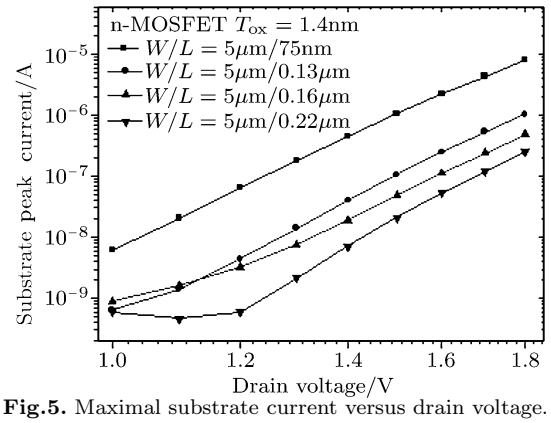


Fig.5. Maximal substrate current versus drain voltage.

In Fig.6(a), there are two areas of gate stress voltage, for different channel lengths. We have tested the devices under different V_d stresses to determine if I_{sub} peak points exist. A trend can be found that for a given channel length, an increase of drain stress voltage will make it possible to find I_{sub} peak. So in this plot, there exists no I_{sub} maximum point in the lower left area, but there exists in the upper right area. The relationship between the gate voltage at which the peak substrate current appears and the device channel length is shown in Fig.6(b).

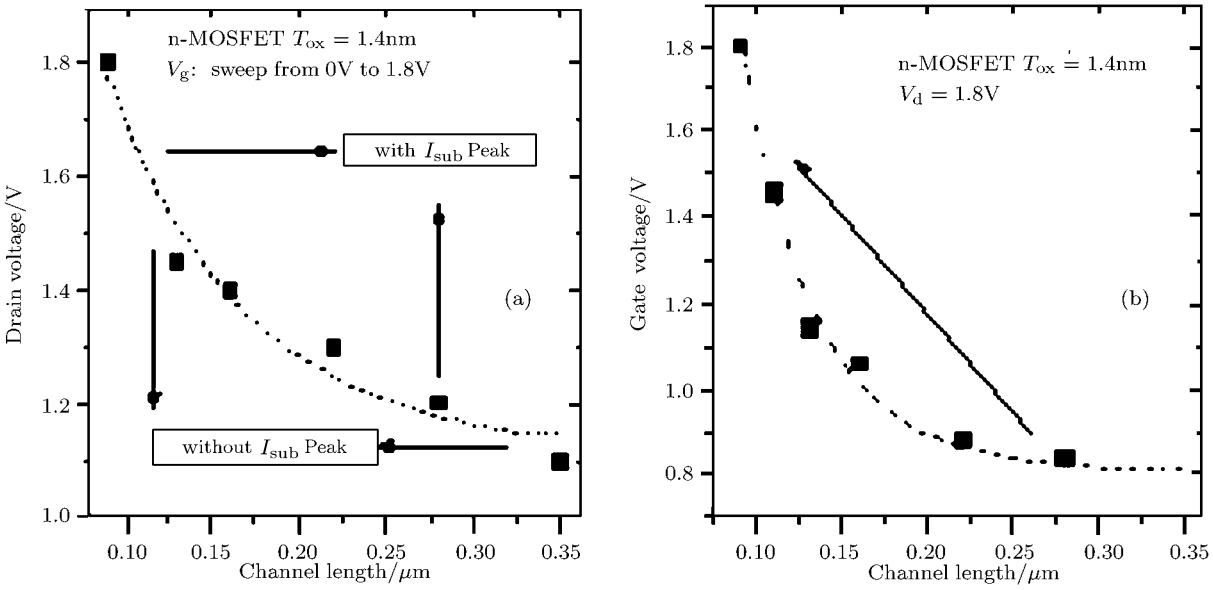


Fig.6. Two-area plot of I_{sub} peak under drain stress.

It is found that the gate voltage goes up to the drain voltage as the channel length decreases.

5. Summary

Drain current degradation saturation is observed in the short channel n-MOSFET devices during HCI stress. This makes it difficult to evaluate quickly the TTF of device by extrapolating the degradation curve to the failure criteria. Different channel lengths of devices were compared with each other and we found that short channel devices are easy to saturate. Therefore it will underestimate the lifetime of the devices. A revised model for degradation power law was provided to fit the degradation curve better. The worst stress condition also changes in short channel device under HCI stress. Traditional I_{submax} point is no longer easy to be found. Devices with different channel lengths were tested at different stress voltages to divide the field into two areas, i.e. areas with and without I_{sub} peak.

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