Vol 15 No 10, October 2006
1009-1963/2006/15(10)/2431-08

Chinese Physics

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Evaluation of negative bias temperature instability in ultra-thin gate oxide pMOSFETs using a new on-line PDO method*

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(Received 27 March 2006; revised manuscript received 2 June 2006)

A new on-line methodology is used to characterize the negative bias temperature instability (NBTI) without inherent recovery. Saturation drain voltage shift and mobility shift are extracted by $I_D - V_D$ characterizations, which were measured before stress, and after every certain stress phase, using the proportional differential operator (PDO) method. The new on-line methodology avoids the mobility linearity assumption as compared with the previous on-the-fly method. It is found that both reaction–diffusion and charge-injection processes are important in NBTI effect under either DC or AC stress. A similar activation energy, 0.15 eV, occurred in both DC and AC NBTI processes. Also degradation rate factor is independent of temperature below 90°C and sharply increases above it. The frequency dependence of NBTI degradation shows that NBTI degradation is independent of frequencies. The carrier tunnelling and reaction–diffusion mechanisms exist simultaneously in NBTI degradation of sub-micron pMOSFETs, and the carrier tunnelling dominates the earlier NBTI stage and the reaction–diffusion mechanism follows when the generation rate of traps caused by carrier tunnelling reaches its maximum.

Keywords: negative bias temperature instability, proportional differential operator, degradation

PACC: 7750, 7360H, 7340Q

1. Introduction

Although negative bias temperature instability (NBTI) has been known for more than 35 years, it has only recently emerged as one of the most serious reliability issues in advanced CMOS technologies.[1−3] Recovery effect is a particular phenomenon in NBTI degradation which has serious effects on measurement and warps NBTI degradation.[4] It is well known that V_T measurements lead to a large recovery which is proportional to the time spent during V_T measurement. As a consequence, the NBTI degradation is underestimated, making the design modelling too optimistic.[5] To overcome this, some on-line measurement techniques were developed including on-the-fly characterization,[6] pulse $I_D - V_G$ technique,[7] oscilloscope technique.[8] Though these methods can greatly avoid the recovery, V_T shift calculation in on-the-fly method cannot be accurate because of a linear mobility degradation assumption. The pulse $I_D - V_G$ technique is also hard to be used in NBTI degradation characterization because of its poor precision.

In this paper, a new on-line technique is proposed, and then a new setup is used to extract V_{DSAT} shift based on proportional differential operator (PDO) technique.[9−12]

2. Experiments

The devices used in this study were pMOSFETs with 10μm in channel width (W) and 0.13μm in channel length (L). The gate oxide thickness was about 2.5nm measured by $C - V$ and simulation methods. HP4156B semiconductor parameter analyser was used to realize the DC NBTI stress. HP 41501A pulse generator was used to provide AC pulse stress voltage. Measurement was re-configured based on Agilent FLEX command[13] to obtain much faster speed. In our experiments, 61 dots $I_D - V_D$ measurement only needed about 80ms. The new setup proved to be better than the conventional one in avoiding the inherent NBTI recovery effect.

To avoid recovery, it was necessary to keep constant stressing of the gate voltage during the stress and the measurement phases. Saturation drain voltage shifts were extracted using $I_D - V_D$ curves in cer-

*Project supported by the State Key Development Program for Basic Research of China (Grant No G2000-036503).
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tain stressing time intervals. Figures 1(a) and 1(b) show the DC and AC stress measurement diagrams

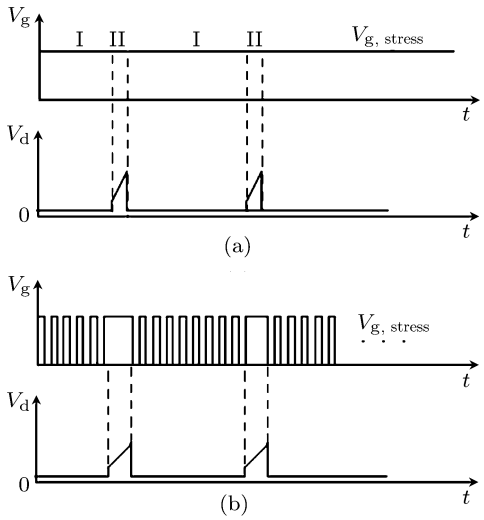


Fig.1. (a) Gate and drain voltage configurations during DC NBTI stress, (b) Gate and drain voltage configurations during AC NBTI stress.

respectively. Phase I denotes the stressing period and phase II the measurement period. It is easy to understand that these configurations decrease or eliminate recovery effect because stress voltage is biased on the gate for all the time including $I_{\rm D}-V_{\rm D}$ measurement time.

The procedure is shown in Fig.2.

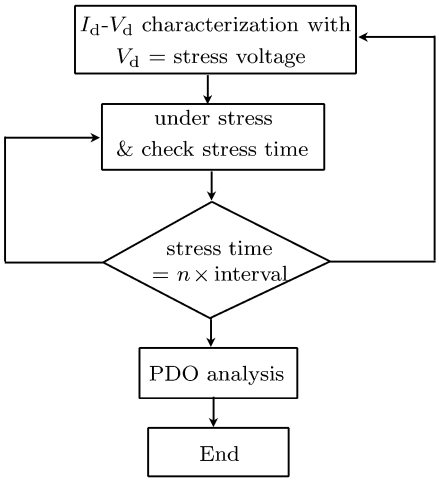


Fig.2. The procedure for DC or AC NBTI stress during new on-line measurement.

3. The PDO characterization technique

3.1. Proportional difference spectral function theorem[9]

The proportional difference of a function, $f(x)$, is defined as $\Delta_{\rm p}f(x)=f(kx)-f(x)$, where k is a certain given positive number ($k>1$) called the proportional differential constant, $\Delta_{\rm p}$ is the proportional differential operator. If $f(x)$ is a simple strictly monotonic, continuous, differentiable function on $[\,0,\infty)$, and if $f(0)=A$, $\lim_{x\to\infty}f(x)=B$, then there exists $x_{\rm p}\in[\,0,\infty)$, such that $\Delta_{\rm p}f(x)$ has an extremum on $x_{\rm p}$, where A and B are two constants.

3.2. The proportional difference of output characteristic of MOSFETs[10,11]

The drain current expression of the MOSFET in closed form, based on the charge sheet model, is given by[14,15]

$$\begin{aligned} I_{\rm d}=\frac{Z}{L}\mu C_i\beta^{-2}\Big\{&(1+\beta V_{\rm G}-\beta V_{\rm FB})(\beta\phi_{\rm SL}-\beta\phi_{\rm S0})\\ &-\frac{1}{2}\left[(\beta\phi_{\rm SL})^2-(\beta\phi_{\rm S0})^2\right]-\frac{2}{3}\alpha\left[(\beta\phi_{\rm SL})^{3/2}\right.\\ &\left.-(\beta\phi_{\rm S0})^{3/2}\right]+\alpha\left[(\beta\phi_{\rm SL})^{1/2}-(\beta\phi_{\rm S0})^{1/2}\right]\Big\} \end{aligned} \tag{1}$$

where Z is the channel width, L is the channel length, μ is the effective carrier mobility, $\beta=q/kT$, C_i is the gate oxide capacitance, $\alpha=\sqrt{2}(C_{\rm FB}/C_i)$, $C_{\rm FB}$ is the flat-band capacitance, $V_{\rm FB}$ is the flat-band voltage, $\phi_{\rm SL}(=\phi_{\rm S0}+V_{\rm D})$ is the potential at the drain end of the channel, and $\phi_{\rm S0}$ is the potential at the source end of the channel.

It is clear from Eq.(1) that the proportional differential spectral function theorem can be satisfied by $I_{\rm D}(V_{\rm D})$. Then

$$\Delta_{\rm p}I_{\rm D}(V_{\rm D})=I_{\rm D}(kV_{\rm D})-I_{\rm D}(V_{\rm D}) \tag{2}$$

should have an extremum when $V_{\rm D}=V_{\rm DP}$.

$$\left.\frac{\partial\Delta_{\rm P}I_{\rm D}(V_{\rm D})}{\partial V_{\rm D}}\right|_{V_{\rm D}=V_{\rm DP}}=0, \tag{3}$$

because $\Delta_{\rm P}I_{\rm D}(V_{\rm D}=0)=\Delta_{\rm P}I_{\rm D}(V_{\rm D}\to\infty)=0$.

From Eqs.(2) and (3), we obtain

$$V_{\rm G} - V_{\rm FB} - 2\phi_B = (k+1)V_{\rm DP} + \gamma\sqrt{(k+1)V_{\rm DP} + 2\phi_B}, \quad (4)$$

where $\gamma = \sqrt{2qN_A\varepsilon_{\rm s}}/C_i$.

Also, the value of $V_{\rm Dsat}$ can be obtained from Eq.(1) under the condition $\partial I_{\rm D}/\partial V_{\rm D}\Big|_{V_{\rm D}=V_{\rm Dsat}} = 0$,

$$V_{\rm G} - V_{\rm FB} - 2\phi_{\rm B} = V_{\rm Dsat} + \gamma(V_{\rm Dsat} + 2\phi_{\rm B})^{1/2}. \quad (5)$$

Comparing Eq.(4) with Eq.(5), we obtain a relationship between $V_{\rm Dsat}$ and $V_{\rm DP}$

$$V_{\rm Dsat} = (k+1)V_{\rm DP}. \quad (6)$$

The MOSFET saturated threshold voltage is defined as[16]

$$V_{\rm ths} = V_{\rm G} - V_{\rm Dsat}, \quad (7)$$

so

$$\Delta V_{\rm ths} = -\Delta V_{\rm Dsat} = -(k+1)\Delta V_{\rm DP}. \quad (8)$$

In the linear region, classical threshold voltage can be written as

$$V_{\rm thl} = V_{\rm FB} + 2\phi_{\rm B} + \gamma\sqrt{2\phi_{\rm B}}, \quad (9)$$

and can be extrapolated from Eq.(4) when $V_{\rm DP} \to 0$,

$$V_{\rm thl} = V_{\rm G}(V_{\rm DP} \to 0) = V_{\rm FB} + 2\phi_B + \gamma\sqrt{2\phi_B}. \quad (10)$$

It is clear that

$$\Delta V_{\rm ths} = -\Delta V_{\rm Dsat} = -(k+1)\Delta V_{\rm DP} \approx \Delta V_{\rm th0}. \quad (11)$$

Combining Eqs.(2), (3) and (6), we also have

$$\Delta_{\rm P} I_{\rm D}(V_{\rm DP}) = \left(\frac{Z}{L}\right)\mu C_{\rm ox} B, \quad (12)$$

$$B = \frac{1}{2}(k^2-1)V_{\rm DP}^2 + \gamma V_{\rm DP}(k-1)\sqrt{(k+1)V_{\rm DP} + 2\varphi_B} - \frac{2}{3}\gamma\frac{(k-1)}{(k+1)}\left[((k+1)V_{\rm DP} + 2\varphi_B)^{3/2} - 2\varphi_B^{3/2}\right]. \quad (13)$$

Then

$$\frac{\Delta\mu_n}{\mu_n} = \frac{\Delta(\Delta_{\rm p}(I_{\rm D}(V_{\rm DP}))}{\Delta_{\rm p}(I_{\rm D}(V_{\rm DP})} - \frac{\Delta B(V_{\rm DP})}{B(V_{\rm DP})}. \quad (14)$$

Figure 3(a) shows PDO spectra, and the position of the maximum can be extracted to calculate saturation drain voltage, threshold voltage, and mobility, which are shown in Fig.3(b).

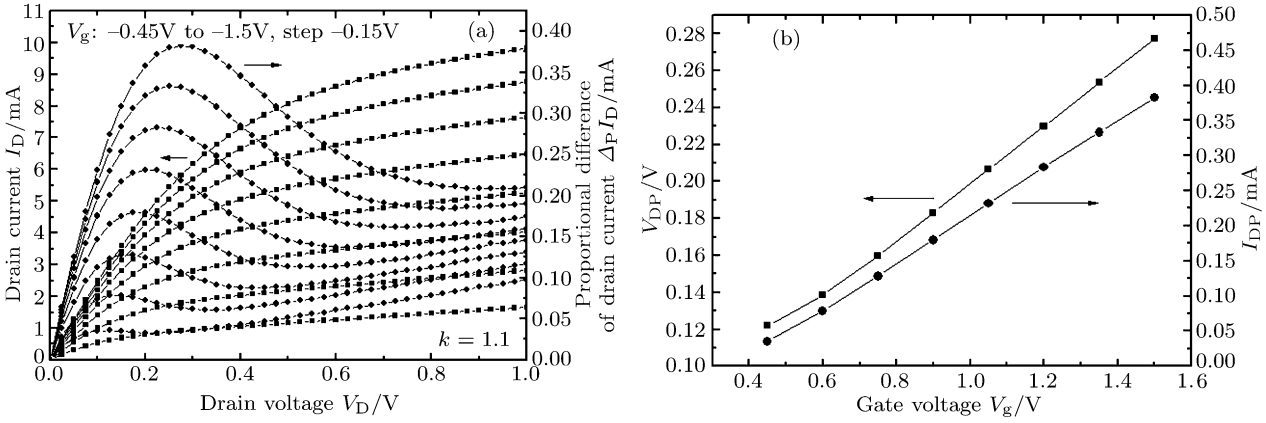


Fig.3. (a) PDO spectra for $I_{\rm D} - V_{\rm D}$ characterization of gate voltage from -0.45 to -1.5V, (b) $V_{\rm DP} - V_{\rm g}$ and $I_{\rm DP} - V_{\rm g}$ relations.

Figure 4(a) shows $\Delta V_{\rm DP}$ – t and $\Delta I_{\rm D}(V_{\rm DP})$ – t from which Fig.4(b) of $\Delta V_{\rm DSAT}(V_{\rm g})$ – t and $\frac{\Delta\mu_n}{\mu_n}$ – t is obtained. The inset in Fig.4(b) is $\frac{\Delta(\Delta_{\rm p} I_{\rm P}(V_{\rm DP}))}{\Delta_{\rm P} I_{\rm P}(V_{\rm DP})}$ – t and $\frac{\Delta B(V_{\rm DP})}{B(V_{\rm DP})}$ – t. Figure 4(b) shows that both $V_{\rm DSAT}$ and mobility shift follow the power law, and it is obvious that mobility linearity prediction is not valid in the on-the-fly method.[6]

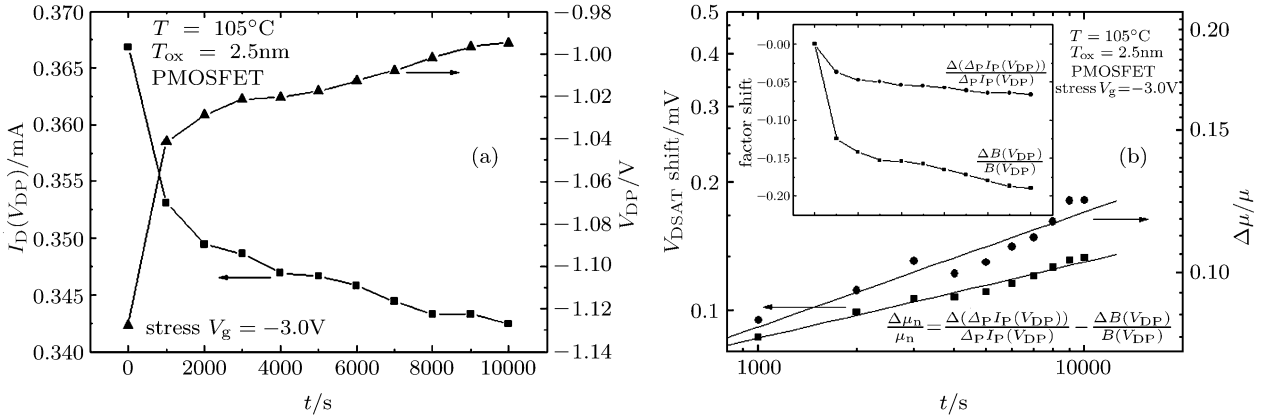


Fig.4. (a) Time dependence of V_{DP} (x peak position) and I_{DP} shift (y peak position) obtained from the $I_D - V_D$ curves using PDO technique, (b) time dependence of saturation drain voltage and mobility degradation within 1000s stress time at 105°C; inset plots the two factors in Eq.(14).

Figure 5 shows the comparison of the PDO method, on-the-fly method[6] with the conventional one.

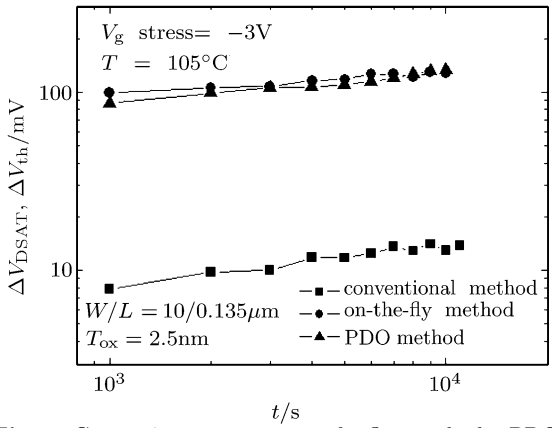


Fig.5. Comparisons among on-the-fly method, PDO method and conventional method at 105oC and -3V stress voltage.

The measured results of the threshold voltage shift ΔV_{ths} from the two on-line methods are consistent with each other, because the inherent recovery has been avoided. The difference between the two on-line methods is attributed mainly to mobility linearity assumption in the on-the-fly method[6] and also the sample diversity. The measurement error should also be considered. However, the error from the conventional method is smaller because of the inherent NBTI recovery effect.

4. NBTI degradation under DC and AC stresses

4.1. Stress voltage dependence of NBTI degradation in short-channel device under DC stress

Figures 6(a) and 6(b) show the comparison of degradations between different stress voltages at 105°C in short-channel pMOSFETs. The NBTI exhibits smaller V_{DSAT} shift with decreasing negative

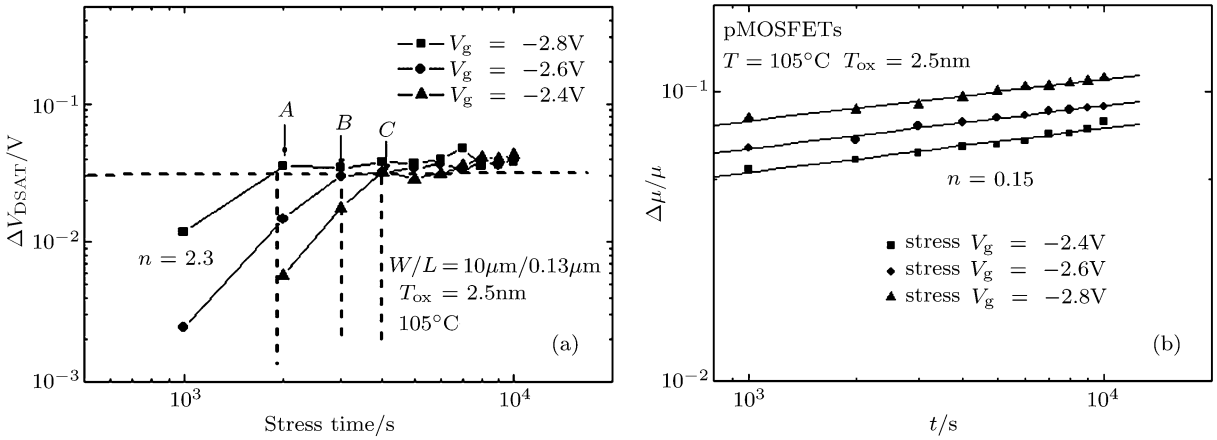


Fig.6. (a) Stress voltage dependence of NBTI degradation, (b) mobility shift during DC stress in short-channel ($W = 10\mu m, L = 0.13\mu m$) pMOSFETs at 105°C.

bias voltage, which is consistent with previous studies.[17,18] Interestingly, the stress time dependence of $V_{\rm DSAT}$ shift does not follow the power law. A power law exists with exponent $n \sim 2.3$ at the beginning, and as time increases continuously, the degradation rate factor (n) decreases and tends to a saturation value about 0.2. The $V_{\rm DSAT}$ shift deviates more from the power law relation as the stress voltage decreases from $V_{\rm g} = -2.4$V to $V_{\rm g} = -2.2$V, indicating that the degradation rate factor is dependent on the electric field. Finally, all the curves merge together. This phenomenon is partially similar to that reported in Ref.[19]. But mobility degradations obey power law and the degradation rate factor is approximately 0.15 under three voltages applied.

Lifetime is extracted from Fig.7 using the criterion of $\Delta V_{\rm DSAT} = 30$mV, as shown in Fig.6. The device's lifetime may be only 36000s even if it works under -1.0V voltage. The NBTI effect becomes more serious as device dimension shrinks.

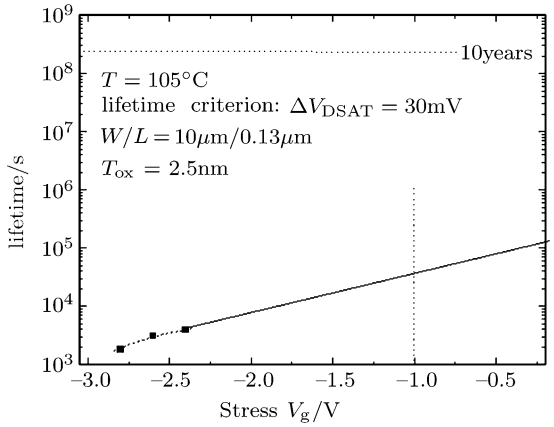


Fig.7. Stress $V_{\rm g}$ dependence of lifetime for short-channel pMOSFETs ($W = 10\mu$m, $L = 0.135\mu$m) at 105°C. Criterion is 30mV shift in $V_{\rm DSAT}$.

4.2. Temperature dependence of NBTI degradation under DC and AC stresses

Figure 8 shows the dependence of degradation rate factor on temperature under DC stress and 10 kHz AC stress. It is shown that the NBTI degradation rate factor is low below 90°C and then it increases abruptly with increasing temperature above 90°C for pMOSFETs.

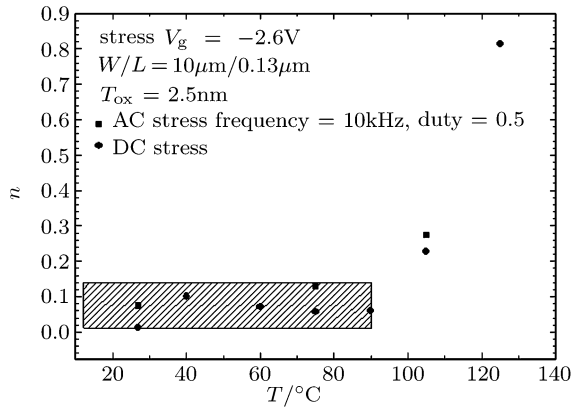


Fig.8. The temperature dependence of degradation rate factor under DC and AC stresses.

Figure 9 shows the normalized $V_{\rm DSAT}$ shift as a function of reciprocal temperature for pMOSFETs, in which the interface state data from Ref.[20] are also indicated.

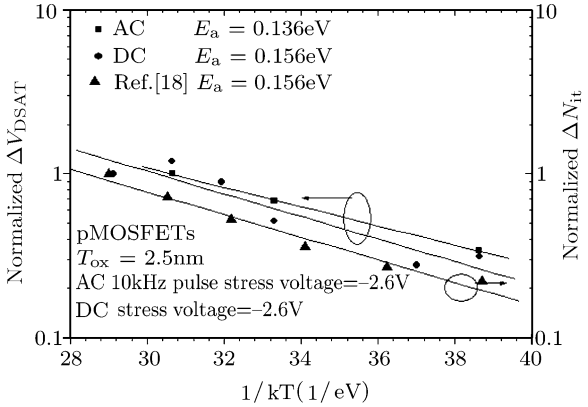


Fig.9. $V_{\rm DSAT}$ shift as a function of reciprocal temperature in pMOSFETs ($W = 10\mu$m, $L = 0.13\mu$m) under DC stress ($V_{\rm g} = -2.6$V) and 10 kHz AC stress (50% duty cycle square wave of 0 to -2.6V gate pulse bias). The interface state data are taken from Ref.[20].

In Fig.9, the activation energy extracted is about 0.15 eV for both AC and DC stresses which is approximately equal to that reported in Ref.[20] (about 0.156 eV).

4.3. Frequency dependence of NBTI degradation under AC stress

Figure 10 shows that $V_{\rm DSAT}$ degradation is partially recovered under AC stress. It is independent of frequency for a wide range of frequencies. This is in agreement with the result reported in Ref.[21].

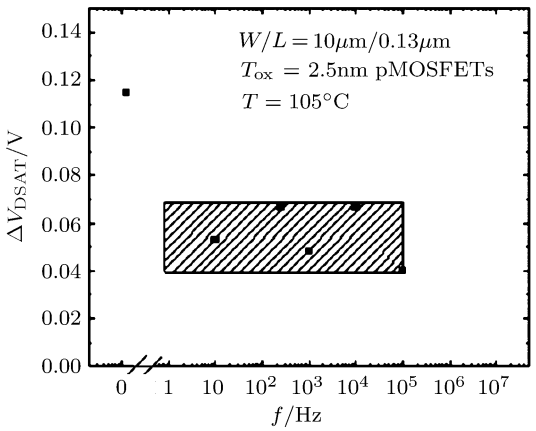


Fig.10. The frequency dependence of NBTI degradation under AC stress. A 50% duty cycle square wave of 0 to -2.6V is applied to the gate. Other terminals are grounded.

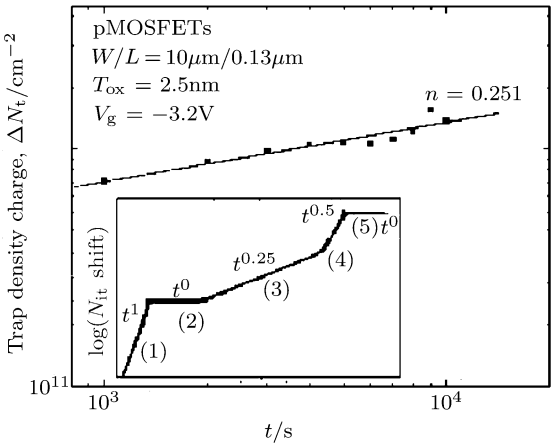
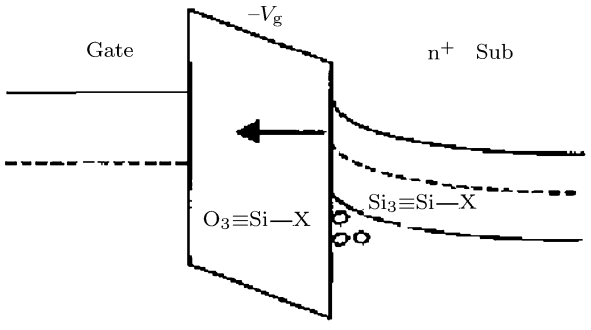


Fig.12. The total trap density generated under NBTI stress in a long-channel device at 105°C ($\Delta N_{it} = q \times \Delta V_{DSAT}/C_{ox}$), The inset indicates the five phases in the reaction–diffusion model. The five phases can be described by two equations: $dN_H/dt = D_H d^2 N_H/dy^2, dN_{IT}/dt = k_f[N_0 - N_{IT}] - k_r N_{IT} N_H^{(0)}$.

5. Discussions

Many models have been proposed to explain the NBTI, including: 1) hole injection from the inverted silicon surface into the gate oxide;[22–26] 2) thermally assisted electron tunnelling model;[27,28] 3) positive mobile charge model;[29] 4) chemical reaction–diffusion model.[30–33] In reaction–diffusion model, the interface trap generation is ascribed to hydrogen releasing from a hydrogen-terminated silicon-dangling bond (Si ≡ Si — H). Under the high temperature and negative gate voltage stress condition, the holes from the induced inversion layer react with the interface trap precursors (Si≡Si — H), breaking the H — Si bond and resulting in the increase of interface trap density. Then the hydrogen species produced diffuse/drift to the gate electrode. During the stress period, the interface acts as a hydrogen source, as shown in Fig.11, and the five phases of the reaction–diffusion model are shown in the inset of Fig.12.



$$Si_3 \equiv Si - X + A \Longleftrightarrow Si_3 \equiv Si^* + B$$
$$O_3 \equiv Si - X + C + p^+ \Longleftrightarrow O_3 \equiv Si^* + B$$
$$B_{Interface} \Longleftrightarrow B_{bulk} \text{ (Diffusion)}$$

Fig.11. Energy band diagram and the equilibrium equation in reaction–diffusion model.

There are five phases in the reaction–diffusion model, as shown in the inset of Fig.12. In the first phase, interface trap density increases rapidly with time due to Si-H bonds breaking in the Si/SiO_2 interface. This is the so-called reaction-limiting process. In the second phase, diffusion of hydrogen begins to take over. In the third phase, trap creation is limited by hydrogen diffusion, and this is so-called diffusion-limited process. In the fourth phase, hydrogen diffuses in the gate with infinite diffusion velocity. Finally in the fifth phase, maximum trap density is reached and the interface trap density no longer increases with time. Because the first two phases are too short to capture and little experiments can take so much time to reach the fourth and fifth phases in thick oxide and long-channel devices, only the third phase can be easily extracted, and the degradation rate factor is approximately 0.25, as shown in Fig.12 for a long-channel device. The measured total generated trap density under NBTI stress in long-channel device at 105°C obeys the power law and the degradation rate factor is also approximately 0.25, which is consistent with the rate in the third phase of the reaction–diffusion model. But with the device scaled down to sub-micron regime, our experimental results show that the interface trap density generated, N_{it}, may be diffusion-limited at the beginning, and finally merges, as shown in Fig.6, which means that the fifth phase has been reached and all the traps have completed their generation and tend to a saturation value. This is because much fewer interface trap precursors exist in sub-micron devices. For

a MOSFET with a 0.1 μm $\times$ 1.0 μm gate area, i.e. 10^{-9} cm^2, and $N_{\rm it} = 10^{10}\,{\rm cm}^{-2}$, there are only ten interface traps and ten fixed charges at the SiO_2/Si interface under the gate.[34]

Interestingly, from Fig.6(a), degradation rate factor can be larger than 2 at the beginning, and it takes more time to reach the turning point (as denoted A, B, C in Fig.6(a)) when stress voltage decreases. So besides reaction–diffusion, carrier-injection also plays an important role in the degradation process. Direct-tunnelling injected hole current from the channel which causes charge trapping should be considered. This process will be the dominant mechanism in PART-I (left-hand side of each turning point) and will lead to the quick generation of traps, and the time becomes longer to reach saturation trap density when lower stress voltage is applied.

In the following, the saturation drain voltage shifts are extracted from PART-II (right-hand side of each turning point) in Fig.6. The activation energy for both AC and DC stresses, 0.15eV, is extracted from Fig.9 and it is approximately consistent with interface trap activation energy (about 0.156 eV) reported in Ref.[20]. The measured result implies that the saturation drain voltage is influenced only by the creation of dangling bonds at the interface.[20] Furthermore, the frequency dependence results in Fig.10 can also be explained by reaction–diffusion: Si-H bonds are broken and traps are created by releasing the hydrogen species $X_{\rm interface}$ at the Si/SiO_2 interface when negative bias are imposed, while the reverse reaction starts when bias changes to be positive, as shown in Fig.11. According to our experimental results, we can conclude that the reaction–diffusion regime is still effective but hole injection becomes non-negligible in the NBTI degradation of the sub-micron device.

6. Conclusions

1. A new on-line methodology using PDO technique has been proposed to avoid recovery effect during the electrical parameter measurements. This technique gives the worst-case NBTI degradation as compared with the conventional methodology. Based on the charge sheet model, the extracted mobility degradation follows the power law. This measured result shows that the linear mobility degradation assumption in the on-the-fly method[6] is not valid.

2. It is found that reaction–diffusion and charge-injection processes are important in NBTI degradation under either DC or AC stress. The same activation energy has been obtained under AC and DC stresses in the temperature range of 27 – 125°C , implying that the conventional method can easily lead to wrong conclusion and the saturation drain voltage should be influenced only by the creation of dangling bonds at the interface. The degradation rate factor is independent of the temperature below 90°C and sharply increases with temperature increasing to above 90°C. The frequency dependence of degradation shows that NBTI degradation is independent of frequency under AC stress.

3. With gate oxide shrinking, reaction–diffusion is not the only mechanism dominating NBTI, and the carrier tunnelling and trapping dominates at the earlier phase of NBTI degradation of the sub-micron device. The reaction–diffusion mechanism begins to be dominant in the NBTI degradation when the generation rate of traps reaches a saturation value by carrier tunnelling.

Acknowledgment

Thanks are due to Motorola Company for providing test samples and measurement equipment.

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