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A bistable, self-latching inverter by the monolithic integration of resonant tunnelling diode and high electron mobility transistor*

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This paper reports that the structures of AlGaAs/InGaAs high electron mobility transistor (HEMT) and AlAs/GaAs resonant tunnelling diode (RTD) are epitaxially grown by molecular beam epitaxy (MBE) in turn on a GaAs substrate. An $Al_{0.24}Ga_{0.76}As$ chair barrier layer, which is grown adjacent to the top AlAs barrier, helps to reduce the valley current of RTD. The peak-to-valley current ratio of fabricated RTD is 4.8 and the transconductance for the 1-μm gate HEMT is 125mS/mm. A static inverter which consists of two RTDs and a HEMT is designed and fabricated. Unlike a conventional CMOS inverter, the novel inverter exhibits self-latching property.

Keywords: resonant tunnelling diode (RTD), high electron mobility transistor (HEMT), molecular beam epitaxy (MBE), bistability, self-latching

PACC: 7360L, 7335C, 6855

1. Introduction

The rapid development of information technology industry needs the circuits and devices to be continuously improved in terms of speed and power dissipation. Over the past years, scaling down has been proved to be an effective method for meeting these requirements. However, the physical limits of conventional technology are likely to be reached in 10–15 years according to the estimation from the semiconductor industry association roadmap.[1] It is necessary to exploit and develop heterogeneous technologies in order to resolve above problems.

The resonant tunnelling diode (RTD)[2] is a quantum device with the unique feature of negative differential resistance (NDR). The electrical properties of RTD with the relationship of photoluminescence spectra and magnetic fields have been studied.[3−4] It has become the most promising candidate for nano-scale integrated circuits in the future. However, it is difficult to design a circuit with RTD only since RTD is a two-terminal device and the current cannot be modulated. RTD-based logic circuits have the characteristics of high speed, low power dissipation, and reduced circuit complexity. To take advantage of these in very large scale integrated circuits (VLSI), RTD must be integrated with transistors. High electron mobility transistor (HEMT) is the most mature III-V device and has comprehensive applications in microwave and high-speed circuits. Compared with the circuits using HEMT alone, the integrated RTD/HEMT circuits are expected to realize higher speed and lower power.

Here, we report on the monolithic integration of nanoelectronics device RTD and HEMT on a GaAs substrate. High quality, reproducibility of molecular beam epitaxy (MBE) grown RTD/HEMT structures and fabrication technology are presented. Good material surface and electronic characteristics are obtained through the optimization of material growth condition and fabrication process. A static inverter which consists of two RTDs and one HEMT is demonstrated by using this technology. Unlike conventional CMOS

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inverter, the novel inverter exhibits self-latching property.

2. Experiment

HEMT and RTD structures were grown by MBE on a 2-inch semi-insulating GaAs substrate from the bottom to the top. Silicon was used as the n-type dopant. Native oxide on the substrate was removed in the cleaning chamber by heating under As_4 pressure of about 133×10^{-5}Pa. Growth interruptions and an *in situ* reflection high energy electron diffraction intensity oscillation technique were used to aid the growth of the thin barrier and well layers. The growth rate for GaAs, AlAs, and $Al_{0.24}Ga_{0.76}As$ was 0.280nm/s, 0.067nm/s, and 0.346nm/s, respectively.

The epitaxial layer structures of RTD/HEMT and the energy band diagram of RTD are shown in Fig.1. A ten periods 18.5nm/1.5nm AlGaAs/GaAs superlattice layers were used as the GaAs buffer. In contrast with the conventional structure of RTD, the RTD

GaAs	5×10^{18}	200nm	(a)
GaAs	5×10^{17}	10nm	
GaAs	5×10^{16}	10nm	
GaAs	undoped	5nm	
$Al_{0.24}Ga_{0.76}As$	undoped	1.2nm	
AlAs	undoped	1.7nm	
GaAs	undoped	5nm	
AlAs	undoped	1.7nm	
GaAs	undoped	5nm	
GaAs	5×10^{16}	10nm	
GaAs	5×10^{17}	10nm	
GaAs	5×10^{18}	50nm	
AlAs	undoped	4nm	
GaAs	5×10^{18}	200nm	
AlAs	undoped	4nm	
$Al_{0.24}Ga_{0.76}As$	undoped	30nm	
delta-doping	3×10^{12}		
$Al_{0.24}Ga_{0.76}As$	undoped	4nm	
$In_{0.18}Ga_{0.82}As$	undoped	12nm	
AlGaAs/GaAs (×10)	undoped	18.5nm/1.5nm (×10)	
S.I. GaAs substrate			

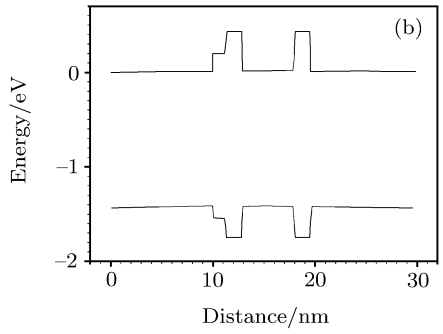


Fig.1. (a) Epitaxial structures of RTD/HEMT, (b) energy band diagram of RTD.

structure we grew had an $Al_{0.24}Ga_{0.76}As$ chair barrier layer adjacent to the top AlAs barrier layer. It helps to improve peak-to-valley current ratio (PVCR) since the chair barrier introduced significantly reduces both the coherent tunnelling current in the valley and the tunnelling current through the X valley. The aluminium mole fraction in the chair barrier is 0.24, which is higher than the values that have ever been reported.[5,6] Thin barrier AlAs layer, which is six monolayers in our scheme, helps to increase the current density and to promote Γ (GaAs)-Γ (AlAs) tunnelling. For fabrication purpose, two AlAs selective stop layers were inserted. The insertion of the etch stop layer is critical for obtaining a smooth HEMT surface, which leads to improved uniformities in threshold voltages and transconductances of the HEMT. It also makes the process repeatable and easy to control. Smooth potential barrier interfaces was obtained through the observation by high resolution transmission electron microscope. The double barrier quantum well region of RTD was not affected by the underlying HEMT structure.

For the device fabrication, the RTD mesa was first defined by nonselective wet etching (ammonia based) down to the n+ GaAs collector contact layer using the emitter metal as a mask. Then a critic-acid-based selective etchant[7] was used to etch down to the first AlAs etch stop layer. This was followed by a slight nonselective etching to remove AlAs layer and expose the HEMT cap layer. The device mesas (i.e. device isolations) were then defined by photolithography and wet etching. Ni/Ge/Au/Ni/Au was deposited and lifted off to make alloy ohmic contacts to the source and drain for HEMT. Rapid thermal annealing was performed at 390°C for 1min. The alloyed condition must be well selected. Over-alloying leads to the degradation of RTD characteristics due to the impurities diffused into the undoped quantum well region of RTD. It will significantly reduce the PVCR since the increase in the valley current, which originates from impurity scattering between the emitter electrode and the quantum well.[8] While lack-alloying results in bad ohmic contact and it affects both the DC and high frequency performance of the devices. The HEMT was completed by recess-etching and formation of the Ti/Pt/Au gate electrode. This recess-etching was carried out with a selective citric-acid-based etchant, which stopped etching at the surface of the second AlAs stop layer. Finally, Ti/Al/Ti/Au was deposited and lifted off for interconnection. A cross

section of the integrated RTD/HEMT mesa structure is shown in Fig.2.

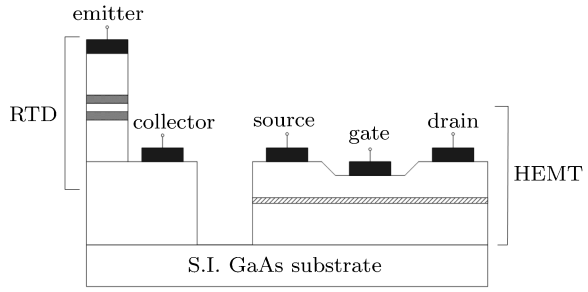


Fig.2. Schematic cross section of the integrated mesa structure.

3. Operation principle

The circuit diagram for the static inverter proposed is shown in Fig.3(a). The lower RTD (RTD-1) is referred to as the driver and the upper RTD (RTD-2) is referred to as the load. For RTD-2, the peak current, which is determined by the emitter area, is fixed. For RTD-1, since it is in parallel connection with a HEMT, the total current is the sum of current through RTD (I_{d1}) and HEMT source-to-drain current (I_{ds}). In this configuration, the peak current of RTD-1 can be modulated by the gate voltage applied on the gate of HEMT (V_{in}).

When the clock voltage (V_{clk}) is smaller than $2V_p$ (twice of the peak voltage of RTD), the circuit is in a monostable state, the output voltage (V_{out}) is low. When V_{clk} is greater than $2V_p$, the circuit is in a bistable state. The load-line diagram in this condition is showed in Fig.3(b). Two possible stable equilibrium states are labelled as '0' and '1'. For a RTD pair in one of the stable equilibrium states, a voltage fluctuation creates a current imbalance which charges (or discharges) the capacitances to drive V_{out} back toward the equilibrium value. Another intersection 'M' in the load-line is metastable. When the circuit is in the metastable state, the current difference in two branches at the output node determines which state the system converts to. An imbalance between the currents forces V_{out} to be away from the unstable equilibrium value. Since the unstable state is between the two stable states, the circuit will always come into one stable state. The monostable–bistable transition[9] is realized with the change of V_{clk}.

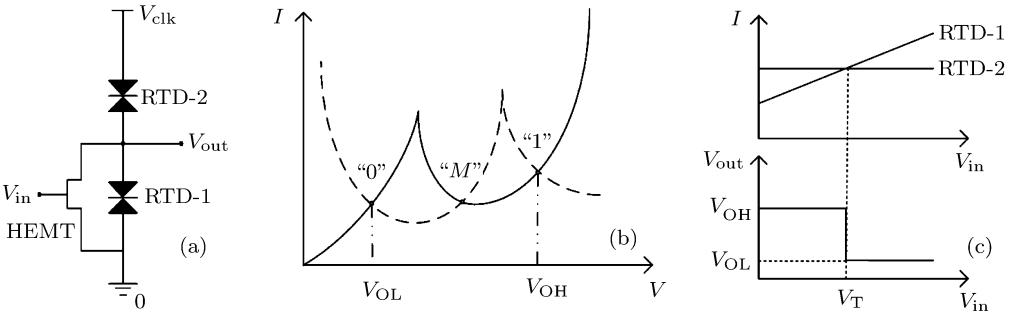


Fig.3. (a) Inverter schematic, (b) load-line in bistable state, (c) transfer characteristics.

A pair of RTDs has the self-latching property. The change of current at the output node influences the potential state of the circuit. To store a new value in a latch, V_{clk} is lowered into the monostable range long enough until V_{out} goes to low. V_{clk} is then restored to the bistable level, and the circuit comes into one of the stable states. The final state of the circuit is determined primarily by the current injected into the output node during the transition. If the injected current is above a threshold level, the latch ends up in high level: '1' state; for currents below this threshold, the latch ends up in low level: '0' state. Once it is latched, V_{out} will not change while V_{clk} is high, even if V_{in} changes.

The inverter operation and transfer characteristics are shown in Fig.3(c). We can see that the peak current of RTD-1 is modulated by V_{in} while the peak current of RTD-2 keeps constant. The circuit logic changes at the threshold voltage (V_T):

When input V_{in}='0' ($V_{in} < V_T$), it satisfies $I_{d1} + I_{ds} < I_{d2}$, the output

$$V_{out} = '1'. \tag{1}$$

When input V_{in}='1' ($V_{in} > V_T$), it satisfies $I_{d1} +$

$I_{ds} > I_{d2}$, the output

$$V_{out} = \text{`0'}. \tag{2}$$

4. Results

Isolated RTD and HEMT were fabricated on the same wafer. The $6\times6\mu m^2$ RTD exhibits a PVCR of 4.8, with a peak current density (J_p) of 8.3kA/cm^2 and a peak voltage (V_p) of 0.44V at room temperature. The RTD current–voltage ($I-V$) characteristics are modelled by a current source which is derived by a physics-based equation:[10]

$$\begin{aligned} I =& C_1 V^i \{\tan^{-1}[C_2(V - V_{T0})] \\ & - \tan^{-1}[C_2(V - V_N)]\} \\ & + C_3 V^j + C_4 V^k, \end{aligned} \tag{3}$$

where C_1, C_2, C_3 and C_4 are the numerical constants, i,j and k are integer exponents larger than two, V_{T0} is the threshold voltage, V_N is the voltage of the steepest part of the NDR region. After optimization by the nonlinear least square method, the parameters are obtained: C_1=18.37, C_2=35.52, C_3=3.52, C_4=-0.59, i=3, j=5, k=3, V_{T0}=0V, V_N=0.49V. The fitting result is shown in Fig.4. The dotted line is the measured data and the solid line is obtained by model simulation. The 1-μm gate HEMT is characterized as a depletion device. It has maximum transconductance of 125mS/mm with a threshold voltage (V_{th}) of –1.0V. The $I-V$ characteristics of a pair RTDs in series connection are shown in Fig.5. There are two peaks in the figure which correspond to the sequential switching of the series-connected RTDs. The current difference in two peak currents is expressed as

$$\Delta I = J_P \times \Delta A \tag{4}$$

where A is the emitter area of RTD. The RTD switches from a peak state (low-resistance ON-state) to a valley state (high-resistance OFF-state) whenever the current exceeds its peak current. So the RTD with small peak current switches first, followed by the RTD with the large peak current. Hysteresis is observed in the serial RTD $I-V$ characteristics. We attribute it to the large parasitic series resistance since the similar phenomenon is not observed in the individual RTD $I-V$ characteristics. It will happen when the accumulated series resistance exceeds the absolute value of the negative differential resistance.[11] No hysteresis is observed in the individual RTD, likely due to the large width of the spacer layer that can eliminate the hysteresis.[12] However, this hysteresis will not cause any problem in the logic operation because only the rising edge of V_{clk} determines the output. In Fig.6, the $I-V$ characteristics of a RTD and a HEMT in parallel connection are showed. Gate voltage V_{gs} varies from –0.6V to 0V in 0.2V steps. Since V_{gs} can modulate I_{ds}, the total current is also modulated. As a result, the peak current of RTD decreases with the absolute value increase of V_{gs}.

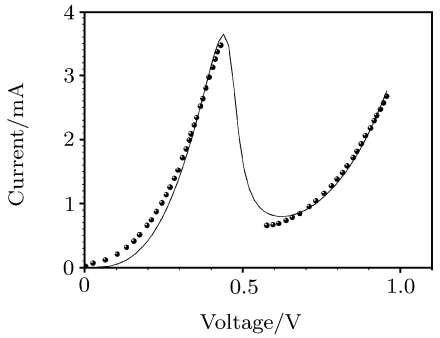


Fig.4. Measured RTD $I-V$ characteristics and model fit.

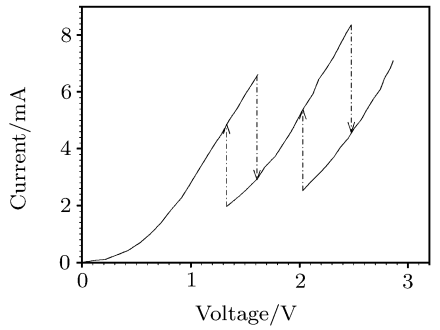


Fig.5. $I-V$ characteristics of a pair RTDs.

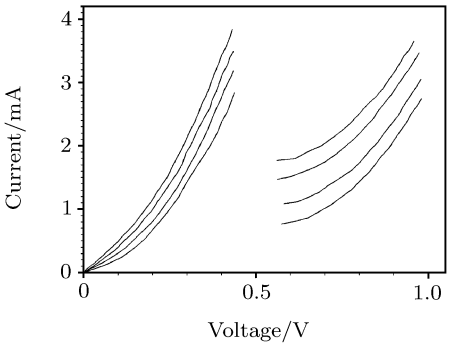


Fig.6. $I-V$ characteristics of a RTD in parallel connection with a HEMT.

The output characteristics and the microphotograph of the inverter are shown in Fig.7. The high level of V_{clk} was set to 1.0V. And the low level of V_{clk} was selected low enough to restrict the circuit in a

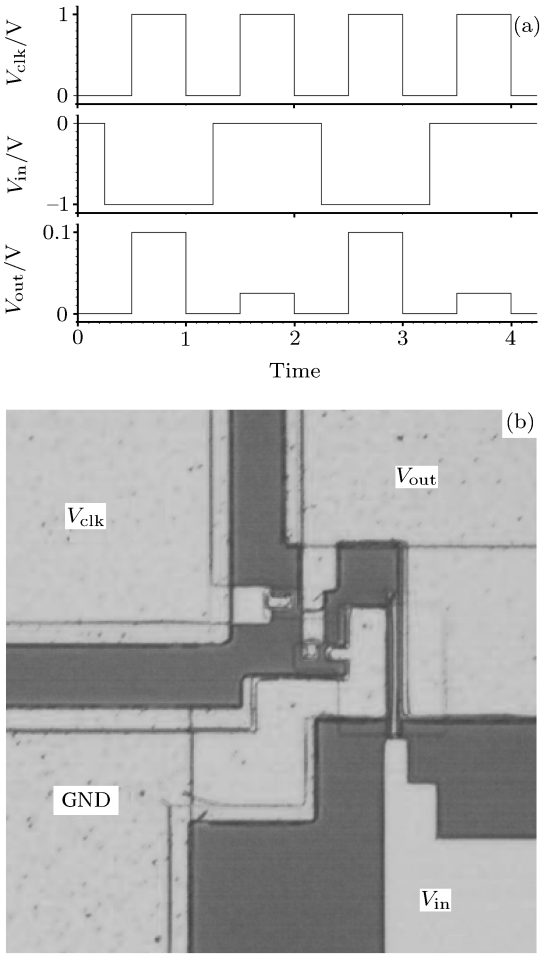


Fig.7. (a) Output characteristics, (b) microphotograph of the inverter.

monostable state. When V_{clk} is low, the circuit is in monostable state, V_{out} is low. When V_{clk} is high, the circuit is in bistable state, the state of V_{out} depends on the level of V_{in}: V_{out} is high when V_{in} is low, and vice versa. Inverted function is achieved. The measured output voltage swing is 99.82mV, which has much deviation with what we expected 0.78V by simulation program with integrated circuit emphasis (SPICE). The explanation for this is the loading effect of the measurement system. The input impedance on this oscilloscope's input port is 50Ω and the estimated magnitude of the output impedance of the inverter is about 340Ω at corresponding frequency. Therefore, the voltage drop across the oscilloscope is only 12.8% of the actual voltage swing. An output buffer is needed to obtain desired results. Unlike the conventional CMOS inverter, the novel inverter is self-latching. The self-latching property allows pipelining operation at the gate level, and thus brings very high through-output, without any area overhead associated to the addition of the latches.

5. Conclusion

Monolithic integration of GaAs/AlGaAs RTD and HEMT is realized on a GaAs substrate. An $Al_{0.24}Ga_{0.76}As$ chair barrier layer, which is grown adjacent to the top AlAs barrier, helps to improve PVCR of RTD. Two selective stop AlAs layers inserted make the process repeatable and easy to control. Basic combinational logic functions of RTD/HEMT have been verified. By using this integrated technology, a static inverter, which consists of two RTDs and one HEMT, is designed and fabricated. The inverter exhibits bistable and self-latching properties. High-speed pipeline operation is expected to be achieved in VLSI based on the monolithic integration of RTD and HEMT.

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