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Emitter of hetero-junction solar cells created using pulsed rapid thermal annealing

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In this paper, we use a pulsed rapid thermal processing (RTP) approach to create an emitter layer of hetero-junction solar cell. The process parameters and crystallization behaviour are studied. The structural, optical and electric properties of the crystallized films are also investigated. Both the depth of PN junction and the conductivity of the emitter layer increase with the number of RTP pulses increasing. Simulation results show that efficiencies of such solar cells can exceed 15% with a lower interface recombination rate, but the highest efficiency is 11.65% in our experiments.

Keywords: emitter, rapid thermal processing (RTP), PECVD, solar cell
PACC: 7208N, 7360N, 8630J

1. Introduction

The manufacturing of silicon integrated circuits (ICs) with dimension as low as a 20-nm feature size is expected to dominate the 21st century. The ultra small feature size coupled with 12 in (may be even 18 in) diameter wafers will force the IC manufacturers to reduce the processing temperature. The rapid thermal process (RTP) technique can be improved by the use of quantum photo-effects and thermal effects in thermal processing. This processing will provide a powerful method to process the compound semiconductors used for electronic and optical devices such as solar cells and flat panel displays.

The interest in RTP technology has grown in the past years as an alternative to conventional furnace processing, to reduce the thermal cost of manufacturing solar cells. As early as 1986, Singh[1] reported his experimental results and pointed out the difference in photo-spectrum between RTP and conventional furnace processing (CFP). And he predicted that high throughput and low defects would be the principal advantages of RTP.[2] This technology was also used for industrial solar cell processing and cell's efficiency could be improved by UV enhanced processing due to the quantum photo-effects.[3]

The approach is adopted in this work to create a PN junction. A phosphors-doped amorphous silicon (a-Si:H) or microcrystalline silicon (μc-Si:H) emitter layer formed by plasma enhanced chemical vapour deposition (PECVD) acts as an emitter layer. At high temperatures, phosphorus diffuses into silicon directly from the emitter. Simultaneously, the back surface field is formed on the rear face. This extremely simple process will reduce the thermal cost of manufacturing solar cells. Due to the tungsten halogen lamp used in our experiment, the thermal effect dominates in the RTP process.

Indeed, the RTP is a good option, particularly when the requirements for device parameters come into conflict with each other. The surface concentration has to keep high to obtain low contact resistance, while the surface recombination rate increases. Some problems still need to be solved such as the recombination at the emitter-base interface in our experiments.

2. Experimental details

The substrates are p-type crystalline silicon wafers with a resistivity of 1.3 Ωcm. After RCA cleaning, an a-Si emitter layer is deposited on the front face of the substrate by PECVD in the mixture of SiH_4 and PH_3. Next, Al is evaporated on the rear face of the wafer. Then, an RTP processing is applied in

Ar/H_2 gas. In this PTP processing, the Al/Si alloy is formed on the rear face and the hetero-junction solar cell structure is formed in the same process. Figure 1 shows the structure of a solar cell.

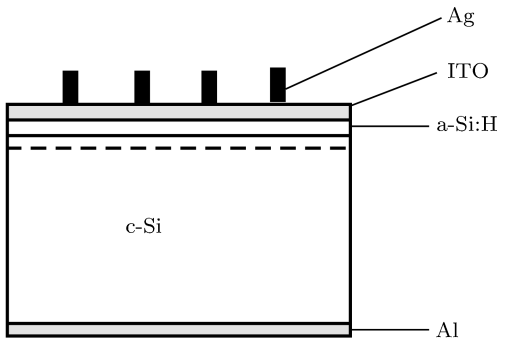


Fig.1. Sketch of a solar cell.

We adopt a pulsed RTP as shown in Fig.2 to crystallize the a-Si emitter layer and therefore to generate a PN junction. The RTP apparatus comprises a quartz chamber with cold walls capable of single wafer processing.[4] The sample is uniformly heated from the top to bottom using halogen-tungsten lamps (1250W/per) in Ar/H_2 ambient atmosphere. The heating rate is about 300°C/s. The RTP processing consists of a number of thermal cycles as shown in Fig.2. Each cycle includes a 60-second thermal bias at 450°C followed by a 10-second thermal bias at 1000°C.

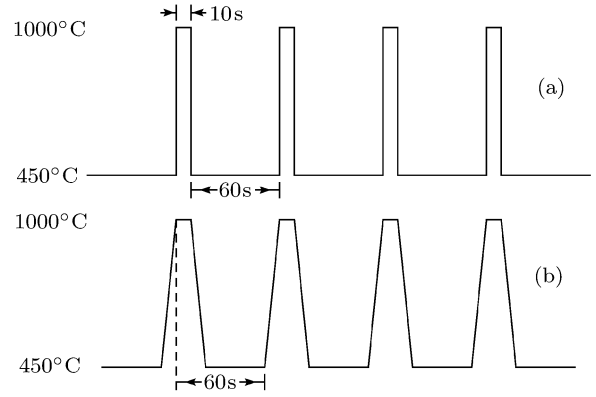


Fig.2. (a): Normative cycles of RTP time & temperature. (b) Real cycles of RTP time & temperature.

In order to investigate the electrical characteristic by Hall Effect, single layers are deposited on a p-type wafer with a high resistivity of 10 Ωcm. The concentration of the carrier and junction depth are measured by spread resistance. *I-V* curves of the device are investigated. The structural properties of the emitter layer are characterized using SEM. In addition, PC1D, a simulation software, is used to simulate the efficiency of solar cell against the thickness of emitter layer.

3. Results & discussion

3.1. The performance of the emitter layer

In order to obtain the thickness and optical band gap, all single layers must be deposited on double-face polished and one-face polished fused quartz separately. From the transmission measurements, the thickness and the optical band gap can be calculated.[5] The activation energy is obtained by conduction measurement. The optical band gap of the single layer varies from 1.54 eV to 1.12 eV before and after RTP.

Figure 3 shows the conductivities of the single n-type layer before and after pulsed RTP with different cycles in Ar/H_2 protection gas obtained by Hall-Effect measurement. From the figure, we can see that conductivity increases with pulse cycle increasing.

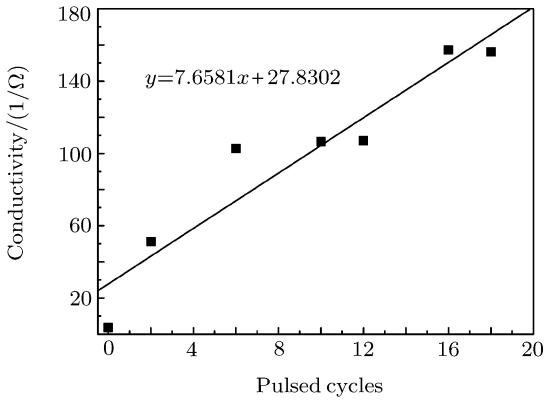


Fig.3. The conductivities of the single n-type layer before and after pulsed RTP with different cycles in Ar/H_2.

3.2. Creating the PN junction

If the process of the RTP for creating the emitter layer is similar to the two-step diffusion process, that is, when the single doped layer is applied to the substrate surface, it can be considered as a doping source and RTP processing is regarded as the redistribution step. The curve of phosphorus concentration can be calculated with conventional Gaussian distribution as follows:

$$X_j = 2\left(\ln\frac{N_S}{N_B}\right)^{1/2}\sqrt{Dt}, \qquad (1)$$

where N_B is the concentration of substrate, and N_S is the surface concentration. Here, in our experiment, the N_S/N_B is about 10^3.

Actually, the diffusion coefficient, D, is related to T, N_S, N_B, ambient atmosphere, and orientation of substrate. With Low N_B and ambient gas, D is a function of T as shown below:

$$D = D_0 \exp(-\Delta E/kT), \tag{2}$$

where T is the temperature, and $k = 8.62 \times 10^{-5}$ eV/K. ΔE , the action energy, is 3.69 eV and D_0, the diffusion coefficient, is 10.5 cm^2/s in the temperature range of 900°C to 1300°C. In our experiment, we use 10 cycles , lasting 100s at 1000°C and 600s at 450°C. Therefore, the diffusion coefficient D and the junction depth in the case of 100s at 1000°C are calculated respectively to be 2.61266×10^{-14} cm^2/s and 1.4 μm by using formula (1). From the data measured from the spread-resistance in our experiments, the junction depth is only 0.5μm, lower than the calculated one. That is to say, the pulsed RTP technology can have lower diffusion efficiency than the CFP technology. Other researches also obtained the same conclusion.[6]

Figure 4 shows the spread-resistance measurements. The concentration of the emitter is flat when Ar/H_2 is used as the annealing gas, which is similar to the conventional thermal diffusion process. It can be seen from Fig.4(a) that the interface of PN junction is steep, which means that PN junction obtained using this method has a steeper concentration distribution. From the fitting line of the junction depth as well as the pulsed cycles, it can be seen that the junction depth increases by 0.0156μm in Ar/H_2 gas when RTP increases by one cycle as shown in Fig.4(b).

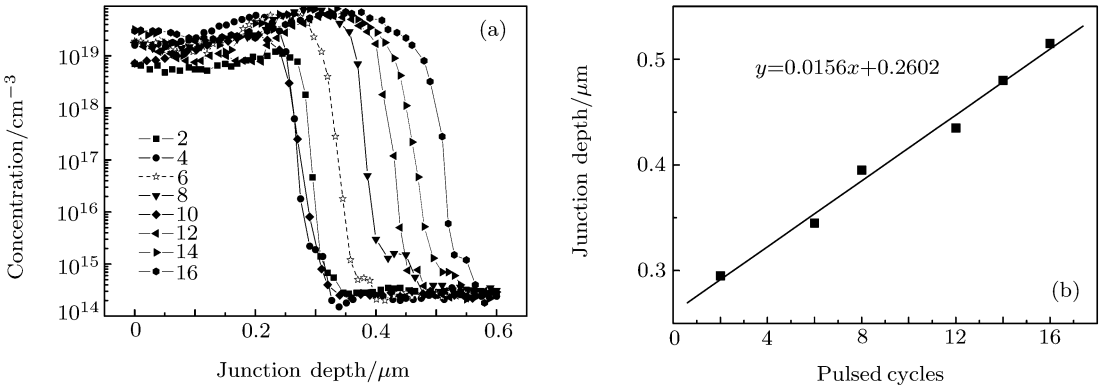


Fig.4. (a) PN curves under pulsed cycles from spread-resistance measurements. (b) Junction depth *vs* cycles pulsed cycles.

3.3. Solar cells

We use PC1D to simulate this type of emitter layer and its effect on solar cells. The parameters in Table 1 are used in simulation. The simulation results show that the efficiencies all exceed 15% with the junction depth of 0.1μm to 0.6μm, and the thickness of the emitter from 0.1μm to 0.3μm has little effect on the parameters of solar cells.

I–V characteristics with the thicknesses of emitter layers being of 0.2μm (8.25%), 0.3μm (9.01%) and 0.4μm (7.98%) are given in Fig.5. These three emitters are annealed within 10 cycles in Ar/H_2 ambient gas and their junction depth is 0.3μm. From the figure, we can see that the cell with an emitter thickness of 0.3μm has better parameters than the others.

Table 1. Parameters used in simulation.

Base	340μm, 1.3Ω·cm
Emitter	1×10^{20}cm^{-3}, Gaussian distribution
Minority Duffusion length	50μm
Front surface recombination	10^3cm/s to 10^5cm/s
Texture	No
Excitation and Mode	One sun, transient

From Fig.5, we also can see that the short currents are low. The concentration of the emitter is the same as that of the solar cell prepared by CFP to our

knowledge. But why are the open voltage (V_{oc}) and short current (I_{sc}) of the solar cell so low? From Fig.6, we can see that after pulsed RTP, although the grain size of the emitter layer is enlarged, there still exist some holes that are formed during the RTP process and further affect the short current of the solar cell. Because the E_g varies from 1.54 eV to 1.12 eV, the emitter layer becomes crystallized, and grain boundaries will reduce the photocurrent.

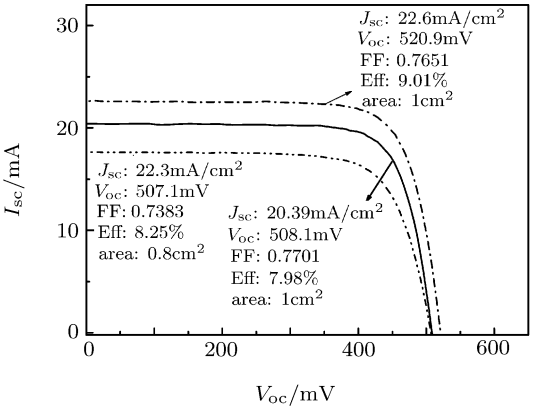


Fig.5. The I-V curves of solar cells.

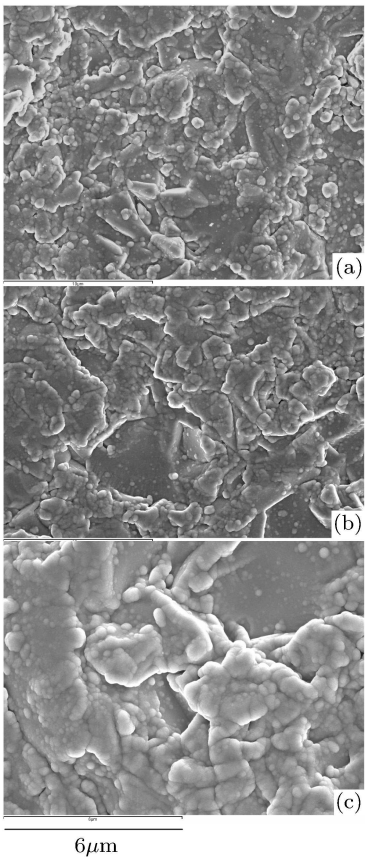


Fig.6. The SEM images of the emitter layer (a) before RTP, (b) after two RTP cycles, and (c) after 10 RTP cycles.

4. New progress

In order to increase the V_{oc} and I_{sc}, we prepare the emitter layer under the same PECVD conditions and add a SiO_2 layer as the cap layer before RTP process. The SiO_2 is prepared by means of sputtering. The SiO_2 layer is currently used as the cap layer in the solid-crystallinity. The SiO_2 can prevent the balling phenomenon in the high temperature process.[7,8] The RTP process and the solar cell technology used there are the same as those mentioned above. The short current density of the solar cell increases from 20.39 mA/cm^{2}to 29.03 mA/cm^2 and Cell's efficiency increases to 11.65% as shown in Fig.7.

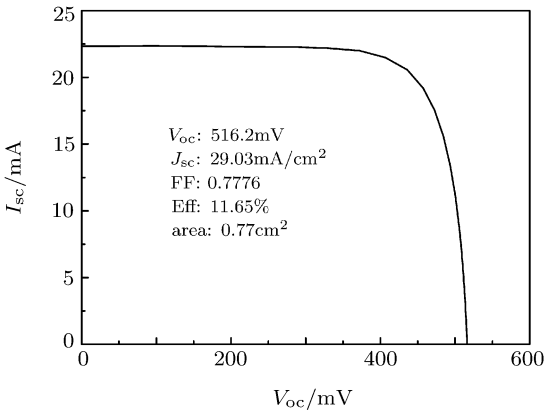


Fig.7. The improved I-V curve of solar cell.

5. Conclusions

In this paper, our pulsed rapid thermal annealing method is used to form the emitter layer and PN junction of the hetero-junction solar cell. Both the depth of PN junction and the conductivity of the emitter layer increase with the pulse number increasing. The solar cell parameters are not in agreement with the simulation results, which may be due to the poor emitter morphology. Since the emitter qualities are sensitive to process parameters, such as pulsed number and temperature. So, it is necessary to optimize the condition, say, using short annealing time and lower thermal effect. Hydrogen passivation has also been applied to the interface of the solar cell to improve the I_{sc} and V_{oc} in our experiments.[9]

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