Vol 15 No 10, October 2006
1009-1963/2006/15(10)/2297-09

Chinese Physics

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Low-parasitic ESD protection strategy for RF ICs in 0.35μm CMOS process*

Wang Yuan(王　源)†, Jia Song(贾　嵩), Chen Zhong-Jian(陈中建), and Ji Li-Jiu(吉利久)

Institute of Microelectronics, Peking University, Beijing 100871, *China*

(Received 29 December 2005; revised manuscript received 12 June 2006)

A systemic and comprehensive ESD-induced parasitic model is presented in this paper, which is used to analyse the parasitic influences of electrostatic discharge (ESD) protection circuits on the performance of radio frequency applications. A novel low-parasitic ESD protection structure is made in a 0.35μm 1P3M silicide CMOS process. The measured results show that this novel structure has a low parasitic capacitance about 310fF and a low leakage current about 12.2nA with a suitable ESD robustness target about 5kV human body model.

Keywords: electrostatic discharge, radio frequency, parasitic capacitance, leakage current

PACC: 4110D, 7340L, 5280

1. Introduction

The performances of integrated circuits (ICs), including speed, power, and integration, generally benefit from the advanced deep-submicron complement metal–oxide–silicon (CMOS) techniques, such as thinner gate oxide, shorter channel length, shallower junction, lightly drained diffusion (LDD) structure and salicided diffusion process. Unfortunately, electrostatic discharge (ESD) robustness of the ICs is terribly degraded by these novel techniques. ESD failures have become a profound reliability problem to the deep-submicron ICs. Statistics indicate that up to 30–40% of all IC electrical failure may be attributed to ESD events.[1] Hence, all of our focus for the past 20 years has been concentrated to the improvement of the ESD robustness level of the ICs. In order to acquire a sufficiently high ESD level, the traditional means is to use a large-area ESD protection device. However, a large-area ESD device is associated with large parasitic effects, including parasitic capacitance $C_{\rm ESD}$ and leakage current $I_{\rm Leakage}$. These parasitic effects are tolerable in the digital and low-speed mix-signal (M-S) applications, but have substantial impact on the high-speed M-S and radio frequency (RF) ICs' performance, such as, clock delay, signal integrity, input/output impedance matching, power efficiency and bandwidth. Hence, ESD protection for M-S and RF ICs has to deal with the tradeoff between good ESD performance and low parasitic effects.

Although some experimental researches[2−4] have been reported about parasitic effects for RF ESD protection, no systemic parasitic models have been reported to estimate the magnitude of these parasitic effects instead of those costly and time-consuming iterative experiments. How to accurately calculate these parasitic effects becomes a puzzle to RF designer. In this paper, a systemic and comprehensive ESD-induced parasitic model is presented, which is used to analyse the ESD-induced parasitic influences and find a low-parasitic ESD protection strategy for RF applications. Using this novel model, a novel low-parasitic ESD protection structure, lower-voltage-triggering silicon-controlled-rectifier series diode string (LVTSCR-SDS), is also performed. Compared with this novel ESD structure, several traditional ESD structures are implemented in a 0.35μm 1P3M silicide CMOS process.

2. ESD-induced parasitic capacitance model analysis

Overall parasitic capacitance of each ESD protection device consists of three parts, as shown in Fig.1: the bonding pad capacitance $C_{\rm Pad}$, the capacitance associated with metal interconnection $C_{\rm M}$, and the ESD device intrinsic capacitance $C_{\rm Si}$. Hence, the total ESD-induced parasitic capacitance $C_{\rm ESD}$ of ESD protection device is

$$C_{\rm ESD} = C_{\rm M} + C_{\rm Pad} + C_{\rm Si}. \quad (1)$$

†E-mail: wangyuan@ime.pku.edu.cn

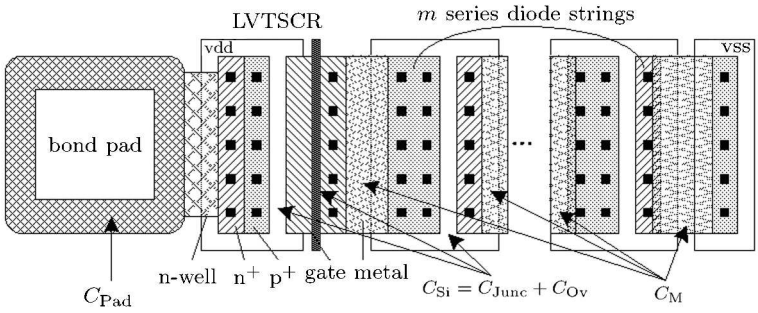


Fig.1. Layout of a kind of ESD protection structure with various ESD-induced parasitic capacitances.

The bonding pad capacitance $C_{\rm Pad}$ is determined by the bonding pad opening rule for a certain CMOS process. In general, the design rules of the minimum passivation opening width and the minimum metal enclosure of the pad are implemented to minimize $C_{\rm Pad}$. In the 0.35μm 1P3M silicide CMOS process, the minimum dimension of a bond pad window including covering metal is $90 \times 90\mu{\rm m}^2$, and $C_{\rm Pad}$ is about 200fF.

Study of the layout suggests that the main source of the parasitic interconnected metal capacitance $C_{\rm M}$ comes from ESD metal lines associated with inter-layer capacitances, including metal-to-diffusion, metal-to-substrate, inter-metals, as well as metal-to-polysilicon, which exist in any ESD structure. Because of the lower capacitance per unit area of less than 0.05fF/$\mu{\rm m}^2$ in the 0.35μm 1P3M silicide CMOS process (as shown in Table 1), $C_{\rm M}$ is always neglected,

Table 1. Interconnected metal capacitance per unit area in a 0.35μm 1P3M silicide CMOS process.

Inter-Layer		$C_{\rm M}$/F/$\mu{\rm m}^2$
From	To	
Metal1	Polysilicon	5.06×10^{-17}
Metal1	Diffusion	3.68×10^{-17}
Metal1	Substrate	2.54×10^{-17}
Metal2	Metal1	3.55×10^{-17}
Metal2	Polysilicon	1.57×10^{-17}
Metal2	Diffusion	1.41×10^{-17}
Metal2	Substrate	1.22×10^{-17}
Metal3	Metal2	3.55×10^{-17}
Metal3	Metal1	1.39×10^{-17}
Metal3	Polysilicon	9.32×10^{-18}
Metal3	Diffusion	8.70×10^{-18}
Metal3	Substrate	7.97×10^{-18}

whereas it cannot be ignored in the advanced high-density IC design which has a large area of metal. To reduce the total $C_{\rm M}$, the device with a high area-efficient ESD level should be selected.

The ESD device intrinsic capacitance $C_{\rm Si}$ is twofold: the junction capacitance $C_{\rm Junc}$ and the gate overlap capacitance $C_{\rm Ov}$.

In general, the pn junction capacitance is the combination of the depletion capacitance $C_{\rm Dep}$ and the diffusion capacitance $C_{\rm Diff}$. The depletion capacitance $C_{\rm Dep}$ is caused by the major carriers in the pn junction potential barrier. With the variation of bias voltage, electrons in n-region and holes in p-region are 'deposited in' or 'taken away from' the barrier region, which results in the changes of barrier width and quantities of the charge in barrier region. This characteristic is similar to the charging and discharging functions of capacitances. Therefore, this pn junction capacitance performance is named as the depletion capacitance $C_{\rm Dep}$. And, the diffusion capacitance $C_{\rm Diff}$ is caused by injected minority carriers under the forward-bias status. With the forward voltage, a number of minority and majority carriers are accumulated in the diffusion region. With variation of forward voltage, the densities of the accumulated carriers are changed, thus forming the diffusion capacitance $C_{\rm Diff}$. Under the circuit normal operation, ESD protection circuit should be in off-state, which means that the pn junction of the ESD device is in the reverse-bias status. Hence, for an ESD device, its pn junction capacitance is only equal to the reverse-bias depletion capacitance, $C_{\rm Junc} = C_{\rm Dep}$. Under the reverse-bias condition, the depletion capacitance is decreased with the increase of reverse voltage, given by

$$C_{\rm Dep}(V) = A_{\rm eff} \cdot \left[\frac{\varepsilon_0 \varepsilon_{\rm Si} q N_{\rm A} N_{\rm D}}{2(N_{\rm A}+N_{\rm D})(V_{\rm D}-V)}\right]^{1/2} \propto \left(1-\frac{V}{V_{\rm D}}\right)^{1/2}, \quad (2)$$

where A_{eff} is the pn effective junction area, N_{A} and N_{D} are the carrier densities of acceptor and donor, and V_{D} is the junction contact potential.

The gate overlap capacitance C_{Ov} exists between drain/source and gate for a MOSFET device. Since the source and gate of a MOSFET ESD device is generally connected with the ground, the source/gate overlap C_{gs} can be neglected. Hence, the gate overlap C_{Ov} can be expressed as

$$C_{\text{Ov}} = C_{\text{gd}} + C_{\text{gs}} \approx C_{\text{gd}} = C_{\text{OvW}} \cdot W_{\text{g}}, \qquad (3)$$

where C_{OvW} is the drain/gate overlap capacitance per gate width, and W_{g} is the width of gate.

Table 2. ESD device intrinsic parasitic capacitance in a 0.35 μm 1P3M silicide CMOS process.

pn junction type	$C_{\text{DepA}}/(\text{F}/\mu\text{m}^2)$	$C_{\text{DepP}}/(\text{F}/\mu\text{m})$
n-well/p-sub	1.44×10^{-16}	4.26×10^{-16}
n-diff/p-sub	1.09×10^{-15}	2.35×10^{-16}
p-diff/n-well	1.36×10^{-15}	2.98×10^{-16}
Capacitance per gate width $C_{\text{OvW}} = 4\times10^{-16}$ (F/μm)		

Table 2 shows ESD-induced intrinsic parasitic capacitance in a 0.35μm 1P3M CMOS process, including the gate oxide capacitance per gate width C_{OvW}, the pn junction capacitances per unit bottom area C_{DepA} and per unit sidewall periphery C_{DepP}.

2.1. Parasitic capacitance for different ESD protection device

The intrinsic capacitances of different ESD protection structures are analysed as follows.

For a single diode, its intrinsic capacitance $C_{\text{Si-Diode}}$ is equal to its pn junction depletion capacitance C_{Dep}.

For a MOSFET device, its parasitic intrinsic capacitance $C_{\text{Si-MOSFET}}$ is a combination of the drain/gate and source/gate overlap oxide capacitances C_{gd} and C_{gs}, and drain/bulk and source/bulk pn junction capacitances C_{db} and C_{sb}, as shown in Fig.2(a). Since the source, bulk and gate for MOSFET are all connected with the ground, C_{gs} and C_{sb} can be neglected. Hence, its intrinsic parasitic capacitance $C_{\text{Si-MOSFET}}$ can be given by

$$C_{\text{Si-MOSFET}} = C_{\text{gd}} + C_{\text{db}} = C_{\text{OvW}} \cdot W_{\text{g}} + C_{\text{DepA}} \cdot W_{\text{g}} \cdot L_{\text{ND}} + C_{\text{DepP}} \cdot 2(W_{\text{g}} + L_{\text{ND}}), \qquad (4)$$

where C_{DepA} and C_{DepP} are the junction parasitic capacitance per unit bottom area and that per unit sidewall periphery, respectively; L_{ND} is the length of drain diffusion. In general, the parameter W_{g} determines the ESD robustness level, so $C_{\text{Si-MOSFET}}$ will depend strongly on L_{ND}. The parameter L_{ND} needs to be further optimized to reduce $C_{\text{Si-MOSFET}}$ for RF ICs, which can be done by decreasing the number of drain-diffusion contact rows.

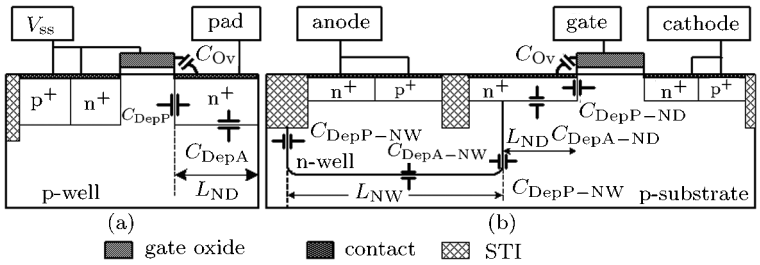


Fig.2. Cross-sections of various ESD devices with associated parasitic capacitances: (a) MOSFET, (b) LVTSCR.

Another ESD structure is the SCR device and its modified structure, LVTSCR. A cross-section of LVTSCR is shown in Fig.2(b). Different from the normal SCR, a saddle n+ diffusion is inserted near the surface at the n-well edge and a 'helper-trigger' MOSFET is built in parallel with the SCR. The intrinsic capacitance of LVTSCR, $C_{\text{Si-LVTSCR}}$, is given by

$$C_{\mathrm{Si-LVTSCR}} = C_{\mathrm{DepA-NW}} \cdot L_{\mathrm{NW}} \cdot W_{\mathrm{NW}} + C_{\mathrm{DepP-NW}} \cdot 2(L_{\mathrm{NW}} + W_{\mathrm{NW}}) + C_{\mathrm{OvW}} \cdot W_{\mathrm{NW}} + C_{\mathrm{DepA-ND}} \cdot L_{\mathrm{ND}} \cdot W_{\mathrm{NW}} + C_{\mathrm{DepP-ND}} \cdot (L_{\mathrm{ND}} + W_{\mathrm{NW}}), \quad (5)$$

where $C_{\mathrm{DepA-NW}}$ and $C_{\mathrm{DepP-NW}}$ are the n-well junction capacitance per unit bottom area and that per unit sidewall periphery, respectively; $C_{\mathrm{DepA-ND}}$ and $C_{\mathrm{DepP-ND}}$ are the saddle n^+ diffusion junction capacitance per unit bottom area and that per unit sidewall periphery, respectively; L_{NW} and W_{NW} are the length and width of n-well, respectively; L_{ND} is the length of saddle n^+ diffusion in the p-substrate. The parameter W_{NW} determines the ESD robustness level of LVTSCR. Similar to $C_{\mathrm{Si-MOSFET}}$, the parameters L_{NW} and L_{ND} should be further optimized to reduce $C_{\mathrm{Si-LVTSCR}}$ by decreasing the number of n^+ and p^+ diffusion contact rows in n-well and the number of saddle n^+ diffusion contact rows in p-substrate.

Figure 3 shows the intrinsic capacitance and layout areas of various ESD structures, including diode, gate-grounded NMOS (ggNMOS), gate-coupled NMOS (gcNMOS), and LVTSCR, with the same ESD

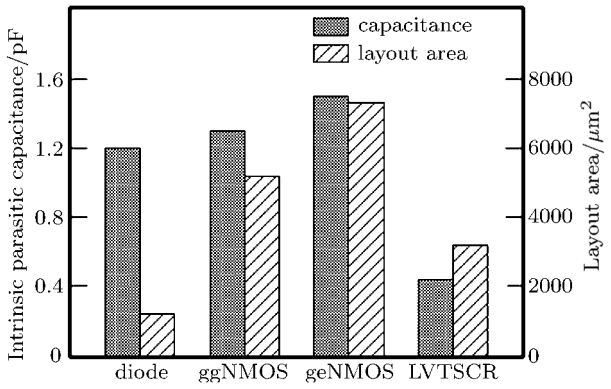


Fig.3. Intrinsic capacitance and layout area of various ESD structure.

robustness target about 5kV human body model (HBM) in a 0.35μm 1P3M silicide CMOS process. Because of their low area-efficient ESD level, the diode, ggNMOS, and gcNMOS have a large layout area and a huge ESD-induced parasitic capacitance. With a 5kV HBM ESD target, the intrinsic capacitance of the diode is about 1.2pF, that of ggNMOS is about 1.3pF, and that of gcNMOS is about 1.5pF. The increase of the gcNMOS capacitance originates from the capacitance of its additive RC circuit. Such a large capacitance is intolerable for RF applications of devices that are very sensitive to parasitic effects. Maybe the LVTSCR is a good choice. The intrinsic capacitance of LVTSCR is about 440fF, including pn junction capacitance, and 'help-trigger' MOSFET's gate overlap capacitance.

2.2. Low-parasitic capacitance strategy

Although the LVTSCR has the lowest parasitic capacitance in all ESD structure, the total ESD-induced parasitic capacitance is close to a magnitude of ~pF level because of the bonding pad and the interconnected metal capacitances as shown in Eq.(1). Hence, a low-parasitic capacitance strategy for RF ESD protection still needs to be given. An approach is the series diode string (SDS) structure, reported in Ref.[5]. One believes that the intrinsic parasitic capacitance of the SDS structure is rapidly reduced when the series diode number m is increased. For an m-stage SDS structure, its intrinsic parasitic capacitance $C_{\mathrm{Si-SDS}}$ can be given by

$$C_{\mathrm{Si-SDS}} = C_{\mathrm{Si-Diode}}/m. \quad (6)$$

When m is increased, though the total device area increases, it is interesting to find that $C_{\mathrm{Si-SDS}}$ is decreased instead of increased. Apparently, a low parasitic capacitance may be obtained in a poor area-efficient diode device. However, since $C_{\mathrm{Si-Diode}}$ of a single diode is sizeable, the layout cost of the SDS structure is excessively expensive to reduce its capacitance, which is beyond the endurance of the today high-density-pin ICs.

Our solution is the LVTSCR-SDS structure, the layout of which is also shown in Fig.1. In the LVTSCR-SDS structure, the LVTSCR device is used to achieve the required ESD robustness level because of its high area-efficient ESD level, and the SDS structure is used to reduce the intrinsic parasitic capacitance. For an m-stage LVTSCR-SDS structure, its intrinsic parasitic capacitance $C_{\mathrm{Si-LVTSCR-SDS}}$ can be expressed as

$$C_{\mathrm{Si-LVTSCR-SDS}} = \left(\frac{1}{C_{\mathrm{Si-LVTSCR}}} + \frac{m}{C_{\mathrm{Si-Diode}}}\right)^{-1} = \frac{C_{\mathrm{Si-LVTSCR}} C_{\mathrm{Si-Diode}}}{C_{\mathrm{Si-Diode}} + m C_{\mathrm{Si-LVTSCR}}}. \quad (7)$$

Obviously, $C_{\mathrm{Si-LVTSCR-SDS}}$ is decreased with the increase of the stage diode number m.

Figure 4 shows the $C_{\mathrm{Si-LVTSCR-SDS}}$ versus the series diode number m. It is illustrated that $C_{\mathrm{Si-LVTSCR-SDS}}$ is decreased from 440 to 29fF when m is increased from 0 to 9. However, according to Eq.(1), the total ESD-induced parasitic capacitance C_{ESD} is not only determined by the ESD device intrinsic capacitance C_{Si}, but also by the bonding pad capacitance C_{Pad} and the interconnected metal capacitance C_{M}. Especially for the LVTSCR-SDS structure, although $C_{\mathrm{Si-LVTSCR-SDS}}$ is decreased when m is increased, C_{Pad} is almost a constant and C_{M} is even increased because of the increase of the total metal area. Obviously, the total parasitic capacitance C_{ESD} is not a monotonically decreasing function of m. When m is small, $C_{\mathrm{Si-LVTSCR-SDS}}$ is the primary factor and C_{ESD} is decreased with the increase of m. Whereas when m is large, $C_{\mathrm{Si-LVTSCR-SDS}}$ is decreased less than the increase of C_{M}, so C_{ESD} is increased with the increase of m.

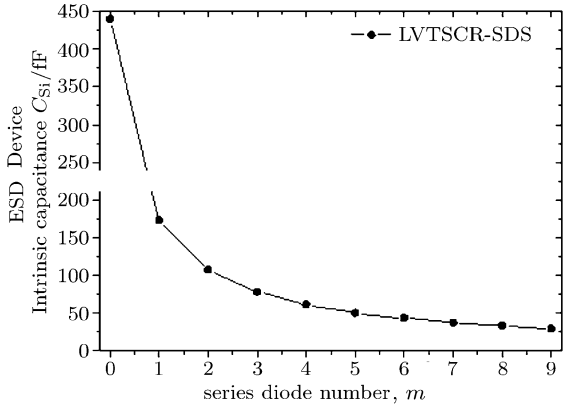


Fig.4. Extracted intrinsic parasitic capacitance $C_{\mathrm{Si-LVTSCR-SDS}}$ with different series diode number m.

The curve of $C_{\mathrm{ESD-LVTSCR-SDS}}$ versus m is shown in Fig.5. When m is increased from 0 to 3, $C_{\mathrm{ESD-LVTSCR-SDS}}$ is decreased from 640 to 310fF. However, when m is increased from 4 to 9, $C_{\mathrm{ESD-LVTSCR-SDS}}$ is increased slightly from 310 to 337fF. In $C_{\mathrm{ESD-LVTSCR-SDS}}$, C_{Pad} is a constant of about 200fF; $C_{\mathrm{Si-LVTSCR-SDS}}$ is decreased with the increase of m, but C_{M} is increased with the increase of m. Hence, it is illustrated that when m is equal to 2 or 3 the minimum $C_{\mathrm{ESD-LVTSCR-SDS}}$ about 310fF could be acquired. In the next section, experimental results also show that the LVTSCR-SDS structure with 2 or 3 series diodes has the best ESD performance.

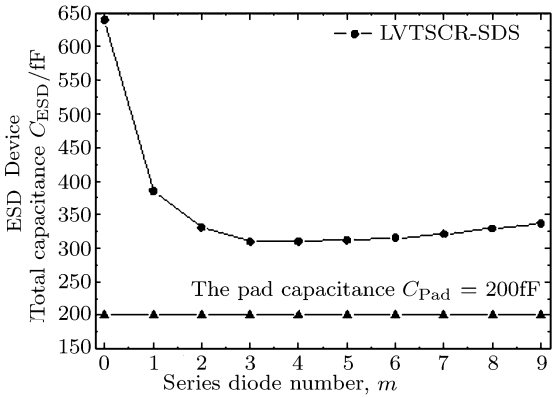


Fig.5. Extracted total parasitic capacitance $C_{\mathrm{ESD-LVTSCR-SDS}}$ with different series diode number m.

3. Leakage current model analysis

Another prominent ESD-induced parasitic effect is the leakage current. Compared with the SDS structure, the novel LVTSCR-SDS structure also has a low leakage performance.

For a standard CMOS process with a p-type substrate, a single diode is made of a parasitic vertical p-n-p bipolar transistor instead of an ideal pn junction diode. Hence, as shown in Fig.6, an m-stage p-n-p-based diode string will form a p-n-p series string in a Darlington configuration whose front-stage base is connected with the next-stage emitter. And all the parasitic p-n-p transistors have a common collector connected with the substrate. Each stage diode contributes its collector current to the substrate as the

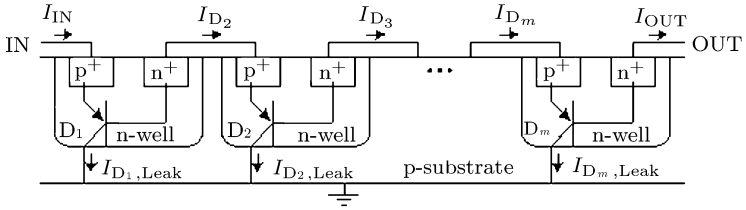


Fig.6. Cross-section of the m-stage SDS ESD protection structure.

leakage current and transfers its base current to the next-stage diode emitter, described by

$$\begin{aligned}
&I_{\mathrm{D}_1} = I_{\mathrm{IN}}, \quad I_{\mathrm{D}_1,\mathrm{Leak}} = \frac{\beta}{\beta+1} I_{\mathrm{D}_1} = \frac{\beta}{\beta+1} I_{\mathrm{IN}},\\
&I_{\mathrm{D}_2} = \frac{1}{\beta+1} I_{\mathrm{IN}}, \quad I_{\mathrm{D}_2,\mathrm{Leak}} = \frac{\beta}{(\beta+1)^2} I_{\mathrm{IN}},\\
&\cdots\\
&I_{\mathrm{D}_m} = \frac{1}{(\beta+1)^{m-1}} I_{\mathrm{IN}}, \quad I_{\mathrm{D}_m,\mathrm{Leak}} = \frac{\beta}{(\beta+1)^m} I_{\mathrm{IN}},\\
&I_{\mathrm{OUT}} = \frac{1}{(\beta+1)^m} I_{\mathrm{IN}},
\end{aligned} \tag{8}$$

where I_{D_i} and $I_{\mathrm{D}_i,\mathrm{Leak}}$ are the diode forward current and substrate leakage current of the i-stage diode, respectively; and I_{IN} and I_{OUT} are the inflow and outflow currents of the total diode string, respectively. Hence, the total leakage current $I_{\mathrm{SDS,Leak}}$ of the SDS is

$$I_{\mathrm{SDS,Leak}} = \sum_{i=1}^{m} I_{\mathrm{D}_i,\mathrm{Leak}} = I_{\mathrm{IN}} - I_{\mathrm{OUT}} = I_{\mathrm{IN}} \left[1 - \frac{1}{(\beta+1)^m}\right] \approx I_{\mathrm{IN}}. \tag{9}$$

The inflow current I_{IN} of the SDS is unity before the diode string turns on. Under the power voltage about 3.3V, for a 6-stage SDS, the voltage shared by each stage diode is about 0.55V (less than the diode turn-on voltage about 0.65V). Hence, I_{IN} can be estimated by

$$I_{\mathrm{IN}} = I_{\mathrm{s}} \exp\left(\frac{V}{kT/q}\right) = I_{\mathrm{s}} \exp\left(\frac{0.55}{0.026}\right) \approx I_{\mathrm{s}} \times 10^9. \tag{10}$$

In general, the saturation current I_{S} is of the magnitude of ∼fA in a 0.35μm CMOS process.[6] According to Eqs.(9) and (10), the total SDS leakage current, $I_{\mathrm{SDS,Leak}}$, is approximately equal to the inflow current, I_{IN}, i.e. about the order of $\sim \mu$A. Such a large leakage current is lethal to RF ICs.

Next, the leakage current of an m-stage LVTSCR-SDS structure is analysed. As shown in Fig.7, the inflow current I_{IN} of the LVTSCR device is divided

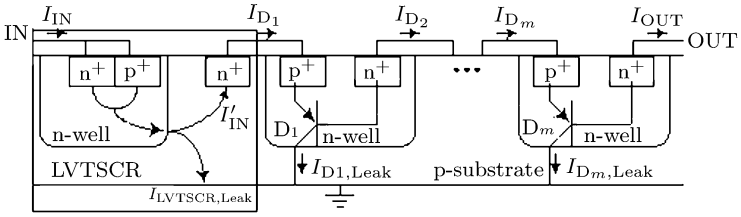


Fig.7. Cross-section of the m-stage LVTSCR-SDS ESD protection structure.

into two parts: the LVTSCR leakage $I_{\mathrm{LVTSCR,Leak}}$ and the inflow current I'_{IN} of the next diode string, described as

$$\begin{aligned}
&I_{\mathrm{IN}} = I'_{\mathrm{IN}} + I_{\mathrm{SCR,Leak}},\\
&I_{\mathrm{D}_1} = I'_{\mathrm{IN}}, \quad I_{\mathrm{D}_1,\mathrm{Leak}} = \frac{\beta}{\beta+1} I'_{\mathrm{IN}},\\
&\cdots\\
&I_{\mathrm{D}_m} = \frac{1}{(\beta+1)^{m-1}} I_{\mathrm{IN}}, \quad I_{\mathrm{D}_m,\mathrm{Leak}} = \frac{\beta}{(\beta+1)^m} I_{\mathrm{IN}},\\
&I_{\mathrm{OUT}} = \frac{1}{(\beta+1)^m} I'_{\mathrm{IN}}.
\end{aligned} \tag{11}$$

The SDS leakage current $I_{\mathrm{SDS,Leak}}$ and the total LVTSCR-SDS leakage current $I_{\mathrm{LVTSCR-SDS,Leak}}$ are given by

$$\begin{aligned} I_{\mathrm{DS,Leak}} &= I'_{\mathrm{IN}} - I_{\mathrm{OUT}} = I'_{\mathrm{IN}} \left[1 - \frac{1}{(\beta+1)^m}\right] \approx I'_{\mathrm{IN}}, \\ I_{\mathrm{LVTSCR-SDS,Leak}} &= I_{\mathrm{LVTSCR,Leak}} + I_{\mathrm{SDS,Leak}} \approx I_{\mathrm{IN}}. \end{aligned} \tag{12}$$

By comparing Eq.(12) with Eq.(9), although the leakage currents of the two diode strings are almost equal to the inflow current I_{IN}, the I_{IN} of the LVTSCR-SDS is less than that of the SDS structure. For a SCR device, I_{IN} is equal to its forward-blocking current, which is of a magnitude of ∼nA in a 0.35μm CMOS process.[7,8] Apparently, inserting a LVTSCR device in the SDS structure is greatly helpful to improving its leakage performance.

4. Experiments and results

To testify our novel systemic ESD-induced parasitic model, the above ESD protection structures are implemented in a 0.35μm 1P3M silicide CMOS process. Besides the pure-SDS (Fig.8(a)), to calculate the variation of the parasitic effects with different series diode number, the LVTSCR-SDS are fabricated with various diode numbers from 2 to 6 (Fig.8(e)), with a fixed ESD robustness target about 5kV human body model (HBM). Moreover, three modified diode strings are also made in the same test chip, including the clad-SDS (Fig.8(b)), boost-SDS (Fig.8(c)), and cantilever-SDS structures (Fig.8(d)), which have been reported to have eliminated the Darlington effect.[9] The leakage current performance and I–V characteristic of the chip are measured by the Agilent semiconductor parameter analyser 4156C. And the ESD robustness performance is tested by the ESD & Latchup test equipment KEYTEK ZAPMASTER 7/4. The photograph of the test chip is shown in Fig.9.

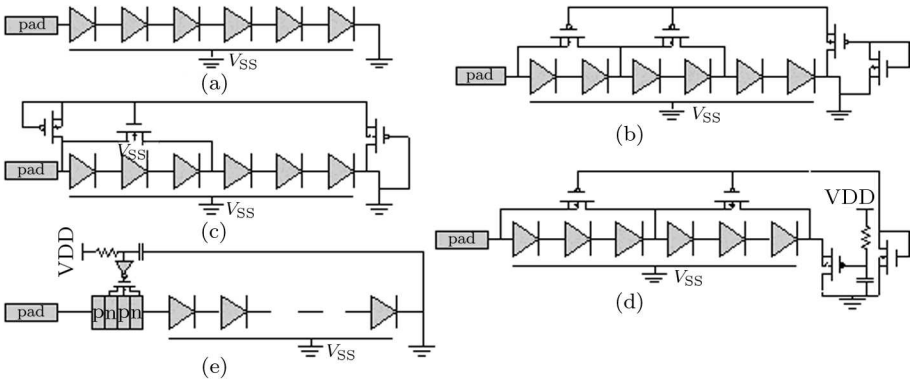


Fig.8. Schematic diagrams of the (a) Pure-, (b) Clad-, (c) Boost-, (d) Cantilever-, (e) LVTSCR-SDS structure.

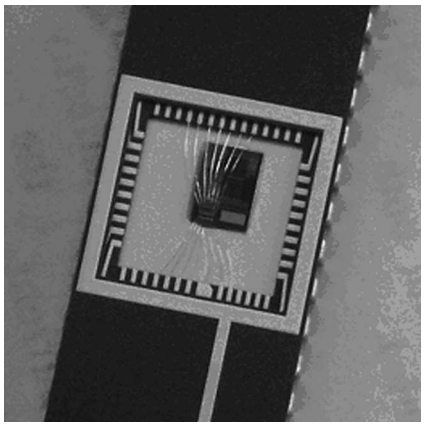


Fig.9. Photograph of test chip.

4.1. Leakage current performance

The measured leakage currents of the various ESD structures are illustrated in Fig.10, including the pure-, clad-, boost-, cantilever-, and LVSCR-SDS structures. It is clear that the leakage currents of the former four traditional SDS structures are all at $\sim \mu$A level. Under the power voltage about 3.3V, the leakage current of the pure-SDS is about 3.3μA. The clad-SDS is about 3μA. The cantilever-SDS is about 1μA. And the boost-SDS is about 0.5μA. Obviously, such a large leakage current level is intolerable for RF ICs which are very sensitive to parasitic effects. The measured

leakage currents of the LVTSCR-SDS structure with various diode numbers are shown in Fig.11. Under the power voltage of 3.3V, the $I_{\mathrm{LVTSCR-SDS,Leak}}$ of the LVTSCR-SDS is about 12.2nA. Since the series diode string scarcely contributes to the total leakage current, the leakage current is quasi-constant when the series diode number is increased. Hence, the ∼nA-level LVTSCR-SDS structure is preferable to the ∼μA-level traditional SDS structure for the RF ESD protection. Moreover, the spurious values in Figs.10 and 11 originate from the noise of the testing equipments, which is neglected in our analysis.

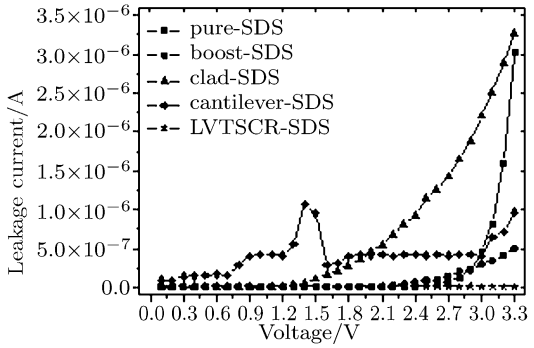


Fig.10. Measured leakage currents I_{Leakage} of various ESD structures.

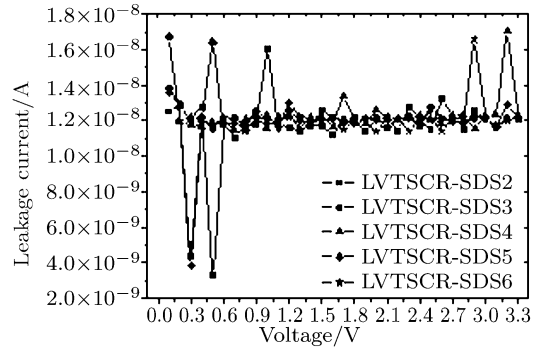


Fig.11. Measured leakage currents $I_{\mathrm{LVTSCR-SDS,Leak}}$ with different series diode number m.

4.2. I–V characteristic

The measured I–V characteristics of the diode strings together with four traditional ESD designs are shown in Fig.12. The trigger voltages of the pure-, clad-, boost- and cantilever-SDS structure are about 3.9, 3.7, 4.5 and 5.4V, respectively. The peak current is 50mA which is determined by the measuring equipment. To protect the equipment, a peak current about 50mA is limited by the Agilent semiconductor parameter analyser 4156C.

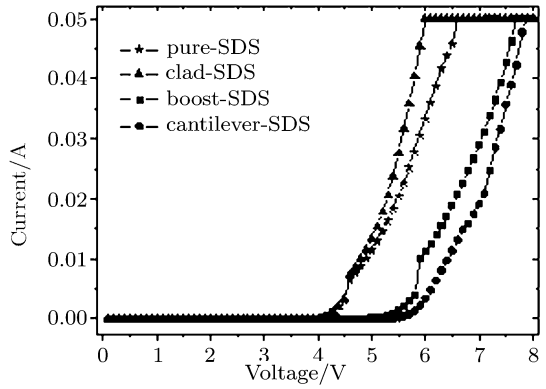


Fig.12. Measured I–V characteristics of the four traditional series diode string structure.

The measured I-V characteristics of the LVSCR-SDS structure with different series diode numbers are shown in Fig.13. The trigger voltages of the LVSCR-SDS device are about 8 to 9V. Moreover, Fig.13 shows that the increasing speed of the current with the voltage becomes gradually slow when the series diode number m is increased. A sharp slope of the I-V characteristic is beneficial to the discharge of the ESD current, whereas a gently slope is harmful. When the series diode number is increased, the parasitic turn-on resistance R_{ESD} of ESD structure is increased because the parasitic resistance is also in series. Too large a R_{ESD} will hamper the discharge of ESD current. Obviously, a large number of series diodes are not recommended for the LVSCR-SDS structure for ESD protection. It is found that a LVSCR-SDS structure with 2 or 3 series diodes may be optimal.

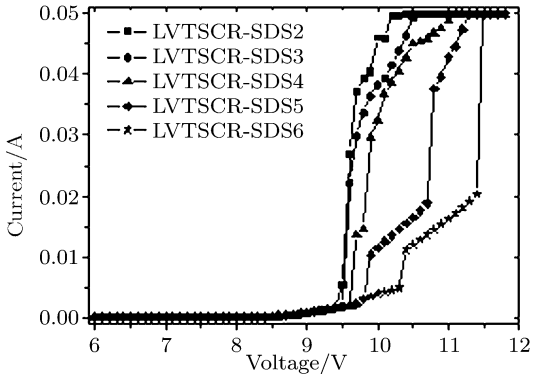


Fig.13. Measured I-V characteristics of the LVSCR-SDS structure with different series diode number m.

4.3. ESD performance

The measured ESD failure voltages of various ESD protection structures are shown in Fig.14. The ESD failure voltage of the pure-, clad-, boost-, and cantilever-SDS structures are equal to 2, 2.5, 2, and 2.5kV, respectively. With the same layout-size diode, the ESD failure voltage of the LVTSCR-SDS structures with different series diode numbers is decreased

from 5 to 2.5kV when the diode number is increased from 2 to 6. It is also clear that a LVSCR-SDS structure with 2 or 3 series diodes has the best ESD performance.

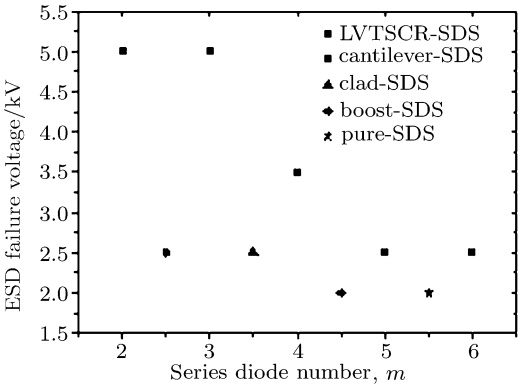


Fig.14. Measured ESD failure voltage of various ESD protection structure.

5. Conclusion

In summary, in this paper, a systemic and comprehensive ESD-induced parasitic model has been presented, which is used to analyse the parasitic influences of ESD protection circuits on the performance of RF ICs. This novel model can accurately estimate ESD-induced parasitic capacitance and leakage current, instead of the costly and time-consuming iterative experimental methods. Using this model, a novel low-parasitic ESD protection structure, LVTSCR-SDS structure, is made in a 0.35μm 1P3M silicide CMOS process. This novel model also can help to determine the most suitable series diode number m of the LVTSCR-SDS structure. Analytical and experimental results show that a LVTSCR-SDS structure with 2 or 3 series diodes has the lowest parasitic capacitance about 310fF and a low leakage current about 12.2nA with a fixed ESD robustness target about 5kV HBM.

Acknowledgment

The authors would like to thank Fu Yilin, Han Dedong, and Zhang Ganggang for their support for this work.

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