Vol 15 No 1, January 2006
1009-1963/2006/15(01)/0195-04

Chinese Physics

© 2006 Chin. Phys. Soc.
and IOP Publishing Ltd

Fabrication and characterization of groove-gate MOSFETs based on a self-aligned CMOS process*

Ma Xiao-Hua(马晓华)[a)b)†], Hao Yue(郝 跃)[a)b)], Sun Bao-Gang(孙宝刚)[c)], Gao Hai-Xia(高海霞)[a)b)], Ren Hong-Xia(任红霞)[a)b)], Zhang Jin-Cheng(张进城)[a)b)], Zhang Jin-Feng(张金凤)[a)b)], Zhang Xiao-Ju(张晓菊)[a)b)], and Zhang Wei-Dong(张卫东)[d)]

[a)] *Microelectronics Institute, Xidian University, Xi'an 710071, China*

[b)] *Key Laboratory of Ministry of Education for Wide Band-gap Semiconductor Materials and Devices, Xidian University, Xi'an 710071, China*

[c)] *Microelectronics Institute, Chinese Academy of Sciences, Beijing 100029, China*

[d)] *School of Design, Engineering and Computing, Bournemouth University, UK*

(Received 29 March 2005; revised manuscript received 9 September 2005)

N and P-channel groove-gate MOSFETs based on a self-aligned CMOS process have been fabricated and characterized. For the devices with channel length of 140nm, the measured drain induced barrier lowering (DIBL) was 66mV/V for n-MOSFETs and 82mV/V for p-MOSFETs. The substrate current of a groove-gate n-MOSFET was 150 times less than that of a conventional planar n-MOSFET. These results demonstrate that groove-gate MOSFETs have excellent capabilities in suppressing short-channel effects. It is worth emphasizing that our groove-gate MOSFET devices are fabricated by using a simple process flow, with the potential of fabricating devices in the sub-100nm range.

Keywords: self-aligned, groove-gate MOSFETs, DIBL, short-channel effects
PACC: 7280C, 7340R, 7360J

1. Introduction

To achieve high speed and high integrating density in very large scale integration (VLSI) circuits, the size of MOSFETs has been continuously scaled down. As the effective channel length enters into deep submicron or super-deep submicron regime, short-channel effects, such as hot carrier effect (HCE) and drain-induced barrier lowering (DIBL), are becoming critical problems.[1] In order to achieve smaller channel length while with short channel effects restrained, new device structures and fabrication processes, such as the Fin-FET and Tri-FET, were proposed.[2,3] The double lightly doped drain (LDD) concave device was reported,[4,5] in which short-channel effect had been reduced. However, compared with that of planar device, parasitic capacitance of that device is larger due to the large overlap of gate polysilicon with source and drain areas, especially when the thickness of oxide is under nanometre level. And non-planar silicon-on-insulator (SOI) V-groove-gate n-MOSFETs have been reported recently.[6] By adopting the KOH self-limiting etching and anisotropic etching, a 36nm channel length n-MOSFET was obtained. But the V-groove p-MOSFET can not be fabricated using the above techniques.[6–8]

In this paper, a process flow for fabricating groove-gate planar self-aligned CMOS devices, its schematic structure being shown in Fig.1, is presented and the experimental results of the groove-gate CMOS transistors with physical channel length (L_g) of 140nm are discussed. We found that the short channel effects were reduced significantly in the groove-gate MOSFETs. Furthermore, most of the layout masks for the groove-gate MOSFET are same as those for the conventional planar MOSFET, and the number of process steps is reduced.

2. Device fabrication

The groove-gate MOSFETs, whose schematic

*Project supported by the National Natural Science Foundation of China (Grant No 60376024).

†E-mail: xhma@xidian.edu.cn

structure is shown in Fig.1, were fabricated on a 6-inch P-type silicon (100) wafer. The masks of a conventional planar CMOS process were used except that the size of poly-gate mask was diminished. A 25nm thermal SiO_2 film was grown as the mask for well implantation. The P^{31-}(150keV, $1.1\times10^{13}cm^{-2}$) was implanted to form N-well and the B^{11+}(150keV, $1.2\times10^{13}cm^{-2}$) to form P-well. The active area was then defined. The As^{75-} was implanted to form N^{++} (45keV, $4\times10^{15}cm^{-2}$) source/drain for n-MOSFET and BF_2 (25keV, $3\times10^{15}cm^{-2}$) to form P^{++} source/drain for p-MOSFET.

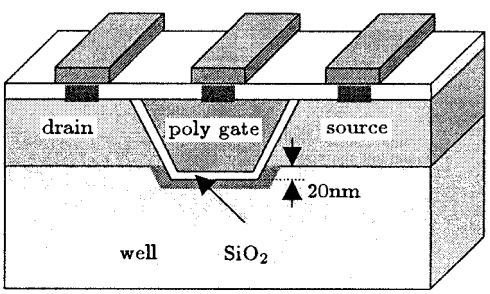


Fig.1. Schematic structure of the groove-gate MOSFETs.

After rapid thermal annealing (RTA) at 1005°C for 5s, groove etching was carried out in the following steps. First, a hard oxide mask on top of the N^{++} and P^{++} areas was patterned by a combination of electron-beam lithography and reactive ion etching (RIE), so that the groove area was defined. The silicon in the opening was then etched away by RIE to form the groove, the bottom of which was 20nm below the N^{++} and P^{++} regions. The etching procedure defines the gate areas and the source/drain regions. Thereafter, to adjust the threshold voltage, a 6nm sacrificial SiO_2 was grown to cap the silicon. As^{75-} (for n-MOSFET) and B^{11+} (for p-MOSFET) were implanted into the bottoms of the groove. The sacrificial SiO_2 was then removed, and a 5nm thermal SiO_2 film was grown as the gate dielectric layer at a low temperature of 750°C and annealed at 850°C in a N_2O_2 ambient. A 240nm polysilicon layer was deposited and As^{75-} was implanted. The polysilicon on the wafer surface was removed by chemical mechanical polishing (CMP), which stopped at the oxide surface, and the remained polysilicon in the groove was used as the gate electrode. The self-aligned process was defined by the groove etching and polysilicon CMP steps, and it reduced the parasitic capacitance between the gate and the source/drain regions. Finally, silicide and metal interconnect was formed.

The scanning electron microscope (SEM) images of the device structure is shown in Fig.2. The measured channel length is 140nm, which consists of lengths of the bottom and side edges of the groove below the source/drain regions. Figure 2 shows that the fabrication flow has succeeded in fabricating the desired structure.

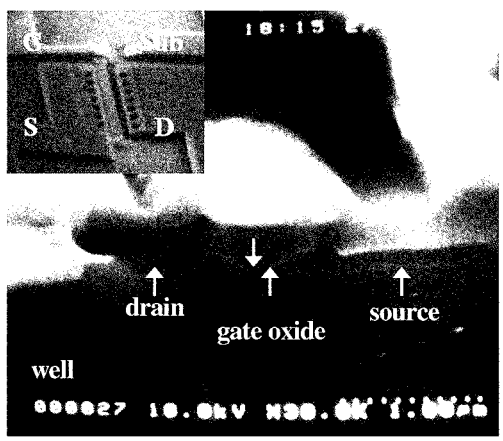


Fig.2. Cross section micrograph with inset SEM image of the top view of a 140nm groove-gate length device.

3. Experimental results and discussion

The devices were tested at room temperature with a HP4156B semiconductor parameter analyser and a signatone S1160 probe station. The $I_D - V_{GS}$ characteristics of the fabricated groove-gate MOSFETs are shown in Fig.3(a) and 3(b). The figures show that the subthreshold slope (S/S) is 114mV/decade at V_{DS}=0.1V for n-MOSFET and 220mV/decade at V_{DS}=–0.1V for p-MOSFET. These transistors exhibit excellent capability of suppressing short channel effects with the DIBL of 66mV/V for n-MOSFET and 82mV/V for p-MOSFET. The gate current of p-MOSFET is about 10pA at V_{DS}=–3.0V and V_{GS} = –3.0V, which proves good oxide quality and very low boron diffusion through the gate oxide. The threshold voltages (V_T) of –1.39V for p-MOSFET and 1.19V for n-MOSFET are obtained. The threshold voltage can be reduced by further process optimization, such as reducing the gate oxide thickness and increasing the concentration of V_T adjusting implantation.

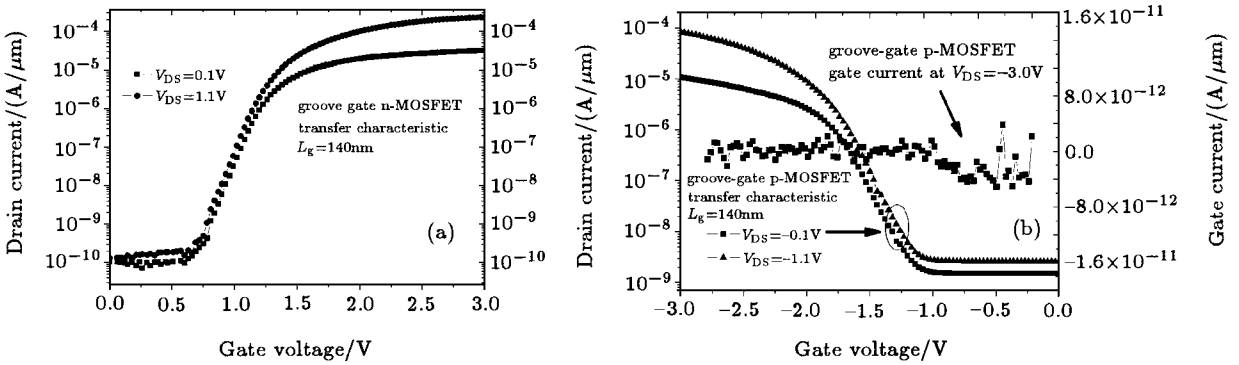


Fig.3. (a) $I_D - V_{GS}$ characteristics of n-MOSFET, (b) $I_D - V_{GS}$ and $I_G - V_{GS}$ characteristics of p-MOSFET.

The $I_D - V_{DS}$ characteristics of the groove-gate transistors are presented in Fig.4. The saturated drain current is 310μA/μm for n-MOSFET and 195μA/μm for p-MOSFET at $|V_{GS}|$ =3.1V and $|V_{DS}|$=3.0V. Figure 5 gives the substrate current of a groove-gate n-MOSFET and a planar n-MOSFET with the same physical parameters. It shows that the substrate current of the groove-gate n-MOSFET is 150 times less than that of the planar n-MOSFET. The groove-gate device exhibits higher immunity to short channel effects such as hot carrier effects and DIBL,[9] while the major electrical parameters are in the same range as those of the conventional devices.

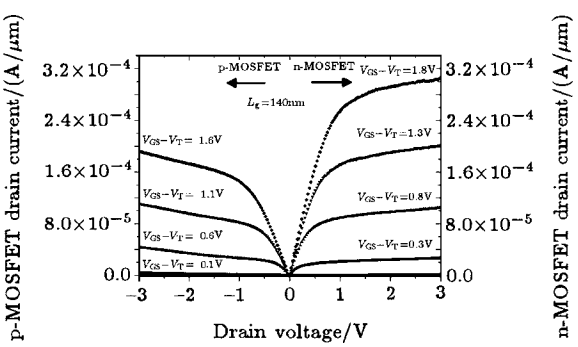


Fig.4. $I_D - V_{DS}$ characteristics of groove-gate n-MOSFET and p-MOSFET.

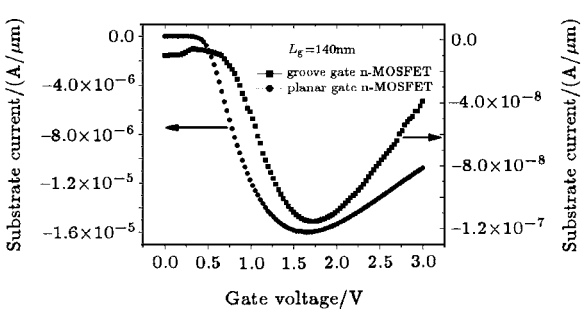


Fig.5. $I_{sub} - V_{GS}$ characteristics of groove-gate and planar-gate n-MOSFET.

4. Conclusion

The new groove-gate CMOS devices based on self-aligned process have been fabricated successfully. Measurement results show that the groove-gate MOSFETs have much better capability of suppressing short channel effects than conventional planar MOSFETs. It should also be noted that these performance enhancements have been achieved by using a process flow that is not much more complicated than that used for fabricating the conventional planar devices, as only one extra step, the groove etching, is required. Most of the layout masks for conventional planar devices can be adopted to fabricate groove-gate devices. The first prototype devices present promising characteristics and very weak short-channel effects.[10] For the next batch of devices, the temperature of gate-oxide formation[11] will be reduced and process conditions will be further optimized. The threshold voltage will be reduced by further process optimization, such as reducing the gate oxide thickness and increasing the dose of V_T-adjusted implantation. The etching precision will be further improved to achieve shorter channel length, and therefore better performance.

References

[1] Wong H, Frank D and Solomon P 1998 *Proc. IEDM98* 407

[2] Fried D M, Duster J S and Kornegay K T 2003 *IEEE Electron Device Lett.* **24** 592

[3] Doyle B S, Datta S, Doczy M *et al* 2003 *IEEE Electron Device Lett.* **24** 263

[4] Sunouchi K, Takato H, Nitayama A *et al* 1988 *Proc. IEDM88* 226

[5] Hieda K, Sunouchi K, Takato H *et al* 1992 *IEEE Trans. Electron Dev.* **39** 671

[6] Appenzeller J, Martel R, Avouris *et al* 2002 *IEEE Electron Device Lett.* **23** 101

[7] Knoch J, Appenzeller J, Lengeler B *et al* 2001 *J. Vac. Sci. Technol.* A **19** 1737

[8] Appenzeller J, Martel R, Solomon P *et al* 2000 *Appl. Phys. Lett.* **77** 298

[9] Ren H X and Hao Y 2001 *Chin. Phys.* **10** 189

[10] Ren H X and Hao Y 2002 *IEEE Solid-State Electronics* **46** 665

[11] Appenzeller J, Alamo D J, Martel R *et al* 2000 *Electrochem. Solid State Lett.* **3** 84