Vol 14 No 9, September 2005
1009-1963/2005/14(09)/1886-06
Chinese Physics
© 2005 Chin. Phys. Soc.
and IOP Publishing Ltd

The conduction mechanism of stress induced leakage current through ultra-thin gate oxide under constant voltage stresses*

Wang Yan-Gang(王彦刚)[a)†], Xu Ming-Zhen(许铭真)[a)‡],
Tan Chang-Hua(谭长华)[a)], Zhang J. F[b)], and Duan Xiao-Rong(段小蓉)[a)]

[a)] *Institute of Microelectronics, Peking University, Beijing* 100871, *China*

[b)] *School of Engineering, Liverpool John Moores University, UK*

(Received 18 March 2005; revised manuscript received 13 April 2005)

The conduction mechanism of stress induced leakage current (SILC) through 2nm gate oxide is studied over a gate voltage range between 1.7V and stress voltage under constant voltage stress (CVS). The simulation results show that the SILC is formed by trap-assisted tunnelling (TAT) process which is dominated by oxide traps induced by high field stresses. Their energy levels obtained by this work are approximately 1.9eV from the oxide conduction band, and the traps are believed to be the oxygen-related donor-like defects induced by high field stresses. The dependence of the trap density on stress time and oxide electric field is also investigated.

Keywords: stress induced leakage current, oxygen-related donor-like defects, trap-assisted tunnelling, ultra-thin gate oxide
PACC: 7360H, 7340Q

1. Introduction

The stress induced leakage current (SILC) is one of the major oxide reliability issues especially for non-volatile memory applications, because it will not only reduce the data retention time of dynamic random access memory and electrically erasable programmable read only memory devices, but also introduce excess power dissipation for the device operation.[1] Many researches[1−9] have been focused on this problem since it was first reported by Maserjian and Zamani at 1982.[3] Based on the tunnelling process, several models had been proposed as possible conduction mechanism of SILC, such as the positive charge-assisted tunnelling,[3] the thermal-assisted tunnelling,[4] the trap-assisted tunnelling (TAT) via a single or several traps[5−8] and so on.

It is well known that SILC is related to defects produced in oxide during high field stresses, and the former study[9] had shown that these defects are predominantly neutral electron traps which can be generated by anode hole injection. Although the two-step TAT model[5] showed best consistency with experimental results and qualitatively explained the dependence of SILC on oxide thickness (t_{ox}), the properties of defects controlling the TAT process have not been fully understood as the t_{ox} scaling down to 2nm so far.

The purpose of this paper is to investigate the SILC conduction mechanism of ultra-thin gate oxide and to determine the properties of the traps controlling SILC based on the simulation method.

2. Devices and experiments

The testing devices are p^+ polysilicon gate p-MOSFETs ($W/L = 28/1$) fabricated by standard 0.13μm CMOS technology. The oxide films were thermally grown SiO_2 with physical thicknesses 1.9 and 2.15nm, and the gate oxide area (A_{ox}) is 2.8×10^{-5}cm^2.

The constant voltage stress (CVS) was applied to the gate ($V_{g,stress}$=–3.5V, –3.8V to 1.9 and 2.15nm oxides respectively) with source, drain and substrate

*Project supported by the Special Foundation for State Major Basic Research Program of China (Grant No TG2000-036503).
†E-mail: wangyg@ime.pku.edu.cn
‡Corresponding author. E-mail: mxu@ime.pku.edu.cn

grounded, and the test temperatures were 300K and 378K. The gate current versus gate voltage ($I_g - V_g$) measurements were performed by HP4145B semiconductor parameter analyser after each cycle of stress.

3. Results and discussions

Figure 1(a) and (b) show the typical evolution of $\Delta I_g - V_g$ against stress time (t_{st}) for some devices with different oxide thicknesses at 300K and 378K respectively. The increment of gate current ΔI_g is the difference between I_g after and before stress. This would eliminate the effect of the background current on ΔI_g. SILC is defined as the ΔI_g before oxide breakdown, and it shows a continuous increase with stress time.

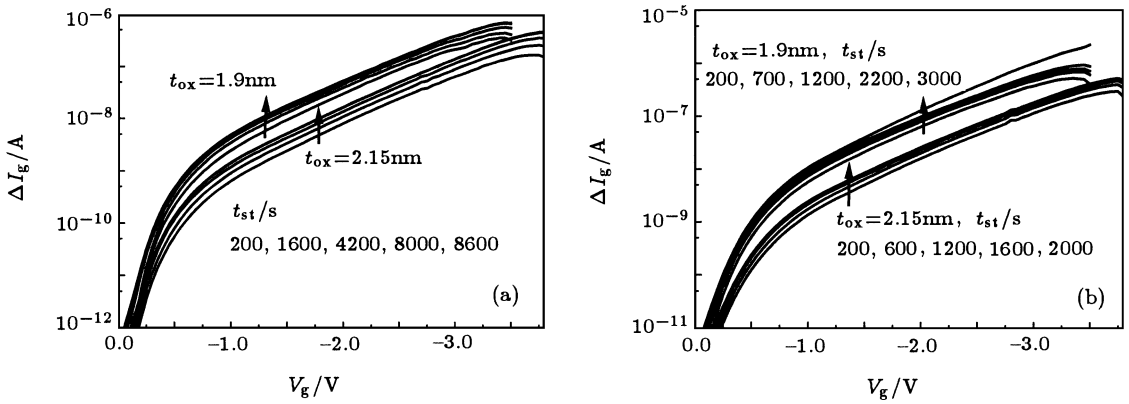


Fig.1. The $\Delta I_g - V_g$ characteristics of p-MOSFET under CVS for t_{ox}=1.9nm and 2.15nm at (a) T=300K, (b) T=378K.

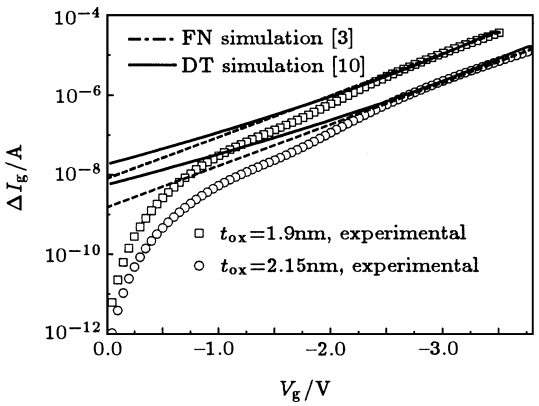


Fig.2. Comparison between the experimental and the simulated results based on FN and DT model, T=300K, t_{st}=4000s.

The positive charge-assisted tunnelling and the thermal-assisted tunnelling are based on the Fowler–Nordheim (FN) mechanism, which was applied to thicker oxide and higher V_g. As t_{ox} scaling down and V_g descending, I_g can be resulted from direct tunnelling (DT).[10] Figure 2 is the comparison between the experimental and the FN and DT simulated results, a large difference especially in lower voltage means neither the FN nor DT process is the dominating SILC mechanism to ultra-thin oxide.

Figure 3 shows that there is a linear relation between $\ln(J_{SILC}E_{ox})$ and $1/E_{ox}$ for both oxide thicknesses at 300K and 378K. This relation corresponds to the deep energy level TAT conduction mechanism.[10] Where the SILC density, $J_{SILC} = \Delta I_g/A_{ox}$, the oxide electric field E_{ox} is determined by V_{ox}/t_{ox}, and the oxide voltage V_{ox} is obtained by the self-consistent quantum mechanism method.

When a p-MOSFET is biased in inversion, it was found by carrier separation experiment that I_g is dominated by the gate valence band electron tunnelling for 1.7V< $|V_g|$ <5V, but by the inverted Si substrate hole tunnelling for $|V_g|$ <1.7V.[11] The $|V_g|$ range selected in this work is between 1.7V and $|V_{gstress}|$, so that the FN tunnelling can be neglected under this condition because the qV_{ox} is smaller than Si/SiO_2 interface barrier (3.15eV), and only the gate valence band electron tunnelling should be considered.

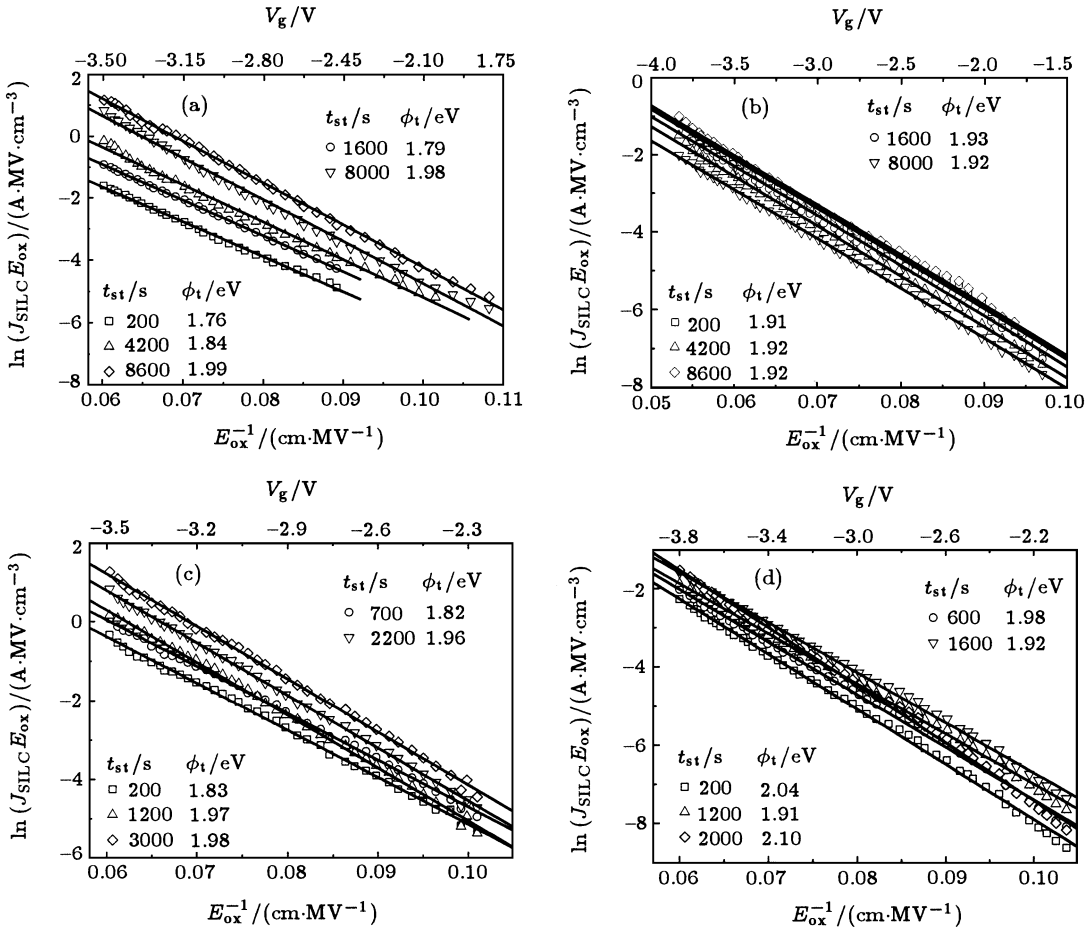


Fig.3. The relationship between $\ln(J_{\rm SILC}E_{\rm ox})$ and $1/E_{\rm ox}$, a deep energy level TAT conduction mechanism of SILC is supported. Different symbols correspond to different stress times and the trap energy levels are also shown in (a) $t_{\rm ox}$=1.9nm, T=300K, (b) $t_{\rm ox}$=2.15nm, T=300K, (c) $t_{\rm ox}$=1.9nm, T=378K and (d) $t_{\rm ox}$=2.15nm, T=378K.

The schematic energy band diagram of a p-MOSFET in inversion is shown in Fig.4 for TAT processes. At first the gate valence band electrons tunnel directly to oxide traps and then from the traps to oxide or anode conduction band when a higher negative $V_{\rm g}$ is applied. It is reasonable to say that TAT via single trap is the most possible process in thin oxides ($<6\sim$7nm), while for thicker ones (>8nm) multi-step tunnelling through several traps dominates the TAT process.[12] On the other hand, the electrons are confined to a narrow potential well at the interface, which leads to quantization of their energy normal to the interface. The current is dominated by tunnelling from the lowest sub-band at room temperature, and higher temperature promote the tunnelling with a little proportion, so the barriers had no evident change with temperature.

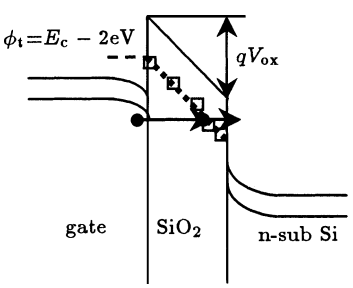


Fig.4. Schematic energy band diagram of the two-step TAT process for a p-MOSFET in inversion.

Using the Wentzel–Kramers–Brillouin (WKB) approximation to obtain tunnelling probability, we can write the total TAT current resulting from the single trap related A process as[13]:

$$J_{\rm tat}=\frac{2C_{\rm t}N_{\rm t}q\phi_{\rm t}\exp\left[\left(-D/E_{\rm ox}\right)\phi_{\rm t}^{3/2}\right]}{3E_{\rm ox}}, \qquad (1)$$

where

$$C_{\rm t} = \left(\frac{m_{\rm poly}}{m_{\rm ox}}\right)^{5/2} \left(\frac{8E_{\rm poly}^{3/2}}{3\hbar\left(\phi_{\rm t} - E_{\rm poly}\right)^{1/2}}\right)$$

and

$$D = 4\sqrt{2qm_{\rm ox}}/3\hbar,$$

$N_{\rm t}$ is the concentration of oxide traps, q the one electron charge and $\phi_{\rm t}$ the trap energy level. $m_{\rm poly} = 0.1m_{\rm e}$ and $m_{\rm ox} = 0.5m_{\rm e}$ are the electron effective mass in polysilicon and SiO_2 respectively.[14] $m_{\rm e}$ is the mass of a free electron, $E_{\rm poly}$ is the energy of an electron (taken as 0.2eV)[15] and $\hbar$ the Plank's constant. From Eq.(1), following equation is obtained[13]:

$$\ln\left(J_{\rm tat}E_{\rm ox}\right) = \left(-D\phi_{\rm t}^{3/2}\right)\left(1/E_{\rm ox}\right) + \ln\left(G\right), \qquad (2)$$

where $G = 2C_{\rm t}N_{\rm t}q\phi_{\rm t}/3$

Equation (2) gives a linear relationship between $\ln(J_{\rm tat}E_{\rm ox})$ and $1/E_{\rm ox}$, with a slope of $-D\phi_{\rm t}^{3/2}$ and D=48.3MV/cm for $m_{\rm ox} = 0.5m_{\rm e}$. So $\phi_{\rm t}$ can be calculated by (-slope/D)$^{2/3}$, and $N_{\rm t}$ could be given by $3G/2C_{\rm t}q\phi_{\rm t}$, where G is the intercept of Y axis.

From our experiment, the simulated $\phi_{\rm t}$ of 1.9nm oxide at different stress times is between 1.76 and 1.99eV (Fig.3(a)), with an average value of 1.872eV, and for 2.15nm oxide, $\phi_{\rm t}$ is between 1.91 and 1.93eV (Fig.3(b)), with an average value of 1.92eV at 300K. While the average $\phi_{\rm t}$ of two thicknesses are 1.912 (Fig.3(c)) and 1.99eV (Fig.3(d)) at 378K respectively. The experimental data which we chose above is arbitrary, so the $\phi_{\rm t}$ results should have universalities to our samples. It is found that our $\phi_{\rm t}$ is close to the former results, such as $\phi_{\rm t}$=2.2eV in Ref.[13], $\phi_{\rm t}$=2.1eV in Ref.[14], $\phi_{\rm t}$=2.46–2.56eV in Ref.[16] and $\phi_{\rm t}$=2.62eV in Ref.[17]. However, the 2.62eV of Ref.[17] was extracted from the $J_{\rm SILC} - E_{\rm ox}$ curves. It is also of most importance that the above $\phi_{\rm t}$ agrees with the trap energy levels in SiO_2 found by some researchers.[18,19]

Xu *et al*[18] reported that the defects in SiO_2 induced by high field stresses are oxygen-related defects which are similar to the oxygen donors in silicon. Using a helium-like model, we calculated the $\phi_{\rm t}$ related to oxygen donor states in SiO_2 at $E_{\rm c}$−2.0eV and $E_{\rm c}$−0.925eV,[18] where $E_{\rm c}$ is the bottom of oxide conduction band. Furthermore, early work[19] also showed that the stress induced defect state in SiO_2 had an activation energy of 2.0eV in average.

For the gate valence band electrons, the barrier for the first tunnelling is 4.27-$\phi_{\rm t}$eV, 4.27eV equals to the Si/SiO_2 interface barrier (3.15eV) adds the band gap of Si (1.12eV). So the barriers for tunnelling to the above two kinds of oxide traps ($E_{\rm c}$-2.00eV and $E_{\rm c}$-0.925eV) are 2.27 and 3.345eV respectively. And the deeper energy level traps are in favor of the first tunnelling for the gate valence band electrons. So the deep energy level TAT processes dominate the SILC of inversion p-MOSFET, which agrees with our simulation results

The $N_{\rm t}$ simulated from Fig.3 is changing with $t_{\rm st}$ and $E_{\rm ox}$. At 300K, $N_{\rm t}$ changes from 1.65×10^{14} to $1.1\times10^{16}/{\rm cm}^3$ for the 1.9nm oxide, and from 1.09×10^{14} to $2.95\times10^{14}/{\rm cm}^3$ for the 2.15nm sample at the selected times. At 398K, the $N_{\rm t}$ ranges are from 6×10^{14} to $1.3\times10^{15}/{\rm cm}^3$ for the 1.9nm oxide and from 2.3×10^{14} to $6.5\times10^{14}/{\rm cm}^3$ for the 2.15nm oxide at the selected times. It is found that the $N_{\rm t}$ increases with both $t_{\rm st}$ and $E_{\rm ox}$.

Figure 5(a)–5(d) compare the simulated results with the experimental data at 300K and 378K. The insets show that the simulated trap density, $N_{\rm t}$ increases not only with $t_{\rm st}$ at the same $E_{\rm ox}$, but also with $E_{\rm ox}$ at a given $t_{\rm st}$. The insets also show that the simulated trap energy, $\phi_{\rm t}$ changes little with stress time. The good agreement between simulation and experimental results strongly supports that the oxide oxygen-related donor-like defects correlative TAT is the conduction mechanism of SILC over a gate voltage range between 1.7V and stress voltage in ultrathin gate oxide under CVS.

As SILC has large influence on the long-term reliability of MOS devices, MOS integrated circuit and flash memory, much efforts have been made to reduce it. An effective method is to use higher dielectric constant materials such as HfO_2 as gate oxide, and the high κ dielectric devices with good isolation and transistor performance have demonstrated.

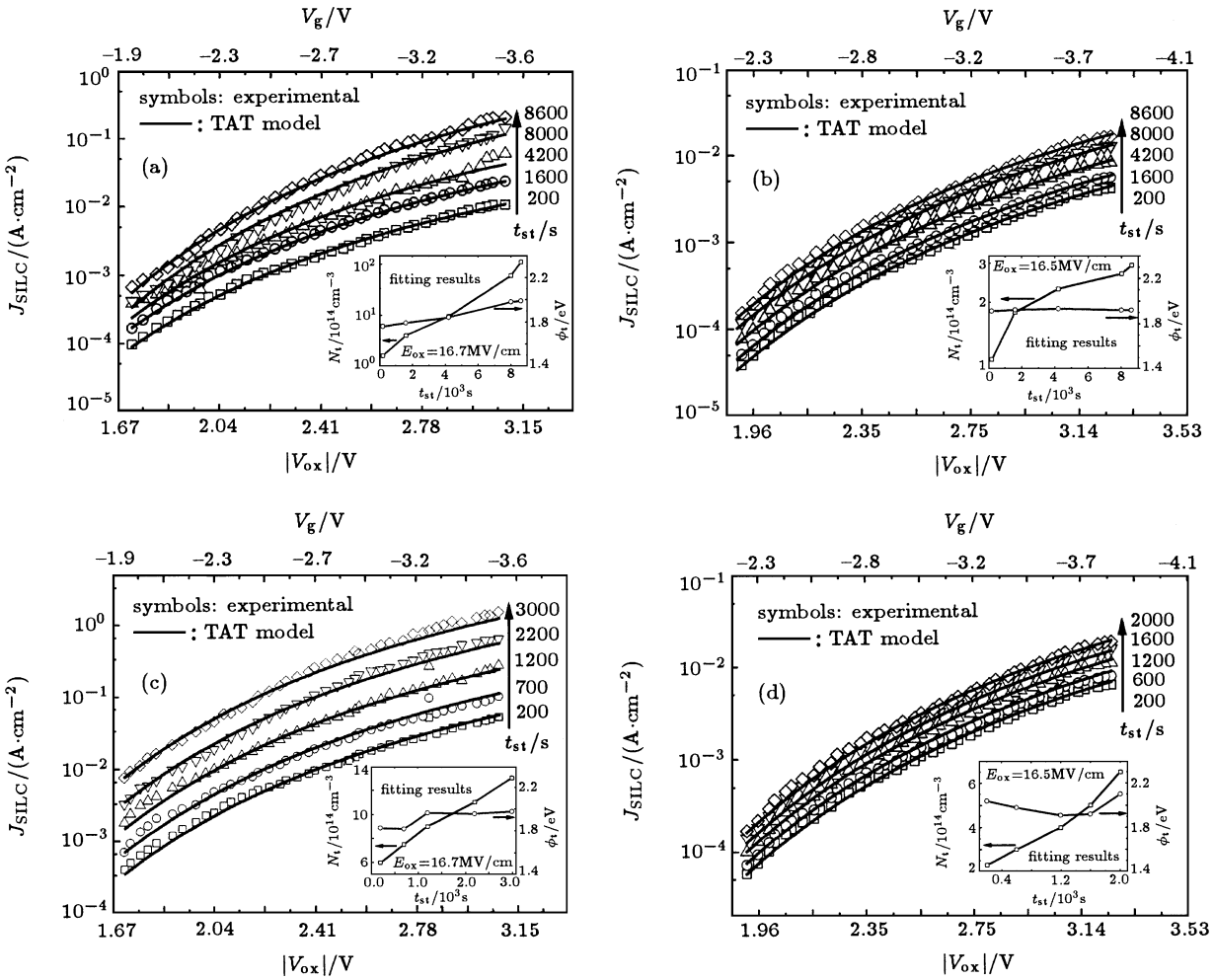


Fig.5. Comparison between the experimental and the simulated results based on Eq.(1) for (a) t_{ox}=1.9nm, T=300K, (b) t_{ox}=2.15nm, T=300K, (c) t_{ox}=1.9nm, T=378K and (d) t_{ox}=2.15nm, T=378K. Different symbols correspond to different stress times. The insets show N_t and ϕ_t change with the stress time and oxide electric field.

4. Conclusions

The SILC of 2nm gate oxide over a definite gate voltage range (1.7V< $|V_g|$ < 3.8V) follows the TAT model. The TAT processes are dominated by oxide traps which have energy level of 1.9eV and the interface traps do not play an important role. The traps are believed to be the oxygen-related donor-like defects induced by high field stresses in 2nm gate oxide, and its densities increase with both the stress time and oxide electric field.

Acknowledgment

The authors would like to thank Motorola Corporation for supplying the test samples.

References

[1] Lin Y H, Lee C L and Lei T F 1998 *IEEE Trans. Electron Devices* **45** 567

[2] Liu H X and Hao Y 2001 *Acta Phys. Sin.* **50** 1773 (in Chinese)

[3] Maserjian J and Zamani N 1982 *J. Appl. Phys.* **53** 559

[4] Olivo P, Nguyen T N and Ricco B 1988 *IEEE Trans. Electron Devices* **35** 2259

[5] Chou A I, Lai K F, Kumar K *et al* 1997 *Appl. Phys. Lett.*

70 3407
[6] DiMaria D J and Cartier E 1995 *J. Appl. Phys.* **78** 3883
[7] Stathis H and Toriumi A 1995 *Appl. Phys. Lett.* **67** 3489
[8] Kimura M and Ohmi T 1996 *J. Appl. Phys.* **80** 6360
[9] Lime F, Ghibaudo G and Guegan G 2001 *Microelectron. Reliab.* **41** 1421
[10] Yang B L, Lai P T and Wong H 2004 *Microelectron. Reliab.* **44** 709
[11] Shi Y, Ma T P, Prasad S *et al* 1998 *IEEE Trans. Electron Devices* **45** 2355
[12] Ghibaudo G, Riess P, Bruyere S *et al* 1999 *Microelectron. Eng.* **49** 41
[13] Fleischer S, Lai P T and Cheng Y C 1993 *J. Appl. Phys.* **73** 3348
[14] Fleischer S, Lai P T and Cheng Y C 1992 *J. Appl. Phys.* **72** 5711
[15] Lundstrom I and Svensson C 1972 *J. Appl. Phys.* **43** 5045
[16] Cheng X R, Cheng Y C and Liu B Y 1988 *J. Appl. Phys.* **63** 797
[17] Houng M P, Wang Y H and Chang W J 1999 *J. Appl. Phys.* **86** 1488
[18] Xu M Z, Tan C H and Mao L F 2001 *Solid State Commun.* **117** 365
[19] DiMaria D J and Stasiak J W 1989 *J. Appl. Phys.* **65** 2342