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Hot-carrier degradation characteristics and explanation in 0.25 μm PMOSFETs*

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The hot-carrier effect (HCE) of deep-submicron PMOSFETs has been investigated. It is found that the HCE includes both generation of interface states and formation of positive fixed charges in the gate oxide. We present experimental evidences showing that two degradation mechanisms are important in the case of deep-submicron PMOSFETs. Firstly, the generation of positive fixed oxide charges is significant in the case of deep-submicron PMOSFETs, which degrades the threshold voltage and even limits the transistor lifetime. For advanced analogy and mixed signal applications, process and device reliability limits need to be set up based also on threshold voltage shift, in addition to traditional methods of the transconductance degradation or gate oxide lifetime. Secondly, the generation of interface states by holes influences the device characteristics. Some speculation on the HCE formation process is included.

Keywords: PMOSFET, hot-carrier effect (HCE), positive fixed oxide charges, interface states, device reliability

PACC: 7340Q, 7300, 7220J

1. Introduction

Recently, MOSFET feature size has been rapidly scaled down in order to improve the circuit performance. As scaling of device advances, control of reliability of deep-submicron PMOSFETs becomes critical. As reported recently,[1−6] the hot-carrier effect has become a major concern when realizing highly reliable integrated CMOS devices.

Many recent publications on submicron PMOSFET hot-carrier degradation interpret the degradation in terms of negative oxide charge with a logarithmic time dependence.[7−10] Electrons are generated by avalanche in the pinch-off region and may be injected into the gate oxide near the drain. These electrons generate negative oxide charges that reduce the effective channel length. This mechanism is called hot-electron-induced punch (HEIP). It is similar in surface-channel and buried-channel transistors.[11,12] At low drain voltage, we may describe the shorter channel as an extended drain. The threshold voltage is shifted accordingly and the drain extension causes a higher drain resistance.

For deep-submicron (0.25μm) PMOSFETs, the situation is very different. In this paper, we show that the cooperation of positive oxide charges and interface states plays a part. Injection of holes into the oxide generates positive oxide charges. This mechanism is most significant for deep-submicron PMOSFETs with a nitrided gate oxide. The generation of interface states by holes reduces the transconductance with a logarithmic time dependence. The time dependence of deep-submicron PMOSFET degradation has been successfully described as a combination of the two effects.

2. Experiment

Test devices used in this work were fabricated using 0.25μm gate CMOS processing technology. Gate oxide was performed in a two-step oxidation pro-

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cedure. NO gas annealing followed by gate oxidation was performed for the samples with T_{ox}=5nm. The channel length and width of devices used in this work are 0.25μm and 5μm, respectively. All data given in this paper are for these devices. The hot-carrier (HC) stress was applied with source and substrate electrodes grounded as shown in Fig.1. Devices were stressed at HC stress conditions of V_g=–4.25V, V_d=–1.0V, V_s=V_{sub}=0V, stress time t=30000s. The threshold voltage (V_{th}), the maximum transconductance (G_{mmax}), the drain current in the linear region (I_{dlin}) and saturated region (I_{dsat}) were measured at a predetermined period as key device parameters.

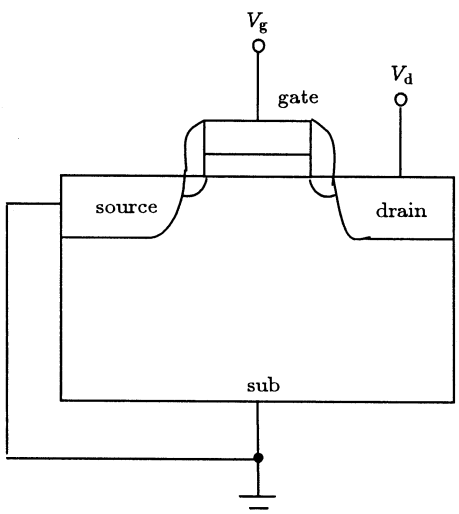


Fig.1. Experimental arrangement for HC stress conducted in this work.

3. Results and discussions

The degradation of PMOSFETs is observed from the shift of transfer characteristic, as shown in Fig.2. The measurement started from recording the initial transfer characteristic of a PMOSFET at V_d=–50mV. A direct current (DC) bias was applied to the gate and drain with the source and substrate grounded. After a prefixed time (30000s), the transfer characteristic was measured again at V_d=–50mV to determine the degradation induced by HC effect. Negative threshold voltage shift, degradation in the subthreshold slope, and increase in the off current (I_{off}) are observed for PMOSFETs after HC stress, suggesting the creation of positive fixed oxide charges and interface states.

Figure 3 shows the dependence of transconductance on the gate voltage at V_d=–50mV before and after 30000s stress. Very large transconductance degradation (interface states generation) is observed.

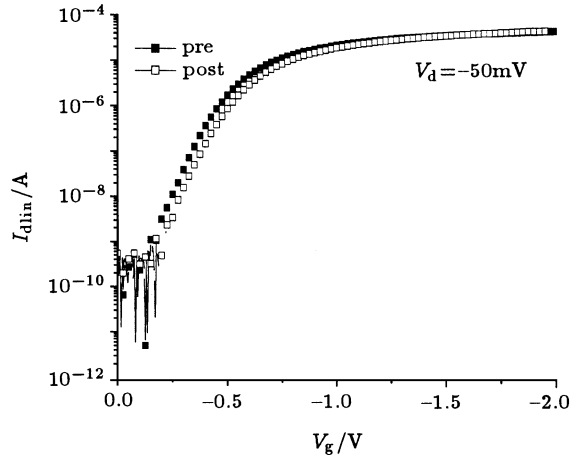


Fig.2. I_{dlin} degradation induced by HC stress.

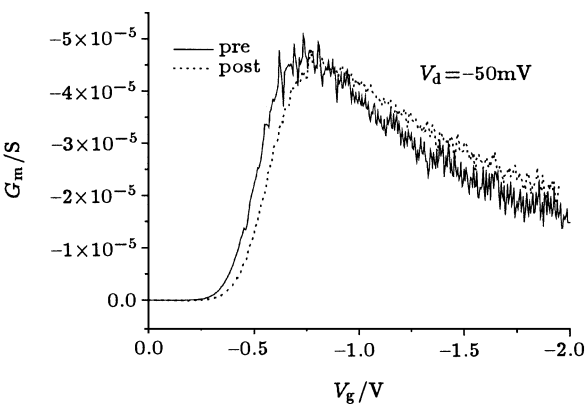


Fig.3. G_m degradation induced by HC stress.

The typical I_{dsat}–V_g characteristics for PMOSFETs at V_d=–1V before and after 30000 s stress are shown in Fig.4. In the I_{dsat}–V_g measurement, I_{dsat} decreases significantly, whereas only a little change is observed in I_{dlin}–V_g measurement.

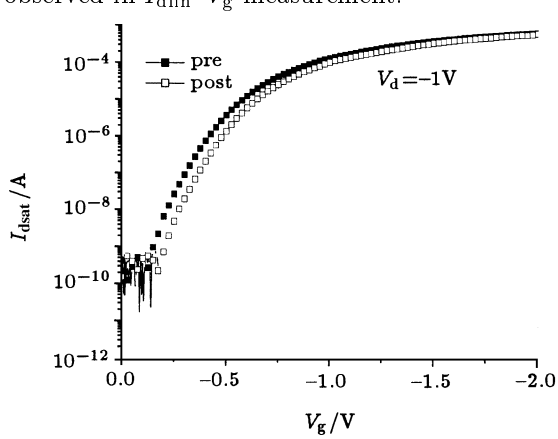


Fig.4. I_{dsat} degradation induced by HC stress.

The typical I_{sub}–V_g characteristics for PMOSFETs before and after 30000 s stress is shown in Fig.5. After HC stress, the peak substrate current ($I_{sub,max}$) shifts to more negative V_g direction due to an increase in the threshold voltage and $I_{sub,max}$ decreases due to the reduction of drain current because the impact ionization rate (I_{sub}/I_d) is almost the same before and after stress.

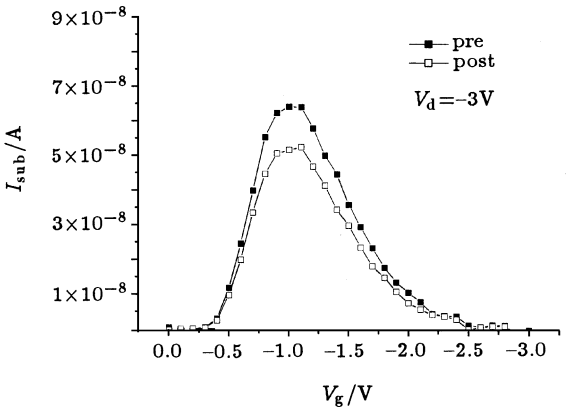


Fig.5. I_{sub} degradation induced by HC stress.

The gate current degradation induced by HC stress after 30000 s is shown in Fig.6. The maximum gate current increases after HC stress, implying that maybe neutral oxide traps are formed during stress and contribute to trap assisted hole tunnelling (TAHT) current from the substrate and electron tunnelling from the conduction band of the gate. I_g increases monotonically with increasing V_g at low V_d. However, for the high V_d, the dependence of I_g on V_g changes greatly. In the first stage, I_g increases with increasing V_g, whereas in the second stage, I_g decreases with increasing V_g. Initially, the higher gate electrical field enhances the injection of hot holes, which corresponds to higher I_g. When $|V_g|>2$V, the vertical electrical field decreases with increasing V_g at the drain edge. Therefore, I_g decreases gradually. Moreover, in the medium gate voltage region, $V_g \approx V_d/2$, PMOSFETs work in the saturated region, and the horizontal electrical field in the channel is maximal, which corresponds to the maximum impact ionization rate and leads to much more hot holes. It also contributes to the maximum I_g.

Figure 7 shows the dependence of G_{mmax}, I_{dsat} and I_{dlin} on the stress time, respectively. These device parameter shifts have logarithmic time-dependence.

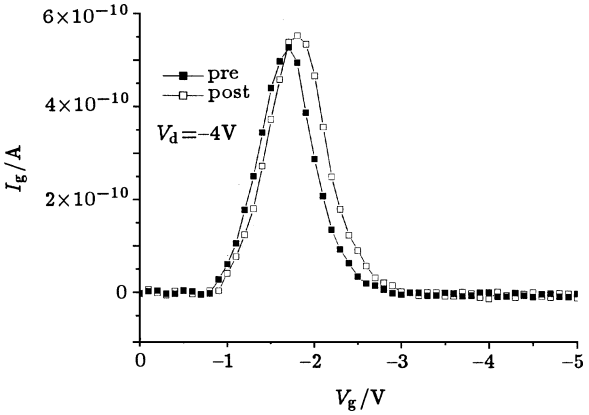


Fig.6. I_g degradation induced by HC stress.

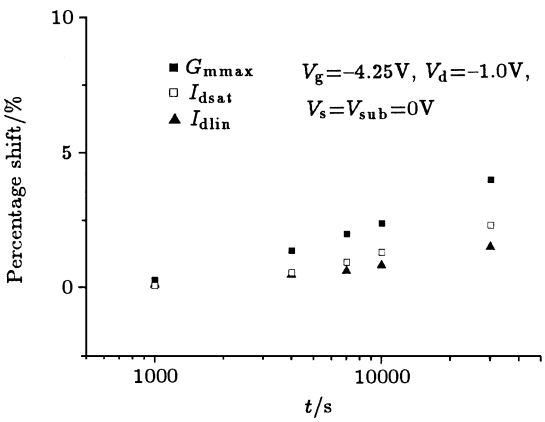


Fig.7. Degradation of device parameters induced by HC stress versus stress time.

Figure 8 shows the plot of delta V_{th} versus the stress time for V_g=–4.25V, V_d=–1.0V and V_s=V_{sub}=0V. The threshold voltage shifts to a more negative direction. The threshold voltage increases with the stress time and can be approximated by a power law relationship, shown in Eq.(1). The time evolution coefficient n is 0.56, the constant C is 1.01×10^{-4}.

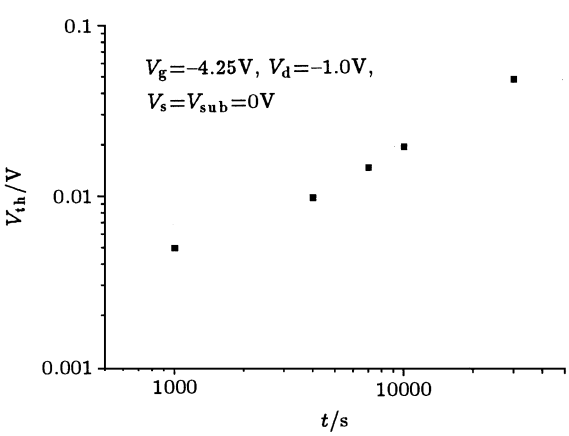


Fig.8. V_{th} shift induced by HC stress versus stress time.

$$\Delta V_{\rm th} = Ct^n. \quad (1)$$

Comparison of degradation of different device parameters induced by HC stress is shown in Table 1. Under HC stress conditions, percent degradation in $V_{\rm th}$ is much higher than $G_{\rm mmax}$, $I_{\rm dsat}$ and $I_{\rm dlin}$. These devices meet conventional HC lifetime specifications of both $G_{\rm mmax}$ and $I_{\rm dsat}$ degradation by wide margin. However, higher amount of $V_{\rm th}$ shift causes concern in several mixed-signal applications. Process and device reliability limits need to be set up based on $V_{\rm th}$ shift specification also. Degradation from HC stress can be minimized by further drain engineering optimization. Moreover, nitridation enhances the generation of positive charges by several orders of magnitude.[13] Increase in nitrogen concentration causes increase in trapped charges in the oxide during stress and thereby increase in $V_{\rm th}$ shift. Nitrogen is required in these technologies to reduce the boron penetration in low voltage PMOSFETs. Therefore, the $V_{\rm th}$ shift poses significant reliability challenges in mixed signal applications.

Table 1. Device parameters degradation induced by HC stress.

Device parameters	Degradation/%
$\Delta G_{\rm mmax}/G_{\rm mmax0}$	–4.08
$\Delta I_{\rm dsat}/I_{\rm dsat0}$	–2.40
$\Delta I_{\rm dlin}/I_{\rm dlin0}$	–1.59
$\Delta V_{\rm th}$	–9.80

Here, we propose a model to explain the HC degradation characteristics and time dependence of the negative voltage shift in deep submicron PMOSFETs, as depicted in Fig.9.

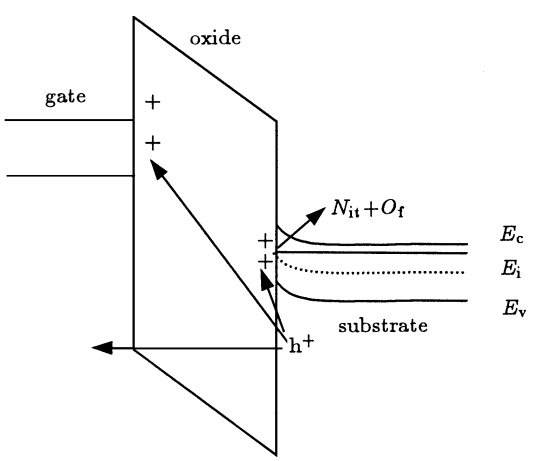


Fig.9. Schematic diagram for the generation of the interface states and positive fixed oxide charges.

The interface state $N_{\rm it}$, trivalent silicon dangling bonds $Si_3 \equiv Si^*$ and fixed oxide charges $O_3 \equiv Si^+$ are generated by the impact of hot holes on the hydrogen-terminated Si bonds and contribute to the negative threshold voltage shift.[14] The electrochemical reaction are expressed as follows:

$$(Si_3 \equiv Si - H) + h^+ \Leftrightarrow (Si_3 \equiv Si^*) + H_i^+, \quad (2)$$

$$(O_3 \equiv Si - H) + h^+ \Leftrightarrow (O_3 \equiv Si^+) + H_i, \quad (3)$$

$$(H_i, H_i^+)_{\rm interface} \Leftrightarrow (H_i, H_i^+)_{\rm bulk}. \quad (4)$$

Here, hydrogen atoms and ions are believed to be the by-products of the electrochemical reaction.

The whole process can be explained as follows. Holes are activated thermally and gain enough energy to dissociate the interface defects by the vertical electrical field near the lightly doped drain (LDD) regions because of higher hole concentration near the edge.[14,15] The interface states and positive fixed oxide charges are generated by the impact of hot holes on the hydrogen-terminated Si bonds and contribute to the negative $V_{\rm th}$ and $G_{\rm mmax}$ shift. $V_{\rm th}$ shift is very sensitive to the generation of positive oxide charges, the generation of interface states causes mobility degradation and therefor $G_{\rm mmax}$ reduction. The generation of positive oxide charges makes the gate electric field decreased. In order to generate the same amount of hot holes in the channel, a higher negative gate voltage must be applied to the gate. So, the $V_{\rm th}$ shifts towards the negative direction.

In order to confirm the roles of interface states and positive fixed oxide charges, we apply opposite stress at high temperature to have PMOSFETs annealed. $V_{\rm g}$=4.25V, t=7000s. $V_{\rm th}$ recovery and $G_{\rm mmax}$ recovery is 14% and 3%, respectively. Compared with $G_{\rm mmax}$ recovery, $V_{\rm th}$ recovery is much higher under the annealing conditions, indicating higher amount of detrapping. This indicates that the majority of the traps contributing to $G_{\rm mmax}$ shift are interface traps that cannot be annealed, whereas the positive fixed oxide charges contributed to $V_{\rm th}$ shift can be annealed. Therefore, the positive fixed charges is believed to be responsible for $V_{\rm th}$ shift. $V_{\rm th}$ shift increases more rapidly than $G_{\rm mmax}$ shift (corresponding to interface states generation), the generated oxide fixed charges should be much more than the interface states.

4. Conclusion

A combination of two degradation mechanisms determines the time dependence of hot-carrier degradation in PMOSFETs. For 0.25μm PMOSFETs, the generation of interface states and positive oxide

charges by hot holes causes the degradation. The generation of positive oxide charges is shown to determine the threshold shift, which limits lifetime of deep-submicron PMOSFETs. Generation of positive oxide charges is important with respect to the reliability of deep-submicron PMOSFETs with a nitrided gate oxide.

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