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I–V–T studies on Ni-silicide/n-Si(100) contacts formed by Ti–Ni–Si solid state reaction*

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The current–voltage (I–V) characteristics of Ni silicide/n-Si(100) contacts, which were formed from solid-state reaction of Ni–Si with a thin Ti capping layer at different annealing temperatures, were measured at temperatures ranging from 80K to room temperature. The low temperature I–V curves exhibit an excess current at the low bias region which is significantly larger than that predicted by the traditional thermionic emission (TE) model. A double-Schottky barrier height (SBH) model simplified from Tung's pinch-off model is used to analyse the measured I–V curves, from which the extent of the SBH inhomogeneity can be extracted. Higher annealing temperature results in larger SBH inhomogeneity, implying the degradation of the silicide film uniformity. The thin Ti capping layer increases slightly both the NiSi phase transfer temperature and the thermal stability of the formed NiSi film.

Keywords: Schottky barrier, metal-semiconductor contact, current-voltage characteristics
PACC: 7340E, 8130B, 8115N

1. Introduction

Self-aligned silicide (salicide) is one of key issues in modern VLSI technologies.[1] Recently, Ni monosilicide (NiSi) has received much attention for the sub-0.25μm technology generations because of its low resistivity, low growth temperature, small stress and less silicon consumption as compared to the commonly used silicides: $TiSi_2$ and $CoSi_2$.[2–4] The reaction of Ni–Si system, as well as the Ni silicide/Si characteristics, has been quite extensively studied in the past.[5–7] It is well known that during the annealing of the Ni–Si system, Ni diffuses into Si to form silicide, first Ni_2Si is formed at about 200–300°C, then NiSi at about 400–600°C, and then $NiSi_2$ at temperature higher than about 700°C. Because $NiSi_2$ is a high-resistivity phase, it should be avoided during the device fabrication. Therefore, the thermal stability is a key concern in the implementation of NiSi. Adding alloying elements, such as Co,[8] Pt[9,10] or Pd,[11] have been investigated to suppress the $NiSi_2$ phase formation.

The Ni–Si phase transformation and the silicide characteristics are usually studied using material characterization techniques such as transmission electron microscopy, x-ray diffraction, Auger electron spectroscopy, Rutherford backscattering spectroscopy and four-point sheet resistance measurement, etc. However, these techniques need relatively large detecting area and provide averaged signals which are proportional to the volume or area percentage of certain phases or atoms, so that some very small defects at or near the silicide/Si interface, which may have strong influence on the salicide device characteristics and are important for device scaling, are difficult to detect. We have pointed out in our previous papers that a Schottky diode is a sensitive device to detect the defects or other imperfections at or near the silicide/Si interface.[8,12–14] In this paper, the Schottky barrier height (SBH) characteristics of Ni-silicides/n-Si(100) contacts, which are formed by Ti–Ni–Si solid-state reaction at various annealing temperatures, are studied using the temperature-dependent current–voltage (I–V–T) measurement.

2. Experimental

The starting materials were n-type (100) Si wafers

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with a resistivity of 5–8 Ω·cm. Square windows with different areas were defined using the standard processes of thermal oxidation, photolithography and wet etching, etc. A p^+ guard-ring around the active area was formed by boron diffusion and an n^+ layer at the back was formed by phosphorous diffusion. Immediately after a standard RCA cleaning and a short dipping in a diluted HF solution, the patterned wafers were loaded into a vacuum chamber with a base pressure of about 7×10^{-5}Pa. 15 nm Ni and 5 nm Ti were deposited by electron-beam evaporation sequentially without opening the chamber. Ni silicidation was performed in an AST rapid thermal annealing system. The samples were isochronously annealed in an N_2 atmosphere for 1 min at temperatures of 550, 650 and 750°C, respectively. After silicidation, the unreacted metal was selectively etched.[15] A 100nm Ti layer was deposited on the back of samples to provide an ohmic contact. I–V measurements were carried out by a computer controlled system with a Keithley 617 electrometer, HP3478A multimeter and a cryostat which controls the sample temperature from liquid N_2 to room temperature within ±3°C deviation.

3. Results and discussion

Figure 1 shows typical I–V curves measured at different temperatures. According to the traditional thermionic emission (TE) model, the current of an ideal Schottky diode under a forward bias V is expressed by the following equation at $V > 3kT/q$:[16]

$$I = A \cdot A^{**} \cdot T^2 \cdot \exp\left(-\frac{\Phi}{k \cdot T}\right) \cdot \exp\left(\frac{q(V - I \cdot R_s)}{n \cdot k \cdot T}\right), \quad (1)$$

where A is the diode active area, A^{**} is the effective Richardson constant (about 117A/cm^{2}K^2 for n-Si), T is the temperature in Kelvin, k is the Boltzmann constant, q is the electronic charge, n is the ideality factor, R_s is the series resistance of the diode and Φ is the barrier height in eV. Eq. 1 is utilized to fit the experimental I–V data with adjustable Φ, n and R_s as fitting parameters. The higher than about 180K I–V curves and the large bias region of the low temperature I–V curves can be fitted by Eq.(1) quite well. Both Φ and n are temperature dependent, which can be attributed to the SBH inhomogeneity.[15,17] Assuming a Gaussian distribution of SBH, the I–V characteristic can still be expressed by Eq.(1) while the Φ is replaced by an apparent barrier height, Φ_{ap}, expressed as[17]

$$\Phi_{ap} = \overline{\Phi} - \frac{\sigma^2}{2kT}, \quad (2)$$

where $\overline{\Phi}$ and σ are the mean value and the standard deviation of the Gaussian function. Obviously, σ is an indicator of the SBH inhomogeneity.

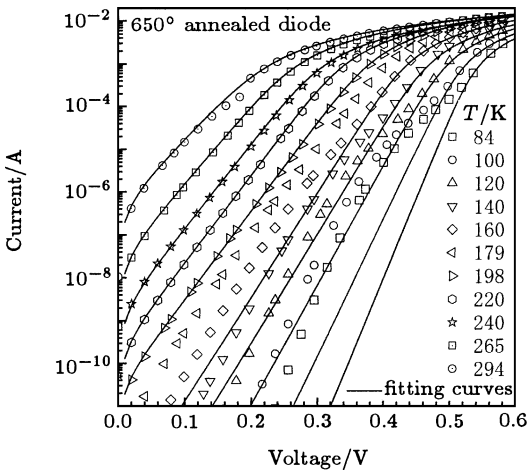


Fig.1. Forward I–V–T characteristics of NiSi/n-Si(100) diode formed by 650°C annealing of a Ti–Ni–Si system, the solid lines are calculated using a traditional TE model.

Figure 2 shows the Φ_{ap}-$1/T$ relationship of the diodes formed at different annealing temperatures. From the linear fitting of the experimental data, the standard deviation of the SBH distribution is extracted to be 71.8, 68.9 and 72.0 meV for the samples annealed at 550, 650 and 750°C, respectively. This indicates that the 650°C annealed sample has smallest SBH inhomogeneity, implying its superior silicide uniformity as compared with other two samples. However, the linearity of the Φ_{ap}-$1/T$ relationship is not

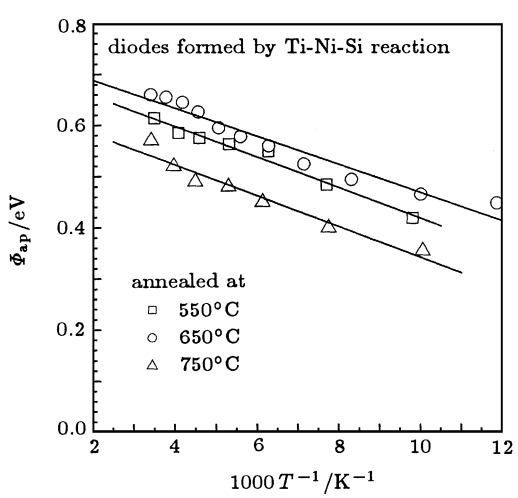


Fig.2. Relationship between the apparent barrier height (Φ_{ap}) deduced from the TE model and the reciprocal measurement temperature ($1/T$) for diodes annealed at 550, 650 and 750°C, the solid lines are the linear fitting of the experimental data, from which the standard deviation (σ) of the SBH distribution is determined.

good. A more complicated SBH distribution function, such as double-Gaussian[18] or Gaussian and lognormal,[19] has been proposed to explain the deviation; however, this method is somewhat arbitrary and lacks physical meaning. Another reason for the deviation is the bias voltage dependence of the effective barrier height.[20]

Furthermore, Fig.1 shows that the measured current of the low temperature I–V curves significantly exceeds that predicted by the TE model in the low bias region. The excess current cannot be ascribed to the carrier recombination in the space charge region, the tunnelling current through the SBH and the sidewall leakage because of the absence of a frequency-dependence of capacitance (not shown here), the low doping level of Si substrate and the p^+ guard-ring structure, respectively, while it has been attributed to the embedded low SBH patches in the silicide/Si contact.[13,14,21] According to Tung's pinch-off model, the current through a circular patch with low barrier height can be expressed as:[21]

$$I_{\rm patch} = A^{**}T^2 \left[\frac{4\pi kT\gamma\eta^{2/3}}{9[\Phi^0 - V_n - (V - IR_{\rm sr})]^{2/3}}\right] \times \exp\left[-\frac{\Phi^0}{kT} + \frac{\gamma[\Phi^0 - V_n - (V - IR_{\rm sr})]^{1/3}}{kT\eta^{1/3}}\right] \quad (3)$$

with $V_n = (kT/q)\ln(N_{\rm C}/N_{\rm D})$, $\eta = \varepsilon_{\rm Si}\varepsilon_0/(qN_{\rm D})$, patch parameter $\gamma = 3\left(\Delta R_0^2/4\right)^{1/3}$ and local series resistance $R_{\rm sr} = \rho_{\rm s}/(4\pi R_0)$, where Φ^0 is the overall SBH except the patch, $N_{\rm C}$ is the effective density of states in the Si conduction band, $\varepsilon_{\rm Si}\varepsilon_0$ is the Si permittivity, R_0 is the patch radius, Δ is the barrier height reduction of the patch and $\rho_{\rm s}$ the local resistivity through the patch. Then the total current can be expressed as[21]

$$I_{\rm total} = I_1 + \sum_i C_i I_{\rm patch}(\gamma_i, R_{{\rm sr}-i}), \quad (4)$$

where I_1 is the current through the whole contact as described by Eq.(1). C_i is the number of patches with a parameter of γ_i. Parameters γ_i, C_i and its local series resistance $R_{{\rm sr}-i}$ are unknown and should be used as fitting parameters. However, the fitting is difficult and is also somewhat arbitrary if many different γ_i patches need to be considered.[14,22] We noticed that Eq.(3) is still somehow similar to Eq.(1) apparently, thus the summary contribution of all patches, i.e. the second item of Eq.(4)'s right-hand side, can be expressed as Eq.(1) formally with new meanings for three fitting parameters Φ, n and $R_{\rm s}$. The contact seems to contain two diodes with different $\Phi_{\rm ap}$, n and $R_{\rm s}$:

$$\begin{aligned} I_{\rm total} =& I_1 + I_2 \\ =& A \cdot A^{**} \cdot T^2 \cdot \left[\exp\left(-\frac{\Phi_1}{k \cdot T}\right) \times \exp\left(\frac{q(V - I_1 \cdot R_1)}{n_1 \cdot k \cdot T}\right) + \exp\left(-\frac{\Phi_2}{k \cdot T}\right) \cdot \exp\left(\frac{q(V - I_2 \cdot R_2)}{n_2 \cdot k \cdot T}\right)\right]. \end{aligned} \quad (5)$$

Such a simple double-barrier-height model is used to fit the experimental I–V data. Figure 3 shows an example of the fitting result for the 100K I–V curve of the 650°C annealed diode. The fitting curve matches the experimental data very well. The fitting parameters are Φ_1=0.465eV, n_1=1.57, R_1=13Ω and Φ_2=0.418 eV, $n_2 = 1.60$, R_2=1500Ω, respectively. Notice that R_2 is much larger than R_1 due to the pinch-off effect at the low SBH patches.[21] Figure 4 shows the fitting results of all temperature I–V curves for the 650°C annealed diode, they all can be fitted by Eq.(5) quite well. Here R_1 and R_2 keep the same value at all temperatures, while Φ and n (both 1 and 2) are temperature-dependent. With the measurement temperature decreasing, Φ (both 1 and 2) decreases and n increases.

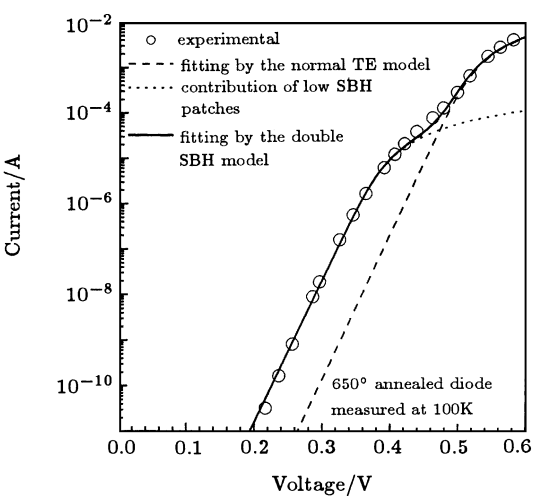


Fig.3. 100K forward I–V curve of 650°C annealed diode and its fitting curves based on the double-SBH model.

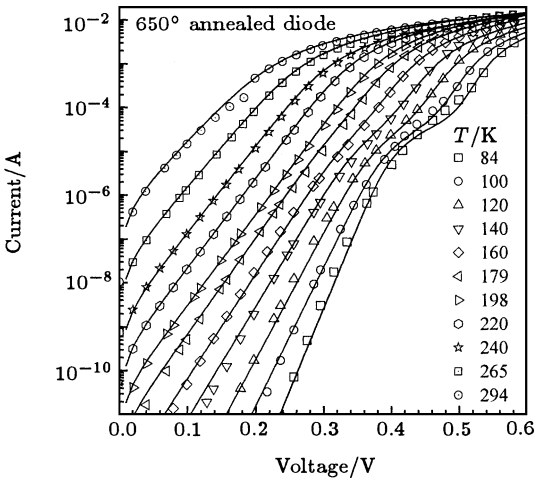


Fig.4. Forward I–V–T characteristics of the 650°C annealed diode and the fitting curves based on the double-SBH model.

The physical meaning of this model can be understood as follows. It is reasonable to assume that the contact contains numerous patches with different γ, $R_{\rm sr}$ and C, and the patches with larger γ usually have larger $R_{\rm sr}$ and smaller C_i. It has been pointed out that the contribution of numerous patches with similar $R_{\rm sr}$ can be described as a Gaussian distribution of the barrier height.[12−14] As a rough approximation, all patches can be divided into two parts, one part includes patches with small $R_{\rm sr}$, similar to the global resistance $R_{\rm s}$. The contribution of these patches and the current through the whole smooth contact area can be represented by I_1 in Eq.(5). The other part includes patches with large $R_{\rm sr}$, which usually have large patch parameter γ and much lower barrier height. Currents through these patches are represented by I_2 in Eq.(5). In the low current region, i.e., in the low bias region of the low temperature I–V curves, I_2 dominates because it has low apparent barrier height (Φ_2). However, with increasing of the current, I_2 decreases dramatically due to the series resistance effect, and I_1 may dominate because R_1 is much smaller than R_2. This results in a "kink" phenomenon in the low temperature I–V curves around 10^{-4}–10^{-6} A, as observed in Fig.1. Therefore, Φ_2 and R_2 can also be used as indicators of the barrier height inhomogeneity along with the above mentioned σ. Larger R_2 and lower Φ_2 means larger γ low SBH patches, and indicates larger SBH inhomogeneity.

Figure 5 shows the fitting results of the 100K I–V curves of diodes annealed at 550, 650 and 750°C. The local resistances (R_2) are 10^4, 1500 and 6×10^5 Ω, and the low SBH (Φ_2) are 0.383, 0.418 and 0.315 eV, respectively. The 650°C annealed diode shows smallest R_2 and largest Φ_2, indicating better SBH homogeneity than other two samples, in agreement with the above σ result.

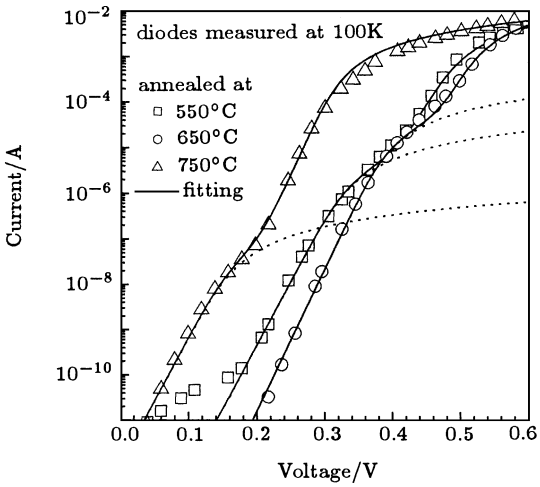


Fig.5. 100K forward I–V characteristics of diodes annealed at 550, 650 and 750°C, the dotted lines are the contribution of the low SBH patches (I_2), the solid lines are the total current fitted by the double-SBH model.

Now we discuss the silicide phase formation during the solid-state reaction of the Ti–Ni–Si system according to the above I–V–T results. The barrier heights deduced from I–V curves near room temperature, which is the normal-meaning SBH not including the low SBH patches' effect, are 0.61 and 0.67eV for the 550 and 650°C annealed samples, respectively. It is known that the Ni_2Si/Si contact has barrier height of about 0.62eV while that of NiSi/Si is about 0.67eV,[14] it indicates that the silicide formed is Ni_2Si at 550°C, and it has transferred to NiSi at 650°C. For the Ni–Si reaction without the Ti capping layer, the transfer temperature is about 400°C.[7,14] Therefore it can be concluded that the Ti capping layer hinders the NiSi phase formation. On the other hand, the NiSi silicide film-quality becomes worse with increasing annealing temperature, probably due to the formation of silicide spikes or embedded $NiSi_2$ grains, which act as low SBH patches.[8,14,23] In the Ti–Ni–Si case, 750°C annealed sample contains patches with $\Phi_2 = 0.315$eV and $R_2=6\times10^5\Omega$. In the Ni–Si case, as reported in Ref.[14], a similar extent of SBH inhomogeneity appears in the 650°C annealed sample. This indicates that the thermal stability of NiSi is slightly improved by the Ti capping layer.

4. Conclusion

Ni-Silicide/n-Si(100) contacts, which were fabricated by the Ti–Ni–Si solid-state reaction at various

temperatures, were studied using the I–V–T measurement. A simple double-SBH model is used to analysis the experimental I–V curves. The standard deviation of SBH distribution (σ), the low barrier height (Φ_2) and the local series resistance (R_2) are suggested to be indicators of the extent of the barrier height inhomogeneity. Compared with the Ni–Si reaction system, a thin Ti capping layer can hinder the NiSi phase transformation and improve the thermal stability of the NiSi film.

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