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Bifurcation behaviours of peak current controlled PFC boost converter*

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Bifurcation behaviours of the peak current controlled power-factor-correction (PFC) boost converter, including fast-scale instability and low-frequency bifurcation, are investigated in this paper. Conventionally, the PFC converter is analysed in continuous conduction mode (CCM). This prevents us from recognizing the overall dynamics of the converter. It has been pointed out that the discontinuous conduction mode (DCM) can occur in the PFC boost converter, especially in the light load condition. Therefore, the DCM model is employed to analyse the PFC converter to cover the possible DCM operation. By this way, the low-frequency bifurcation diagram is derived, which makes the route from period-double bifurcation to chaos clear. The bifurcation diagrams versus the load resistance and the output capacitance also indicate the stable operation boundary of the converter, which is useful for converter design.

Keywords: peak current control, PFC converter, discontinuous conduction mode, chaos, bifurcation diagram

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1. Introduction

Power factor correction (PFC) of switched power supplies has been one of the most concerning issues in the last decade. There has been various research on the topology and control method of PFC applications.[1,2] Among them, the boost converter is a popular one for its efficiency and easy implementation by the peak current control method.[3] In this paper, the stability of the peak current controlled PFC converter is studied by bifurcation behaviours.

Power electronics system can exhibit a variety of nonlinear behaviours because of the cyclic switching of the circuit topologies. Bifurcation and chaotic phenomena have been reported in some type of DC–DC converters.[4−10] Some typical bifurcation routes to chaos have been recognized, such as period-doubling bifurcation, border collision bifurcation, Neimark–Cacker bifurcation, etc. Most of the analyses use the discrete map that describes the dynamics from one switching time to the next.

Recently, the fast-scale bifurcation in PFC boost converter has been reported in Refs.[11,12]. The slow-scale bifurcation phenomena in average-current controlled PFC boost AC/DC converters have been found by Orabi *et al.*[13,14] For the fast-scale bifurcation analysis of average current controlled PFC converter, the discrete map can be derived because the input-voltage variation can be neglected during the switching period.[11] For the peak current controlled PFC converter, supposing the converter are operating in a continuous conduction mode (CCM), the reference signal is replaced by a ramp signal, then, the iteration map can be obtained to describe the dynamics of the inductor current.[12] However, for the slow-scale bifurcation, it is difficult to derive the discrete map because the input-voltage variation cannot be neglected. A double averaging model is developed in Ref.[15]. It can be used to roughly estimate a low-frequency period-doubling bifurcation point, but the route to chaos remains unclear. The PFC boost converter is commonly designed in CCM,[1,3] and then it is intuitive to analyse the converter using the CCM model for the slow-scale bifurcation.[14] However, it has been found that the PFC boost converter can operate in the discontinuous conduction mode (DCM) near the

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crossover point of the line voltage, in particular, the PFC converter may operate in the DCM during the whole line cycle under the light load condition.[16] The low-frequency bifurcation generally happens in the light load condition, under which the converter may operate alternatively in CCM and DCM. It has been found that the transition from CCM to DCM can cause some bifurcations, chaos and so forth.[17] Therefore, the analysis using the CCM model only may miss some critical details of the bifurcation behaviours for the PFC boost converter. In Ref.[14], only period 2 operation is given by using CCM model.

In this paper, the combined CCM and DCM model is employed to analyse bifurcation behaviours of the peak current controlled PFC boost converter. The structure of this model can be changed automatically from CCM to DCM operation according to the inductor current. The bifurcation diagram is given using the proposed model. By this way, the route from period-doubling bifurcation to chaos is made clear. From the bifurcation diagram derived in this paper, the stable operation areas of the peak current controlled PFC boost converter are made clear with respect to the output capacitance and the load resistance. Moreover, it has been found that the root mean square (RMS) value of the input AC voltage has an important effect on bifurcation behaviours, which was not included in the previous work.[14] These results are very useful for the PFC converter design and analysis.

2. Configuration and operation of the peak current controlled PFC converters

The circuit configuration of the peak current controlled PFC converter is shown in Fig.1. The basic circuit consists of inductor L, capacitor C, diode D, switch S and load resistance R. $v_{\rm in}$ is the rectified input voltage, which is obtained by the diode bridge fed with sinusoidal input voltage. And p_2 and p_3 are proportional factors, $T_{\rm f}$ is the filter time constant, $T_{\rm c}$ is the integrator time constant. Suppose that all components in the circuits are ideal, and no parasite effect is considered.

2.1. Operation mode of PFC converter

In Fig.1, by turning on the switch S at the beginning of the switch cycle, the inductor current $i_{\rm L}$ increases; when it reaches the reference value $i_{\rm ref}$, the switch S is turned off and remains off until the beginning of the next cycle. The peak inductor current is programmed approximately by $i_{\rm ref}$. The switch operation and inductor current waveform are shown in Fig.2(c). According to the different state of the switch S and the diode D, there are three possible states in the converter. Normally the switch S and the diode D are turn on and off in a complementary mode, i.e. one is on while the other is off, and vice versa. In this case, the inductance current is always nonzero, and this mode is said to be CCM. On the other hand, if the inductance current is too small, the inductance current may drop to zero before the next period begins, introducing an "idling" interval during which neither the switch S nor the diode D is conducting. This operation mode is referred to as DCM. Generally, in the DC–DC conversion case, i.e. DC–DC converter application, the converter is set in one of the two operation modes. But in the PFC converter, the situation is quite different; at the top of the reference current, the PFC converter works in CCM (which can be seen in Fig.2(c)), but there exists DCM near the crossover point of the input AC voltage (which can be seen in Fig.2(d)), because the inductor current is small at this stage. Therefore, CCM and DCM can occur alternatively in a PFC converter. With decreasing load, the duration of DCM in half of line period (in our case, it is 10ms) would increase. In the light load condition the converter may operate in DCM during all the half of line period.

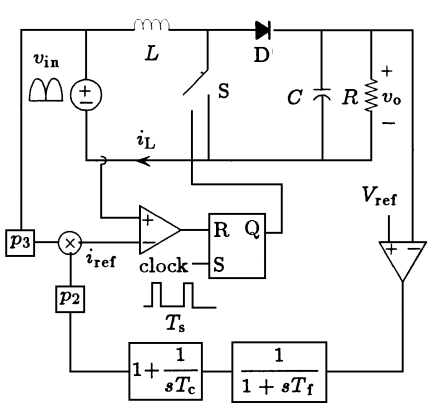


Fig.1. Configuration of the peak current control PFC converter.

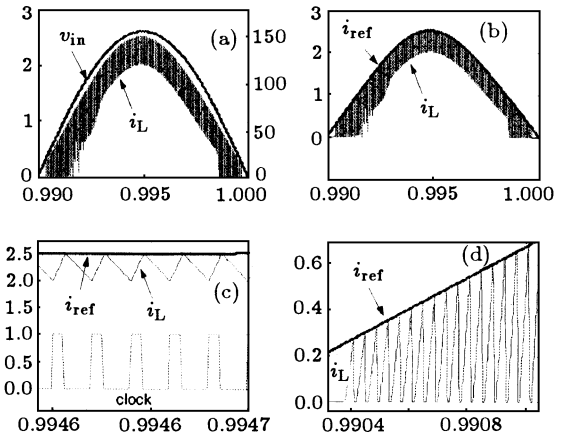


Fig.2. Corresponding waveform of the peak current control boost PFC converters: (a) input rectified voltage and inductor current waveform; (b) reference current and inductor current waveform; (c) enlarged reference current, inductor current and clock signal waveform; (d) reference current and inductor current waveform near the crossover point of the line voltage, which indicates clearly the DCM operation.

2.2. Control loop of PFC converter

The function of the PFC converter lies in two aspects: firstly, the converter can convert the rectified AC voltage into DC output and keep the output voltage v_o at a constant value; secondly, the converter can keep the waveform of current drawn from the AC source being sinusoidal and in the same phase with the voltage, so that the near-unity power factor can be obtained (the waveform of the input rectified voltage and the inductor current is shown in Fig.2(a)). Two control loops are employed in the PFC converter to implement the function. The outer voltage loop, consisting of a first-order filter, a PI controller and a proportional factor, serves to control the output voltage v_o. The reference current signal i_{ref} is derived from the output of voltage control loop multiplied by a signal proportional to the input voltage, so that the reference current signal i_{ref} has the waveform of the input voltage with the amplitude controlled by the voltage loop. By changing the amplitude of the reference current, the output voltage v_o can be adjusted. The inner current loop is designed to let the inductor current i_L track the reference current i_{ref} in a peak current programming mode or peak current control mode, which is described in last section.

2.3. Mathematical model of PFC converter

The combined CCM and DCM model is used for the bifurcation analysis for PFC converter; the model is given as follows:

$$\dot{\boldsymbol{x}} = A_1\boldsymbol{x} + B_1 v_{in} \quad \text{if} \quad S \quad \text{is on}, \tag{1}$$

$$\dot{\boldsymbol{x}} = A_2\boldsymbol{x} + B_2 v_{in} \quad \text{if} \quad S \quad \text{is off and } i_L > 0, \tag{2}$$

$$\dot{\boldsymbol{x}} = A_3\boldsymbol{x} + B_3 v_{in} \quad \text{if} \quad S \quad \text{is off and } i_L = 0, \tag{3}$$

where v_{in} is the rectified input voltage, $\boldsymbol{x}$ is the state vector defined by $\boldsymbol{x} = \begin{bmatrix} v_C & i_L \end{bmatrix}^T$, v_C denotes the voltage across the capacitor C and i_L denotes the current through the inductor L, v_C is equal to the output voltage across the load resistance R, i.e. $v_C{=}v_o$. A_i and B_i (i=1, 2, 3) are given by

$$A_1 = \begin{bmatrix} -\dfrac{1}{RC} & 0 \\ 0 & 0 \end{bmatrix}, \tag{4}$$

$$A_2 = \begin{bmatrix} -\dfrac{1}{RC} & \dfrac{1}{C} \\ -\dfrac{1}{L} & 0 \end{bmatrix}, \tag{5}$$

$$A_3 = \begin{bmatrix} -\dfrac{1}{RC} & 0 \\ 0 & 0 \end{bmatrix}, \tag{6}$$

$$B_1 = B_2 = \begin{bmatrix} 0 & 1/L \end{bmatrix}^T, \tag{7}$$

$$B_3 = \begin{bmatrix} 0 & 0 \end{bmatrix}^T. \tag{8}$$

The structure of this model can be changed automatically from CCM to DCM operation, and vice versa, according to the state of the switch and the inductor current.

The current reference signal is given by

$$i_{ref} = p_2 p_3 v_{in} (V_{ref} - v_o) \frac{1}{1 + sT_f} \left(1 + \frac{1}{sT_c}\right). \tag{9}$$

From the model of the PFC converter, it can be seen that the topology of the circuits varies according to the state of the switch and inductor current. There are three consecutive dynamics from Eqs.(1)–(8) covering the possible CCM and DCM operation; each of the dynamics is linear but the total dynamics are nonlinear, which is referred to as piecewise nonlinearity. Besides this nonlinearity, there is the multiplication operation in the PFC converter, which makes the PFC converter more complex than the general DC–DC converter. In addition, there are two periodical signals in PFC converter, i.e. the time variant input rectified voltage with low frequency and the switching signal with high frequency. There are no theoretical methods that can be applied directly for bifurcation analysis to such a complex AC–DC converter system.

Fortunately, the computer program can be used to simulate the dynamic behaviours of this system. For the fast-scale instability, even though the bifurcation occurs under certain parameters, the inductor current waveform is still approximately sinusoidal. Thus, the fast-scale instability has little effect on the power factor characteristics. However, for the low-frequency bifurcation, the inductor current waveform will become non-sinusoidal, the power factor will dramatically decrease. Therefore, much attention should be given to the low-frequency instability and bifurcation behaviours.

3. Bifurcation behaviours of peak current controlled PFC converters

The computer simulation is performed using the model derived in the last section. The simulation program is developed in MATLAB. The parameters used in simulation are given in Table 1.

3.1. Fast-scale instability of the peak current controlled PFC converter

Fast-scale instability means the instability and bifurcation on the scale of switching frequency, the instability waveform of inductor current with the fast scale is shown in Fig.3(a). The sampled data of inductor current with the switch frequency (in our case, 50kHz) is given in Fig.3(b), from which it is clear that the inductor current undergoes a period-double bifurcation and becomes chaotic after and before the crossover point of the input sinusoidal voltage. When the parameters change to another set, the waveform of inductor current becomes chaotic during the whole line cycle, this can be seen in Figs.4(a) and 4(b); in Fig.4(b), the sampled data clearly shows the chaotic state of the inductor current. These results are consistent with the results in Ref.[11].

Table 1. Parameters used in the simulations.

parameters	value
Input voltage $v_{\rm in}$	80–110$V_{\rm rms}$/50Hz
Reference output voltage $V_{\rm ref}$	230–565.6V
Inductance L	1.3–2mH
Capacitance C	40–470μF
Load resistance R	80–3000Ω
Switch period $T_{\rm s}$	20ms
Filter time constant $T_{\rm f}$	4ms
Controller time constant $T_{\rm c}$	1/70s
Feedback gain p_2	1/60
Feedforward gain p_3	0.08

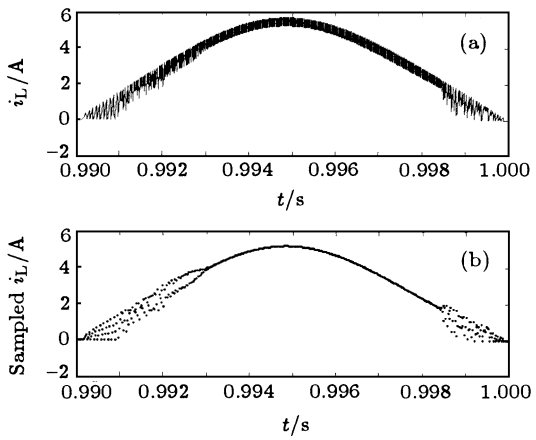


Fig.3. Fast-scale bifurcation and chaos, with $R = 135\Omega$, $V_{\rm ref} = 230$V, $v_{\rm in} = 110V_{\rm rms}$, $L = 2$mH, C=470μF.

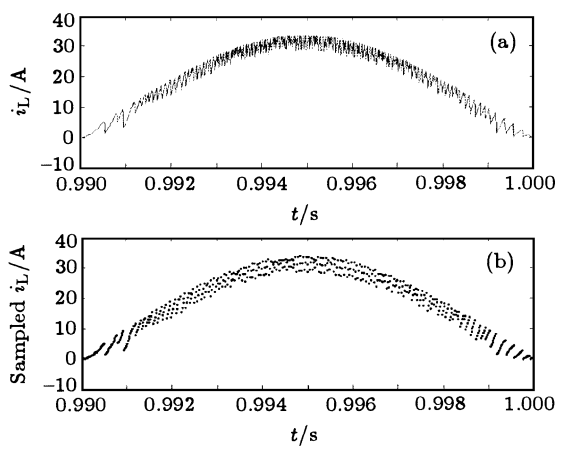


Fig.4. Fast-scale chaotic operation, with $R = 135\Omega$, $V_{\rm ref} = 400\sqrt{2}$V, $v_{\rm in} = 110V_{\rm rms}$, $L = 1.3$mH, $C = 470\mu$F.

3.2. Low-frequency period operation of the peak current controlled PFC converter

In normal cases, the converter will keep the inductor current sinusoidal and keep the output voltage constant with a small fluctuation; in this way, the converter can obtain a near-unity power factor. The phase plot and the time-domain waveform of the inductor current $i_{\rm L}$ and the output voltage $v_{\rm o}$ are given in Fig.5, where the inductor current is filtered by a sixth-order low-pass filter to remove the switching frequency components and obtain a more legible waveform (in the following figures, the current waveform is derived in the same way). From Fig.5, it can be seen that the converter is operating in period 1, i.e. double the line frequency (100Hz). This case is referred to as stable operation in the power switch converters. In this case, the power factor of the converter is near unity and the output is kept at the reference voltage 230V. The converter meets the two functional requirements.

When the parameters change, we have Fig.6 through Fig.8, in which the phase plot and time domain waveform of the inductor current $i_{\rm L}$ and the output voltage $v_{\rm o}$ are shown. The PFC converter are working in low-frequency period 2, period 4 and period 6 respectively. In period 2 operation shown in Fig.6, the period of the output voltage and the inductor current becomes double of the period 1 operation i.e. 0.02s. For period 4 and period 6 operation the period becomes 0.04s and 0.06s respectively. The higher period operations can also be obtained if the parameters are changed until the chaos occurs as shown in Fig.9, where the chaotic attractor and the corresponding time domain waveform of the inductor current and output voltage are shown in Figs.9(a), 9(b) and 9(c).

From Fig.6 to Fig.9, it should be pointed out that when the low-frequency bifurcation and chaos occur, the power factor of the PFC converter would decrease dramatically, because the inductor current becomes non-sinusoidal, the PFC functions are destroyed, which induces plenty of noises. On the other hand, comparing Fig.3 with Fig.5, we have a near-unity power factor even though the fast-scale bifurcation and chaos have happened. Therefore, the low-frequency bifurcation and chaos should be paid more attention to avoid them so as to obtain the expected performance.

From Fig.5–Fig.9, we see that there exist plenty of dynamical behaviours in the peak current controlled PFC converter; in order to have a clear look at the relationship between the steady state operation and parameter set, the low-frequency bifurcation diagram is given in the next section.

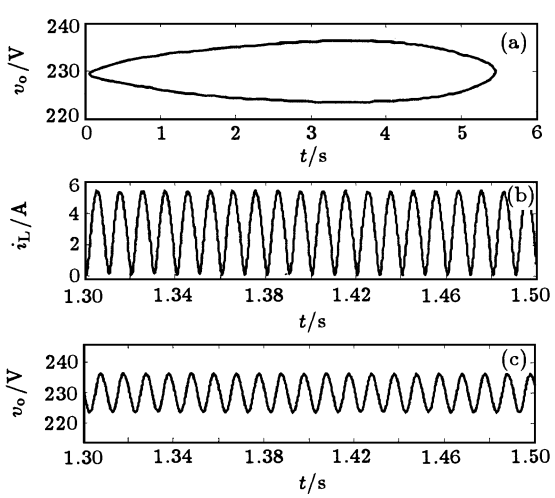


Fig.5. Low-frequency period 1 operation, with $C = 470\mu$F, $R = 135\Omega$, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

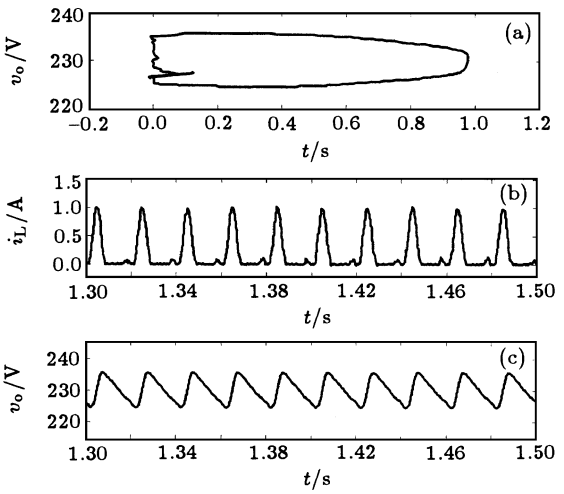


Fig.6. Low-frequency period 2 operation, with $C = 140\mu$F, $R = 2000\Omega$, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

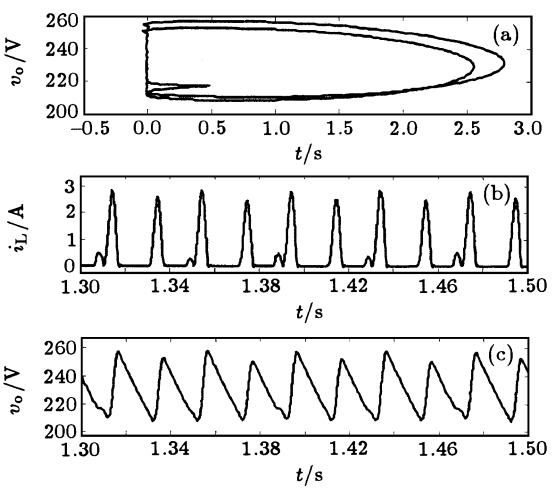


Fig.7. Low-frequency period 4 operation, with $C = 80\mu$F, $R = 900\Omega$, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

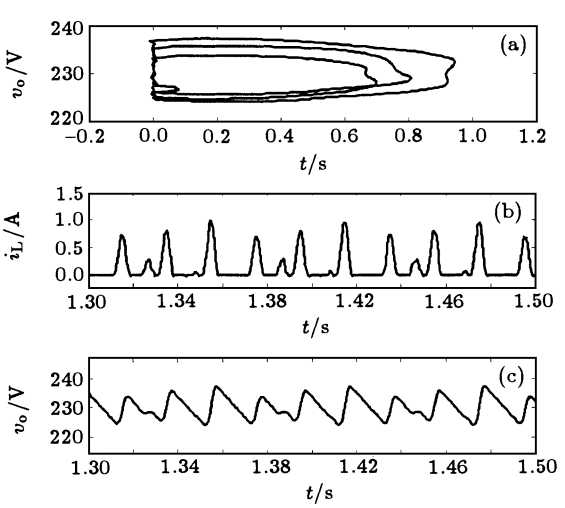


Fig.8. Low-frequency period 6 operation, with $C = 110\mu$F, $R = 2500\Omega$, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

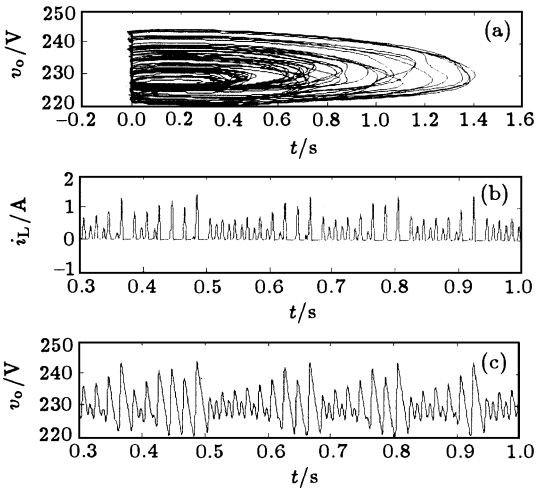


Fig.9. Low-frequency chaotic operation, with $C = 80\mu$F, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 90$V$_{\rm rms}$, $R = 2135\Omega$.

3.3. Low-frequency bifurcation behaviours of the peak current controlled PFC converter

Low-frequency bifurcation means bifurcation and chaotic operation on the scale of double the line frequency. Bifurcation diagrams versus capacitance and load resistance are shown in Fig.10–Fig.13. In the bifurcation diagram, the output voltage $v_{\rm o}$ is sampled at double the line frequency. The bifurcation diagram can be interpreted as follows: one point corresponding to a parameter means period 1 operation (with the frequency of 100Hz) and two points mean period 2 operation (with the frequency of 50Hz), and so on. When the points corresponding to a parameter are mixed into a dashed line, chaos occurs in the system.

From Fig.10, it can be seen that as the output capacitance decreases, bifurcation occurs with the capacitance value about 155μF, where period 2 occurs, and then period 4, etc, occur in sequence. Finally, the two pieces of chaotic area connect with each other and become a large area of chaotic operation, which gives a period-doubling bifurcation route to chaos. When the capacitance becomes smaller, the output voltage turns back to period 1 operation, but in this area, the fluctuation of output voltage becomes too large to be used for power supply if the load of the converter is heavy.

From Fig.11, it can be seen that the period-doubling bifurcation and border-collision bifurcation[16] would occur with the increase of the load resistance (i.e. with the decrease of the load), if the output capacitance is small.

From Figs.12 and 13, it can be seen that the bifurcation is quite different when the parameter set is different. Bifurcation point and its behaviours after the bifurcation are also different. These bifurcation diagrams indicate the rich possible dynamics in such PFC converters.

From the engineering viewpoint, the bifurcation diagrams also indicate the stable operation regime of the peak current controlled PFC converter, which are very useful for the designers to understand and design the converters.

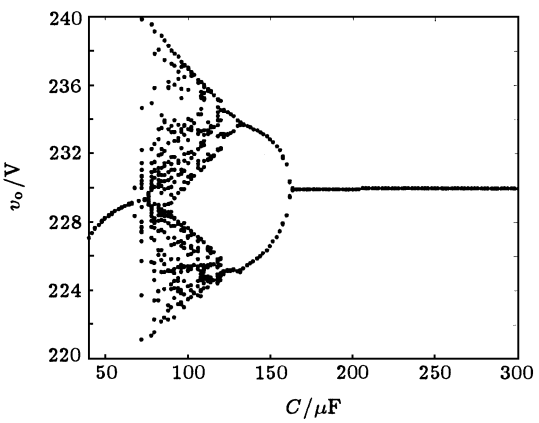


Fig.10. Output voltage bifurcation diagram versus capacitance value, with $R = 2000\Omega$, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

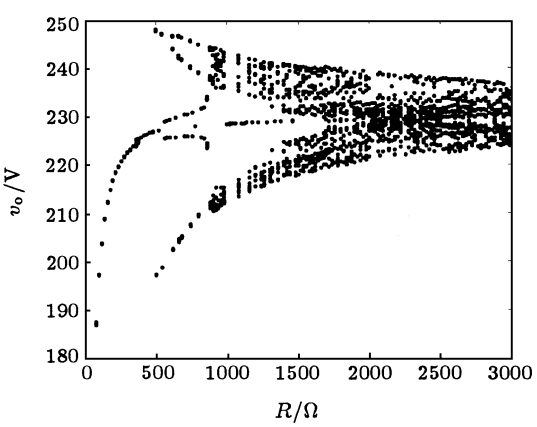


Fig.11. Output voltage bifurcation diagram versus load resistance, with $C = 80\mu$F, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 110$V$_{\rm rms}$.

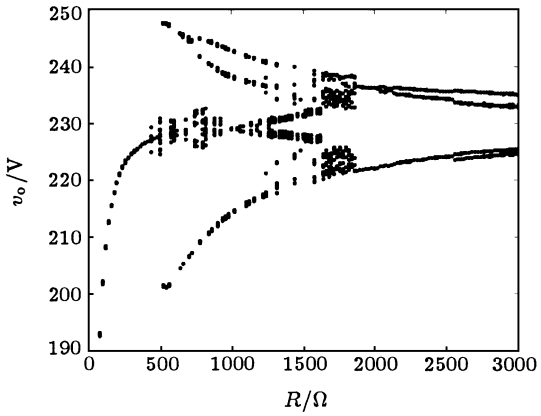


Fig.12. Output voltage bifurcation diagram versus resistance , with $C = 80\mu$F, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 100{\rm V}_{\rm rms}$.

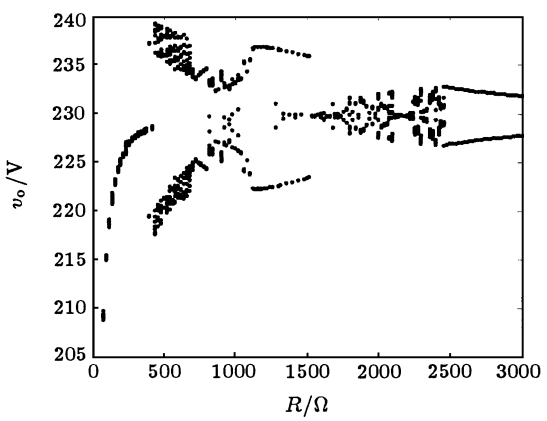


Fig.13. Output voltage bifurcation diagram versus resistance, with $C = 100\mu$F, $L = 2$mH, $V_{\rm ref} = 230$V, $v_{\rm in} = 90{\rm V}_{\rm rms}$.

4. Conclusion

In the conventional power electronics, stability means a condition in which the converter is working in the expected periodic regime. All those subharmonic, quasi-periodic and chaotic operations are regarded as undesirable and should be avoided even though it is perfectly predicted.[11] In this paper, the combined CCM and DCM model is proposed to interpret the bifurcation behaviours (both fast-scale and low-frequency/slow-scale bifurcation) of the peak current controlled PFC converter, to cover the possible DCM operation of the converters. The fast- scale instability is reproduced and the low-frequency bifurcation diagram is derived, which make the route from period-doubling bifurcation to chaos clear. Compared with the fast-scale instability, the low-frequency bifurcation behaviours degrade the power factor more seriously. Therefore, the low-frequency bifurcation should be paid more attention to better utilize the function of the PFC converter.

From an application viewpoint, the bifurcation diagram derived in this paper indicates clearly the stable operation regime of the converter among all the parameter sets, which is very helpful for the PFC converter design and analysis. From the theoretical viewpoint, the method in this paper just reflects the inherent dynamics of the peak current controlled PFC converters, the theoretical method, such as the possible iteration map like the case of DC–DC converter, is still open for further research.

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