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6H-SiC Schottky barrier source/drain NMOSFET with field-induced source/drain extension*

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A novel SiC Schottky barrier source/drain NMOSFET (SiC SBSD-NMOSFET) with field-induced source/drain (FISD) extension is proposed and demonstrated by numerical simulation for the first time. In the new device the FISD extension is induced by a metal field-plate lying on top of the passivation oxide, and the width of Schottky barrier is controlled by the metal field-plate. The new structure not only eliminates the effect of the sidewalls but also significantly improves the on-state current. Moreover, the performance of the present device exhibits very weak dependence on the widths of sidewalls.

Keywords: SBSD-MOSFET, FISD, sidewall, 6H-SiC
PACC: 7280, 7330, 7340S, 7220

1. Introduction

SiC Schottky barrier source/drain MOSFET (SiC SBSD-MOSFET) with metallic source and drain does not require source/drain(S/D) ion implantation and subsequent annealing steps at extremely high temperature. Therefore fabrication is simpler. Also, it has not the problems of crystal damage caused by ion implantation[1] and high S/D parasitic resistance[2] induced by low activation rate of implanted atoms. With these advantages, it appears to be quite attractive for the applications of SiC MOSFETs. But there have been few papers about SiC SBSD-MOSFETs published so far.[3,4,5]

Gate sidewall spacers are required for the insulation between the gate and metallic S/D. This may cause a conduction problem in the channel below sidewalls. Thus the width (δ) of sidewall should be determined by a trade-off between isolation of gate and S/D electrode and channel conduction. Our simulated results show that the device performance is quite sensitive to the width of sidewall. The device will not be turned on normally if sidewall width exceeds 0.1μm.[3] In addition, the output current of the device is still limited by the reverse-biased Schottky barrier at the source side[4] even though the effect of the sidewalls on the device can be neglected. Higher gate voltage is required to produce sufficient output current if contact material of S/D is fixed.

In this paper, a novel 6H-SiC SBSD-NMOSFET with field-induced source/drain (FISD) extension is proposed and demonstrated for the first time. It not only eliminates the effect of the sidewall on the device performance, but also improves the output current.

2.Structure of the novel device

The new device (Fig.1) is structurally similar to SBSD MOSFETs reported previously[6] except for a metal field-plate (i.e. the sub-gate) lying on top of the passivation oxide. The metal sub-gate effectively covering the channel region is formed simultaneously during the regular metal patterning, so no extra processing step is required. During device operation, a high bias is applied to the sub-gate to form a FISD extension below the sidewalls. The polarity of the sub-gate bias is positive for an n-channel device, and negative for a p-channel device.

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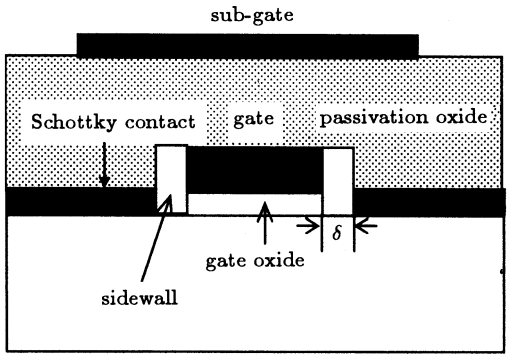


Fig.1. Schematic structure of SBSD-MOSFET with FISD.

3. Results and discussion

A 6H-SiC SBSD-NMOSFET with FISD extension has been simulated with a 2D numerical simulator MEDICI. The basic simulation approach of MEDICI and the adopted models can be found in our previous work.[3,5] In the simulation the gate length of device is taken as 1.5μm, oxide thickness 20nm, acceptor doping concentration (N_A) 5×10^{16}cm^{-3} and the work function of S/D metal 3.9eV. The thickness of the passivation oxide between the sub-gate and gate is around 0.1μm.

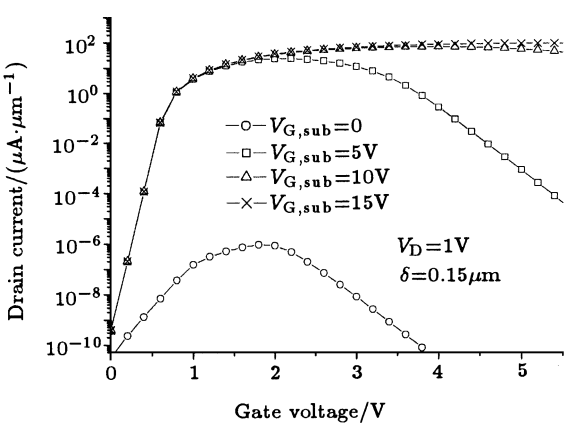


Fig.2. Transfer characteristics for various sub-gate voltages at V_D=1V, δ=0.15μm.

Figures 2 and 3 show the effects of sub-gate ($V_{G,sub}$) on the device characteristics with δ=0.15μm at room temperature. It can be seen that increasing $V_{G,sub}$ will eliminate the effect of the sidewalls. Under V_G (gate voltage)> V_{th} (threshold voltage) and $V_{G,sub}$=0, the device does not operate normally because of the existence of the un-gated channel regions under the sidewall spacers. But this phenomenon is evidently reduced by FISD extension below sidewalls with a positive sub-gate bias applied. To be different from previous SBSD-MOSFETs, the width of the reverse-biased Schottky barrier at the source side is modulated by the sub-gate voltage. The barrier will be narrowed when the positive sub-gate bias increases, thus resulting in higher tunnelling current. So the proposed device effectively improves on-state current at given gate voltage and contact material.

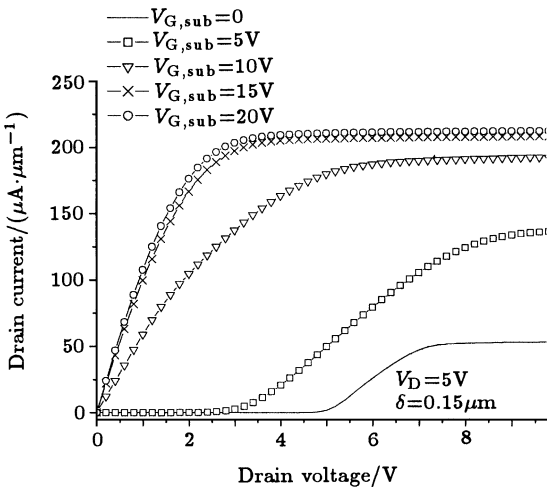


Fig.3. Output characteristics for various sub-gate voltage at V_G=5V, δ=0.15μm.

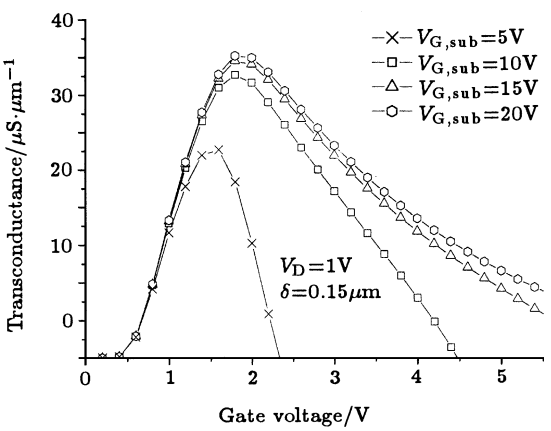


Fig.4. Transconductance versus V_G for various sub-gate voltage at V_D=1V, δ=0.15μm.

It is observed in Fig.4 that the maximal transconductance of the device is but slightly affected by the sub-gate as long as the sub-gate bias is sufficiently large. The transfer currents at $V_{G,sub}$=15V, V_D=1V and different δ are shown in Fig.5. It can be seen that the off-state current and the $I - V_G$ characteristics in subthreshold regions are essentially independent of the widths of sidewalls when the sub-gate bias is large enough. On the other hand, the on-state current has slight increase as the sidewalls become narrower. This is reasonable since the parasitic resistance decreases with reduced sidewalls. So the performance of the

presented device is not sensitive to the widths of sidewalls, which makes the process control easier and more reliable.

4. Conclusion

A novel SiC SBSD-NMOSFET with FISD extension is proposed in this paper. A top metal field-plate (i.e. sub-gate) is formed simultaneously during the regular metal patterning, so no additional mask or processing is needed. During device operation, a high fixed positive bias is applied to the sub-gate to form a FISD extension below sidewalls. The width of Schottky barrier is controlled by the sub-gate bias. The simulated results show that the structure with FISD extension not only eliminates the effect of the sidewalls on the device performance but also significantly improves the on-state current when the sub-gate bias is large enough. Moreover, the device performance is not sensitive to the widths of sidewalls with FISD extension, so process control becomes easier and more reliable.

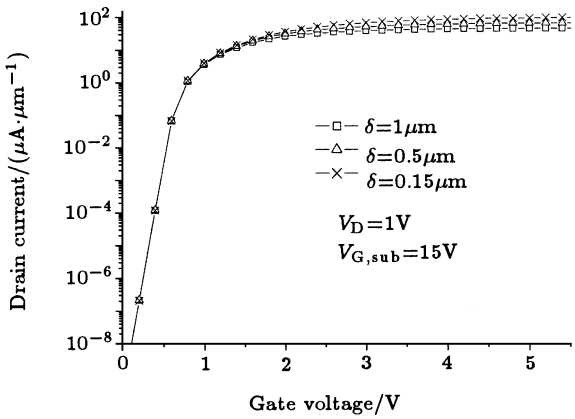


Fig.5. Transfer characteristics for various widths of sidewalls at $V_{\rm D}$= 1V, $V_{\rm G,sub}$=15V.

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