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Effect of the technology of implanting nitrogen into buried oxide on the radiation hardness of the top gate oxide for partially depleted SOI PMOSFET

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The effect of implanting nitrogen into buried oxide on the top gate oxide hardness against total irradiation does has been investigated with three nitrogen implantation doses (8×10^{15}, 2×10^{16} and 1×10^{17}cm^{-2}) for partially depleted SOI PMOSFET. The experimental results reveal the trend of negative shift of the threshold voltages of the studied transistors with the increase of nitrogen implantation dose before irradiation. After the irradiation with a total dose of 5×10^{5}rad(Si) under a positive gate voltage of 2V, the threshold voltage shift of the transistors corresponding to the nitrogen implantation dose 8×10^{15}cm^{-2} is smaller than that of the transistors without implantation. However, when the implantation dose reaches 2×10^{16} and 1×10^{17}cm^{-2}, for the majority of the tested transistors, their top gate oxide was badly damaged due to irradiation. In addition, the radiation also causes damage to the body-drain junctions of the transistors with the gate oxide damaged. All the results can be interpreted by tracing back to the nitrogen implantation damage to the crystal lattices in the top silicon.

Keywords: SOIPMOSFET, radiation hardness, nitrogen implantation, threshold voltage shift
PACC: 6180E, 7340Q, 6170T

1. Introduction

SOI (silicon on insulator) technology is increasingly developing because of its high performance and low-power circuits.[1−3] This is because the buried oxide reduces the junction capacitance and the leakage current. In particular, the small volume and p–n junction area of SOI integrated circuits have advantages for single event upset and high dose rate transient upset effects. However, conventional SOI technologies are not fully adapted to hardened applications. Unless the buried oxide is hardened, it usually induces an additional path of leakage currents for the SOI NMOSFET after total dose irradiation.[4] Some special technologies have been introduced to enhance the buried oxide hardness to the total dose irradiation.[5−6] In this paper, the technology of implanting nitrogen into buried oxide is used for the improvement of the total dose radiation hardness of the buried oxide layer in the SOI structures. But, on the other hand, while the buried oxide is hardened by the implantation of nitrogen into the buried oxide, it is necessary to consider the influence of this technology on the radiation hardness of the top gate oxide formed by the thermal oxidation process of silicon. The reason for this is that the implantation-induced defects in the top silicon may deteriorate the gate oxide quality and thus decrease its radiation hardness. However, this problem has not been well studied. In order to optimize the implantation conditions and elevate the radiation hardness of the SOI transistors, the effect of implanting nitrogen into buried oxide layer on the radiation hardness of the top gate oxide layer for partially depleted SOI PMOSFET is researched and some useful results have been obtained.

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2. Device and experiment

First, standard SIMOX (separation-by-implanted-oxygen) wafers were formed through implanting oxygen into p-type (100) silicon wafers with a resistivity of 20Ω·cm and followed by annealing at high temperature in O_2+Ar_2 atmosphere. Then, nitrogen of different doses was implanted into the buried oxides in the wafers at the same implantation energy (see Table 1). The wafer 0# without nitrogen implantation is used as a control sample. Subsequently, all the wafers were annealed at 1200°C in N_2 atmosphere. The top silicon thickness of the SIMOX wafers is about 200nm, and the buried oxide thickness is about 375nm.

Table 1. Nitrogen implantation doses and energy for the SIMOX wafers.

Wafers	Doses/cm^{-2}	Energy/keV
0#	0	
1#	8×10^{15}	160
2#	2×10^{16}	160
3#	1×10^{17}	160

For partially depleted SOI NMOSFETs, the back channel leakage current due to irradiation may have a bad influence on the measured results associated with the top gate oxide hardness to the total dose radiation. Therefore, the tested SOI transistors fabricated on the SIMOX wafers 0#–3# are the partially depleted SOI PMOSFETs rather than NMOSFETs. The gate length and width are 1.2μm and 3.4μm, respectively. The gate oxide thickness is 25 nm. In addition, the fabricated SOI transistors have the body contacts. The transistor characteristics were measured using the Keithley 4200 system before and after irradiation. The transistors were irradiated with Co-60 source at a dose rate of 1.673×10^4 rad(Si)/min and the total dose is up to 5×10^5rad(Si). The transistor gate and source were biased at 2V; the transistor drain and body were biased at 0 V during irradiation. For convenience, the fabricated transistors are marked by the signs 0#–3# corresponding to the SIMOX wafers 0#–3#, respectively. Thus the transistor 0#–1 denotes the first transistor tested of the group of transistors fabricated on the SIMOX wafer 0#, etc.

3. Experimental results and discussion

The top gate threshold voltages of the transistors are extracted from the measured top transistor transfer characteristics before and after irradiation. The results are summarized in Tables 2–5. The symbols $V_{\rm th}$ and $\Delta V_{\rm th}$ denote respectively the threshold voltage and the corresponding shift due to irradiation. In particular, in each group of transistors 2# and 3#, three among the five tested transistors were found to be seriously damaged by irradiation. As a result, the top gate threshold voltage becomes insignificant for them (as shown in Fig.1) and their output characteristics are very different from the normal ones after irradiation (as shown in Fig.2).

Table 2. Top gate threshold voltages and their shifts for the transistor 0# before and after irradiation.

Transistors	Pre-irradiation $V_{\rm th}$/V	Post-irradiation $V_{\rm th}$/V	$\Delta V_{\rm th}$/V
0#–1	–1.57	–2.19	–0.62
0#–2	–1.65	–2.32	–0.67
0#–3	–1.58	–2.55	–0.97
0#–4	–1.50	–2.10	–0.60
0#–5	–1.50	–2.60	–1.10

Table 3. Top gate threshold voltages and their shifts for the transistor 1# before and after irradiation.

Transistors	Pre-irradiation $V_{\rm th}$/V	Post-irradiation $V_{\rm th}$/V	$\Delta V_{\rm th}$/V
1#–1	–1.99	–2.49	–0.50
1#–2	–1.79	–2.38	–0.59
1#–3	–2.23	–2.72	–0.49
1#–4	–1.89	–2.45	–0.56
1#–5	–1.80	–2.29	–0.49

Table 4. Top gate threshold voltages and their shifts for the transistor 2# before and after irradiation.

Transistors	Pre-irradiation V_{th}/V	Post-irradiation V_{th}/V	ΔV_{th}/V
2#–1	–1.93	–	–
2#–2	–1.66	–2.43	–0.77
2#–3	–1.71	–2.18	–0.47
2#–4	–2.17	–	–
2#–5	–1.80	–	–

Table 5. Top gate threshold voltages and their shifts for the transistor 3# before and after irradiation.

Transistors	Pre-irradiation V_{th}/V	Post-irradiation V_{th}/V	ΔV_{th}/V
3#–1	–2.67	–3.50	–0.83
3#–2	–2.66	–	–
3#–3	–2.63	–	–
3#–4	–2.81	–3.35	–0.54
3#–5	–2.64	–	–

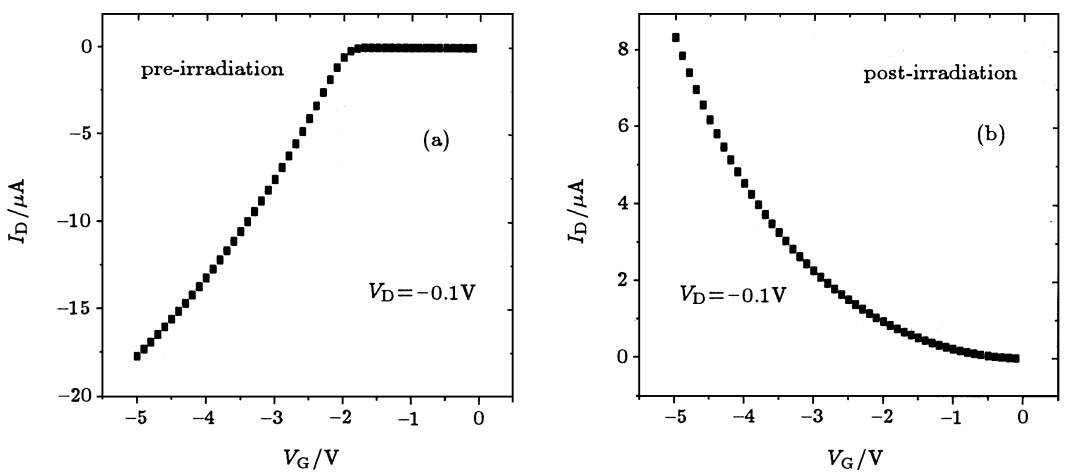


Fig.1. Typical pre-irradiation transfer characteristics (a) and post-irradiation transfer characteristics (b) for the seriously damaged transistors of 2# and 3# due to irradiation. I_D, V_G and V_D denote the drain current, gate and drain voltage, respectively.

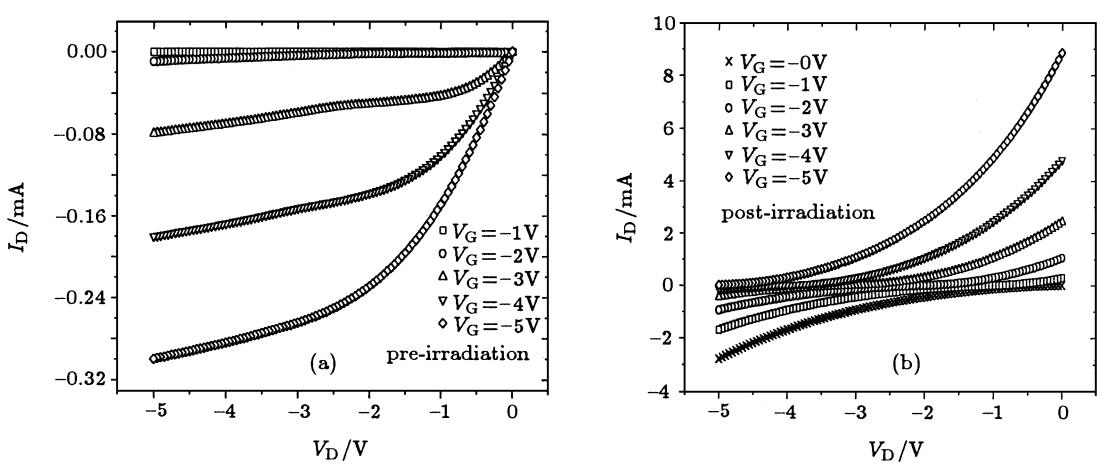


Fig.2. Typical pre-irradiation output characteristics (a) and post-irradiation output characteristics (b) for the seriously damaged transistors of 2# and 3# due to irradiation. I_D, V_D and V_G denote the drain current, drain and gate voltage, respectively.

It is obvious that the pre-irradiation threshold voltages of the transistors 1#–3#, which are fabricated on the SIMOX wafers 1#–3# with nitrided buried oxide layer, are lower than the ones of the transistor 0# processed on the SIMOX wafer 0# without nitrogen in the buried layer. This negative shift of the threshold voltage agrees to a large extent with a previous work[7] on the characteristics of the partially depleted SOI NMOSFET, in which nitrogen was implanted into the buried oxide to reduce the radiation sensitivity of the buried layer. It is well known that the threshold voltage shift can be caused by the positive fixed oxide charges in the gate oxide and the interface-trapped charges between the gate oxide and body silicon. Surely, the lattice defects induced by the previous nitrogen implantation process in the top silicon will result in a poor gate oxide and Si/SiO_2 interface formed in the following thermal oxidation. As a result, the fixed oxide charge and interface trap density are higher for the transistors 1#–3# than 0#. In order to form a p-channel, a negative bias should be applied to the gate of the transistor. This leads to the silicon energy band near the surface to be bent upward. Thus, the donor-like interface traps will release the trapped electrons and serve as the positive fixed ions to affect the threshold voltage, just like the positive fixed oxide charge, when the body silicon surface is strongly inverted. Both the fixed oxide charges and the positive interface-trapped charges will cause a negative threshold voltage shift. Therefore, the transistors 1#–3# are expected to have a lower threshold voltage than the transistor 0# and the maximum nitrogen implantation dose 1×10^{17} cm^{-2} to correspond to the lowest threshold voltage due to the implantation-induced lattice defects in the top silicon. However, the threshold voltages of the transistors 1# and 2# are approximately equal on the average, despite the different nitrogen implantation dose. This suggests that the lattice defect density in the top silicon may affect the distribution of the interface trap density. If the interface traps induced by these defects corresponding to a certain implantation dose tend to concentrate near the valence band top and conduction band bottom in the silicon band gap, the influence of the interface-trapped charges on the threshold voltage will be suppressed.

After irradiation, the negative shift of the threshold voltages occurs as expected (Fig.3), except for the destroyed transistors. A traditional model can be used to account for this shift. The ionizing radiation brings about the electron–hole pairs in the gate oxide. The electrons escaping initial recombination are swept out of the gate oxide layer very quickly and the holes are driven toward the Si/SiO_2 interface at a lower speed under a positive gate bias relative to the body because of the great difference between the electron mobility and the hole mobility.[8] A fraction of the holes are trapped near the interface, and the remainder moves into the body. In addition, the radiation can create the donor- and acceptor-like interface traps. Both the trapped holes acting as fixed positive charges and the donor-like interface traps losing their electrons result in the negative shift of the post-irradiation threshold voltages as mentioned above. Furthermore, the

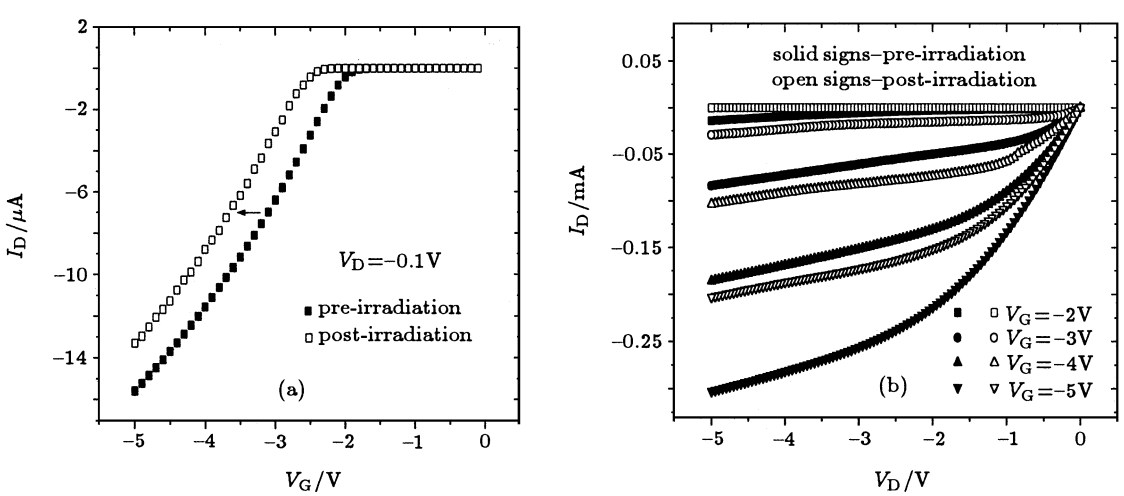


Fig.3. Typical transfer characteristics (a) and output characteristics (b) before and after irradiation. A remarkable threshold voltage shift occurs after irradiation in panel (a) and causes a notable change of the corresponding output characteristics in panel (b). The meaning of all the symbols are the same as in Figs.1 and 2.

threshold voltage shifts of the transistor 1# are smaller than that of the transistor 0#. This may be interpreted in terms of the electron trapping due to the oxide traps inside the gate oxide.[9] Under a positive gate voltage during irradiation, a part of the free electrons near the silicon surface will be injected into the gate oxide and trapped by the oxide traps. The trapped electrons can partly offset the influence of the trapped holes on the threshold voltage shift. The nitrogen implantation damage to the top silicon will lead to a poor thermal oxide and a higher density of the oxide electron traps. Consequently, there are the more trapped electrons in the gate oxide of the transistor 1# than 0# after irradiation. The difference of the threshold voltage shifts between the transistors of the same type is probably caused by the non-uniform distribution of the hole traps and interface-trapped charges after irradiation, and related to the pre-irradiation initial values to some extent.

For the completely destroyed transistors in the groups of the transistors 2# and 3# after irradiation, their gate oxide insulators are badly damaged by the irradiation and large gate leakage currents therefore arise with the gate voltage applied (as shown in Fig.4).

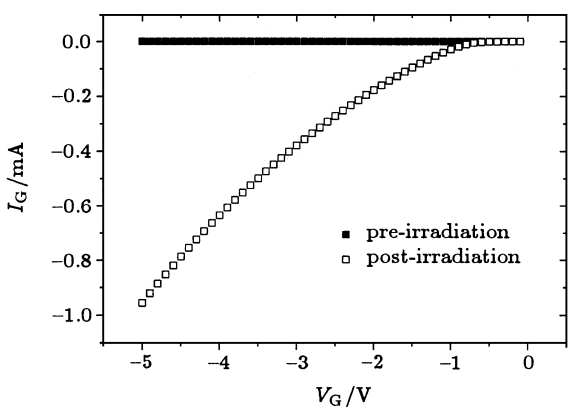


Fig.4. Typical gate leakage current I_G versus gate voltage V_G before and after irradiation for the destroyed transistors under the conditions given in the present paper.

A schematic model can be used to illustrate the irradiation damage mechanism of the gate oxide (as shown in Fig.5). During irradiation, the holes produced by ionizing radiation will accumulate in the gate oxide till reaching a certain homeostasis under a positive gate voltage. Because the free electrons due to radiation have a much higher mobility than the holes, the electrons are speedily driven out of the gate oxide by the external electric field, with the holes transported at a much lower speed as mentioned in Ref.[8]. As a result, the number of holes will greatly exceed that of the electrons in the oxide and a positive space charge layer will be established. Together with the electrons in the accumulation layer near the silicon surface, this positive space charge layer consisting of the radiation-induced holes generates an inner electric field, the direction of which is along the external field and therefore enhances the field intensity in the gate oxide. In particular, for a p-channel transistor, when the gate is biased at a positive value, there are a large amount of free electrons near silicon surface due to accumulation. Thus, a good many of the hot electrons in the accumulation layer will be injected into the gate oxide under the enhanced field, and cause damage to the oxide. The poorer the oxide quality is, the weaker the resistance to this damage. On the other hand, the lower pre-irradiation threshold voltage implies the higher built-in electric field intensity. This will surely increase the amount and energy of the injected hot electrons during irradiation. Also, the irradiation with high dose rate can create a space charge layer with high hole density according to the above analysis. Besides the oxides, the output characteristic at V_G =0V in Fig.2(b) shows the body-drain junctions in the destroyed transistors were also damaged badly due to irradiation.

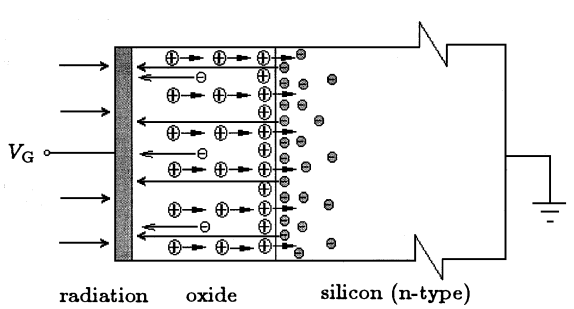


Fig.5. Schematic illustration of the irradiation damage mechanism of the gate oxide for a p-channel transistor at a positive gate voltage $V_G(>0)$ during irradiation.

4. Conclusions

According to the above experimental results and detailed discussion, the process of implanting nitrogen into the buried oxide of the SIMOX wafer will influence the gate oxide hardness to the total dose irradiation. When the nitrogen implantation dose is low (8×10^{15}cm^{-2}) and the total dose of irradiation is 5×10^5rad(Si), the gate oxide hardness improves slightly from the viewpoint of threshold voltage shift induced by radiation under a positive gate voltage

of 2V. But, for the majority of the studied transistors, nitrogen implantation with higher doses (2×10^{16} and 1×10^{17} cm^{-2}) will cause large leakage current through the gate oxides under the normal bias configuration of p-channel transistors after irradiation with 5×10^{5}rad(Si) (i.e. the transistors are destroyed). The nitrogen implantation damage to the crystal lattices in the top silicon is probably responsible for these results. With the high doses of nitrogen implantation, the fact of the irradiation damage to the drains also supports this opinion.

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