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Structural and electrical properties of $SrTiO_3$ thin films as insulator of metal–ferroelectric–insulator–semiconductor (MFIS) structures*

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$SrTiO_3$ (STO) thin films were deposited on p-Si(100) substrates at various substrate temperatures from 300°C to 700°C by radio frequency (RF) magnetron sputtering technique. Their structure and electrical properties were investigated. It was found that the transition from amorphous phase to polycrystalline phase occurred at the substrate temperatures 300–400°C. Their crystallinity became better when the substrate temperatures further increased. The dielectric and leakage current measurements were carried out by using the Si/STO/Pt metal–insulator–semiconductor (MIS) structures at room temperature. It was found that the fixed charge density decreased and both the interface trap density and the dielectric constant increased when the substrate temperatures were increased. The leakage current mechanisms for STO MIS structures with STO films prepared at 700°C followed the space charge limited current (SCLC) under the low applied electric field and the Poole–Frenkel emission under the high one. In addition, the resistivity for films prepared at 700°C was higher than $10^{11}\Omega\cdot$cm under the voltage lower than 10V (corresponding to the electric field of 1.54×10^3kV$\cdot$cm^{-1}). It suggested that the STO films prepared at 700°C were suitable for acting as the insulator of metal–ferroelectric–insulator–semiconductor (MFIS) structures.

Keywords: substrate temperatures, RF magnetron sputtering, electrical properties, $SrTiO_3$ thin films
PACC: 8140G, 8115, 7360, 7360H

1. Introduction

In recent years, non-volatile ferroelectric memory devices (NVFEMD) have been widely researched. These devices are composed of only one transistor using ferroelectric thin films as gate oxides, i.e. metal–ferroelectric–semiconductor field-effect-transistor (MFSFET), to realize the nondestructive read operation. However, preparation of ferroelectric/Si structures with good interface is difficult because of the chemical reaction of Si and ferroelectric materials. Particularly, it is well known that ferroelectric $Pb(Zr,Ti)O_3$ (PZT) thin films easily react with Si and interdiffusion of Pb and Si at the PZT/Si interface occurs even at temperatures as low as 500°C.[1]

One of the possible methods to prevent the reaction and interdiffusion is the use of an intermediate layer such as CeO_2,[2] TiO_2,[3] Ta_2O_5,[4] Si_3N_4,[5] and $SrTiO_3$ (STO)[6] between the ferroelectric thin film and Si substrate; this is known as the metal–ferroelectric–insulator–semiconductor field-effect-transistor (MFIS FET) technique. As the insulator of MFIS structures, it should have a large dielectric constant to decrease the operation voltage of memories,[7] easily grow on Si substrate with good insulator/Si interface, and favour the growth of ferroelectric film on it. Among the aforementioned materials, STO is looked very promising. It is an incipient ferroelectric with a transition temperature near 108K. At room temperature, this material exhibits paraelec-

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tric behaviour. The dielectric constant of STO bulk single crystal is as large as 300,[8] so that one can apply the large enough voltage to reverse the polarization of ferroelectric films. The lattice constant of STO (~0.3905nm) favours its epitaxial growth on Si(100) with the STO unit cell rotated 45°.[9] In addition, STO provides a good lattice match to most materials with perovskite structure, which makes the ferroelectric films such as PZT easily grow on it.

Many studies have been performed on the deposition of STO films by RF magnetron sputtering,[6] multi-ion-beam reactive sputtering,[10] metalorganic solution deposition,[11] sol–gel,[12] and pulsed laser deposition.[13] The RF magnetron sputtering technique is one of most popular methods for preparing films. It is well known that the structure and electrical properties of films strongly depend on the growth conditions, such as substrate temperature. However, few articles reported the effect of various substrate temperatures on the structural and electric properties for STO thin films as insulator of MFIS structures prepared by RF magnetron sputtering. In the present work, we report the preparation of STO thin films deposited on p-Si(100) substrates with various substrate temperatures from 300°C to 700°C by RF magnetron sputtering technique. Their structure and electrical properties were investigated. It suggests that the films prepared at the substrate temperature of 700°C are suitable for acting as the insulator of MFIS structures. In this paper, we especially studied the leakage current mechanisms of STO films in MIS structures. It was found that the leakage current mechanisms followed the space charge limited current (SCLC) under the low electric field and the Poole–Frenkel emission under the high one.

2. Experimental

The p-Si(100) wafers (resistivity ρ ~6–8Ω·cm, corresponding to the doping concentration of $2\times10^{15}cm^{-3}$) were used as the substrates. Surface native oxide layers were removed by dipping in buffered HF solution, rinsing in de-ionized water and blowing dry with N_2 gas right before loading into the deposition chamber. The STO films were grown on p-Si(100) substrates by RF magnetron sputtering technique. A stoichiometric ceramic target with the diameter of 100 mm was used for deposition. The vacuum chamber was pumped by a turbo-molecular pump, resulting in a base pressure of 6.5×10^{-4}Pa. The distance between the target and the substrates was about 90mm. The sputtering took place in plasma containing Ar and O_2 with a ratio of 3:1 and a total pressure of 1.6Pa under total output power of 50W, yielding a growth rate of approximately 0.4nm/min. Before deposition, the target was pre-sputtered for 30min with the substrate shutter closed to achieve stable conditions. During the sputtering, the substrate temperatures were kept at 300°C, 400°C, 500°C, 600°C and 700°C respectively. Typically, the deposition lasted for 3h to obtain the desired thickness of 65nm.

The structure of the STO films was analysed by D/MAX-RA x-ray diffraction (XRD) using a Ni-filtered Cu Kα radiation source. The infrared transmittance spectra were studied by a Fourier transformed infrared (FTIR) spectroscopy (IFS 113V) using a bare Si wafer as the reference. The electric measurements were performed on the films in Pt/STO/Si/Pt MIS configurations. The top electrodes with area of $4\times10^{-4}cm^2$ were fabricated by sputtering Pt through a photoresist lift-off mask. The backside of Si substrates was strongly doped by B^+ to form the ohmic contact with the ion implanting energy and concentration of 50keV and $5\times10^{15}cm^{-2}$, followed by sputtering Pt bottom electrode on it. The capacitance–voltage ($C-V$), current-time ($I-t$), and current density–voltage ($J-V$) characteristics were measured by using a HP4194A impedance analyser and a Keithley 617 programmable electrometer with a metal-shielded sample box. The chemical compositions and depth profiles for the films in the Si/STO structures were studied by Auger electron spectroscopy (AES, Microlab 310F). The thickness of films was observed by using a field-emission scanning electron microscopy (SEM, Philips S360). All the measurements were conducted at room temperature.

3. Results and discussion

Figure 1 displays the XRD patterns of STO films on p-Si(100) as a function of substrate temperatures from 300°C to 700°C. The film prepared at substrate temperature of 300°C is amorphous. When the substrate temperature is up to 400°C, a slight (110) diffraction peak emerges, indicating that the transition from amorphous phase to polycrystalline phase occurs at the temperatures of 300–400°C. As the substrate temperatures further increase, the diffraction peaks become sharp and the full width at half maximum (FWHM) decreases, indicating better crystallinity and an increase in grain size with the in-

creasing substrate temperatures. All the diffraction peaks are assigned to the cubic perovskite structure. The lattice constants calculated from the diffraction peaks were found to be $a = b = c$=0.393nm, which are in good agreement with the data prepared by sol–gel[12] and pulsed laser deposition.[13] From Fig.1, it can also be observed that the relative diffraction intensity of (200) peak gradually increases with the increasing substrate temperatures. Especially, the films deposited at 700°C display highly (200) preferential orientation. It suggests that the high substrate temperatures favour the growth of (200) orientation. Since STO can provide a good lattice match to Si(100) substrate (a_{Si}=0.543nm) with its unit cell rotated 45° (a_{STO}=0.393nm, $\sqrt{2}a_{STO}$=0.556nm in present case).[9] In addition, the nucleation speed is generally fast at the high temperature. Therefore, it is easy to understand that the films deposited at 700°C can epitaxially grow on Si(100) substrates, this fact displayed highly (200) preferential orientation.

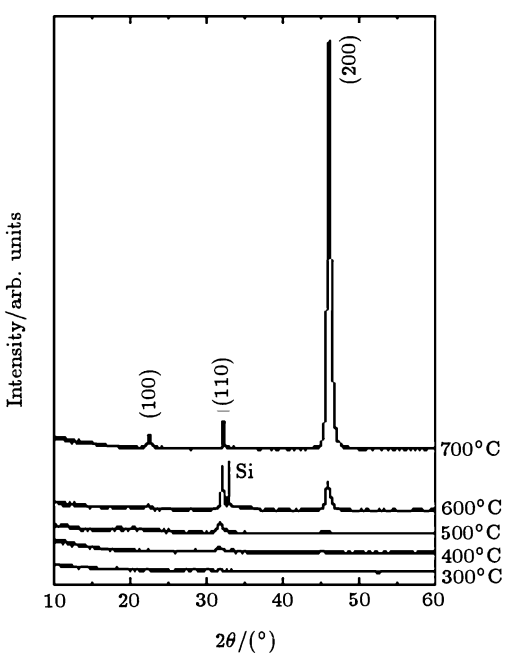


Fig.1. XRD patterns of STO films prepared at various substrate temperatures.

Figure 2 shows the FTIR transmittance spectra of STO thin films on p-Si(100) substrates prepared at various substrate temperatures with a bare Si wafer as the reference. It can be seen that with the increase of the substrate temperatures a clear absorption peak around 550cm^{-1} emerges, which is assigned to the characteristic peak of TiO_6 octahedron. For the film prepared at 300°C, this peak cannot be observed. When the substrate temperature is up to 400°C, this peak emerges with relatively weak absorption intensity. As the substrate temperatures further increase, this absorption peak becomes more and more strong, this fact indicates that the crystallinity becomes better at the high substrate temperature. The FTIR measurements also suggest that the phase transition from amorphous to crystalline occurs at the substrate temperatures 300–400°C, which agrees with the XRD results.

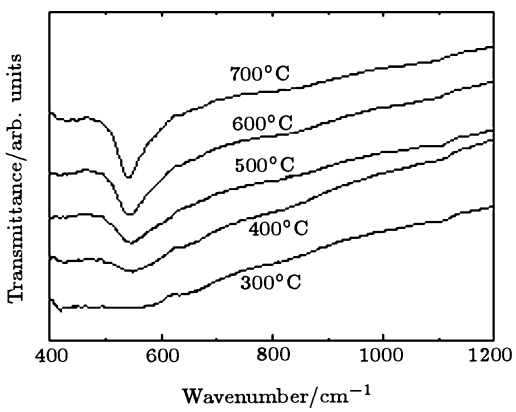


Fig.2. FTIR transmittance spectra of STO films prepared at various substrate temperatures.

Figure 3 shows the $C-V$ plots of STO MIS structures for STO films prepared at various substrate temperatures. The measurements were conducted from –6V to +6V (named as up sweep) and then swept back (named as down sweep) at the frequency of 1MHz. The regions of accumulation, depletion and inversion are clearly shown, which verified a typical MIS behaviour. The thickness of all the films is about 65nm, observed by SEM cross-sectional images. According to semiconductor theory,[14] the capacitance in the $C-V$ accumulation region is almost that of the insulator for MIS structure under high-frequency measurement. By using the capacitance values in the accumulation region, the dielectric constant of films was calculated. The fixed charge density N_f and the interface trap density D_{it} in Si/STO structures were also estimated from the flat-band voltage and the slope of the $C-V$ characteristics,[15] respectively. The calculated results were listed in Table 1. It can be seen that with the increase of the substrate temperatures the dielectric constant increases from 18 to 44 and the fixed charge density decreases from 1.4×10^{12} to 1.9×10^{11} cm^{-2}, which are mainly due to the better crystallinity at higher temperature. However, the interface trap density increases from 2.5×10^{12} to 8.4×10^{12}cm$^{-2}\cdot$eV^{-1} with the increase of the substrate temperatures. Since

a higher deposition temperature can easily lead to a higher interface trap density,[15] it is reasonable for the aforementioned result. It can also be seen in Fig.3 that the $C-V$ curves for the samples prepared at 300–600°C display hysteresis behaviour, which probably originates from the movement of mobile ions in the films[16] and/or the charges injection through the STO/Si interface under the applied voltage.[3] However, there is no such hysteresis behaviour for the samples prepared at 700°C, which indicates that the STO films prepared at 700°C would be appropriate as the insulator of MFIS structures. Therefore, we will mainly study the electric properties of STO films prepared at 700°C in the following.

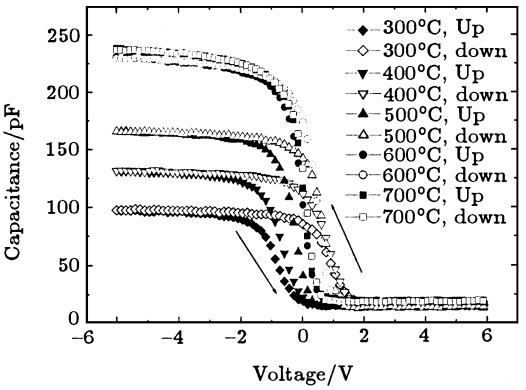


Fig.3. Capacitance–voltage ($C-V$) plots for STO MIS structures with STO films prepared at various substrate temperatures. The filled and empty symbols correspond to the up-sweep and the down-sweep respectively.

Table 1. Dielectric constant, fixed charge density N_f and interface trap density D_{it} calculated from $C-V$ curves for STO MIS structures with STO films prepared at various substrate temperatures.

Substrate temperature/°C	300	400	500	600	700
Dielectric constant at 1MHz	18	24	30	42	44
N_f/cm^{-2}	1.4×10^{12}	1.4×10^{12}	8.8×10^{11}	2.3×10^{11}	1.9×10^{11}
$D_{it}/cm^{-2}\cdot eV^{-1}$	2.5×10^{12}	3.2×10^{12}	5.3×10^{12}	6.6×10^{12}	8.4×10^{12}

Figure 4 shows the dielectric constant and the dissipation factor as functions of frequency under a negative voltage bias for STO MIS structures with STO films prepared at 700°C, which were obtained when the surface of the silicon was in the accumulation region. The dielectric constant decreases slightly with the increasing frequency, while the dissipation factor shows the opposite tendency. Both of them do not display distinguished change up to 1MHz, which indicates good quality of the present films. When the frequency further increase, there is a sharp variation of a decrease in the dielectric constant and an increase in the dissipation factor. Such variation is not related to the materials properties, which may be due to the resonance of an electrical equivalent circuit composed of the stray inductance of the contents and wires and capacitance of the sample under test.[17] The typical values of the measured dielectric constant and dissipation factor at 100kHz are about 42 and 0.01 respectively. However, the value of dielectric constant is much smaller than that for the bulk single crystal (~300).[8] It should be noted that the measured samples are polycrystalline films which are different from the bulk single crystal in structure. The dielectric constant of polycrystalline STO (~250) is smaller than that of single crystal.[8] In addition, there exists large stress in the films due to the difference in the thermal expansion coefficients between the substrates and the films, which may lead to small dielectric constant values.[18] There is another reason which may be related to an interface layer with small dielectric constant formed at the interface of Si/STO during the deposition process at 700°C. This interface layer is in series with the STO film, which results in small values of the equivalent dielectric constant.

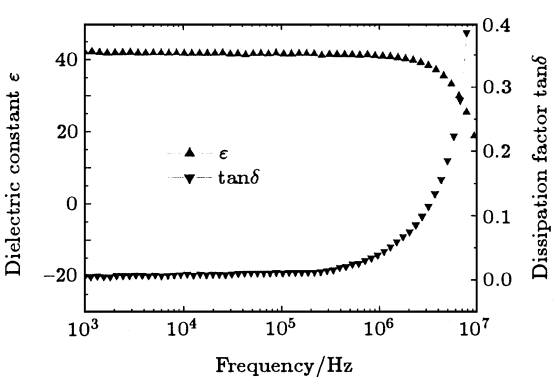


Fig.4. Dielectric constant and dissipation factor as functions of frequency under a negative voltage bias for STO MIS structures.

To further analyse the compositional and the interface properties in the Si/STO structures, AES depth profile for the samples prepared at 700°C was conducted and shown in Fig.5. It can be seen that Sr, Ti and O atoms are homogeneously distributed and

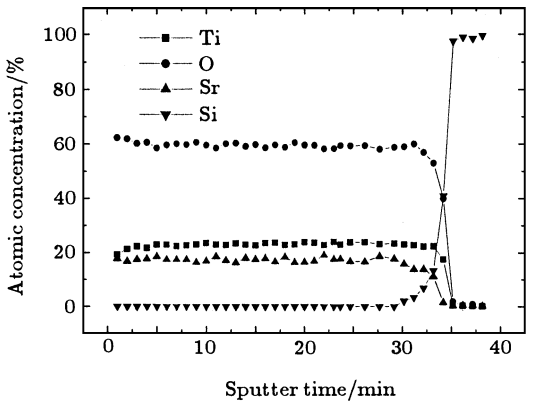


Fig.5. AES depth profiles for Si/STO structures.

satisfy the stoichiometric ratio within the experimental errors in the STO films. A relatively sharp interface can also be observed. The interface layer consists of Si, O, Sr and Ti atoms, due to the interdiffusion in the deposition process at high temperature. By measuring the capacitance values in the $C-V$ accumulation region for the films with different thickness, the intrinsic dielectric constant of STO films can be estimated.[19] STO and the interface layer are in series, following the relation

$$\frac{1}{C_{\rm I}} = \frac{1}{C_{\rm int}} + \frac{1}{C_{\rm STO}} = \frac{d_{\rm int}}{\varepsilon_0 \varepsilon_{\rm int} S} + \frac{d_{\rm I} - d_{\rm int}}{\varepsilon_0 \varepsilon_{\rm STO} S}. \qquad (1)$$

So,

$$\frac{\varepsilon_0 S}{C_{\rm I}} = \left(\frac{1}{\varepsilon_{\rm int}} - \frac{1}{\varepsilon_{\rm STO}}\right) d_{\rm int} + \frac{1}{\varepsilon_{\rm STO}} d_{\rm I}, \qquad (2)$$

where $d_{\rm int}$ and $d_{\rm I}$ are the thickness of interface layer and total thickness of the insulator respectively, $\varepsilon_{\rm STO}$ and $\varepsilon_{\rm int}$ are the dielectric constant of the intrinsic STO and the interface layer respectively, S is the area of Pt top electrode, ε_0 is the vacuum dielectric constant, $C_{\rm int}$ and $C_{\rm STO}$ are the capacitance of the interface layer and the intrinsic STO respectively, and $C_{\rm I}$ is the capacitance in the $C-V$ accumulation region. The $\frac{\varepsilon_0 S}{C_{\rm I}} \sim d_{\rm I}$ curve is shown in Fig.6. By fitting the experimental data into a line, the intrinsic dielectric constant of our resultant STO films is calculated to be about 77. Although the interface layer cannot be described by using a definite molecular formula, its thickness can be estimated by the intercept on the vertical axis. If this interface layer is simply assumed as SiO_2 (dielectric constant ~3.9), the estimated thickness is about 2.6nm.

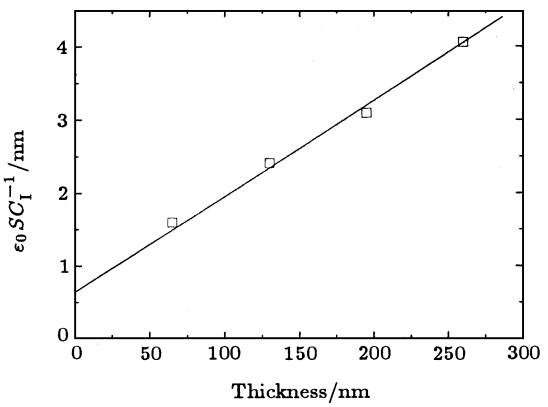


Fig.6. Variation of $\frac{\varepsilon_0 S}{C_{\rm I}}$ with the thickness of the insulator for STO MIS structures.

The leakage current is one of the important characteristics to evaluate the insulator films. Figure 7 shows the $I-t$ relation under an applied voltage of 5V for the STO MIS structures with STO prepared at 700°C. It can be seen that the current decreases exponentially with time and finally reaches a saturated steady-state value. In general, the total current roughly consists of three parts, $I = I_{\rm c} + I_{\rm a} + I_{\rm l}$, as schematized in Fig.7. The first part $I_{\rm c}$, the charging current originating from the electrode system and the quick polarization of dielectric materials, would disappear quickly. The second part $I_{\rm a}$ is the relaxation current, which decreases slowly with time. The last part $I_{\rm l}$ is the leakage current, which retains a saturated steady-state value and does not change with further delaying time. The current would reach a steady-state value when the measuring time adequately long. It is the leakage current which is interesting for insulation properties. Figure 7 shows that the measured current is almost the leakage current after about 3min. Therefore, in the following measurements, the values recorded after 3min under the applied voltage was selected as the leakage current.

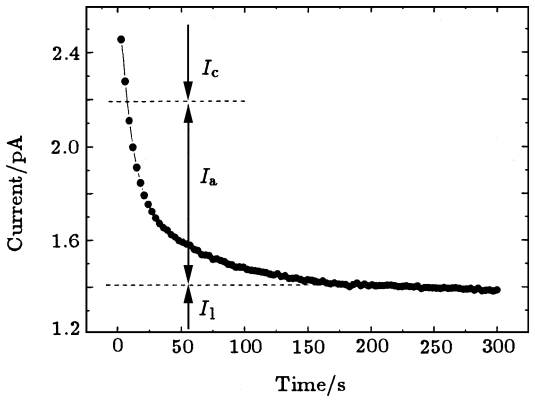


Fig.7. Current–time ($I-t$) measurement under an applied voltage of 5V for STO MIS structures.

Figure 8 shows the $J-V$ characteristic for STO MIS structures with STO films prepared at 700°C. The applied voltage increased from 0V to 10V with a step of 0.2V following a stair-like voltage. The leakage currents were recorded after retaining the measuring voltage for 3min. The leakage current density J is

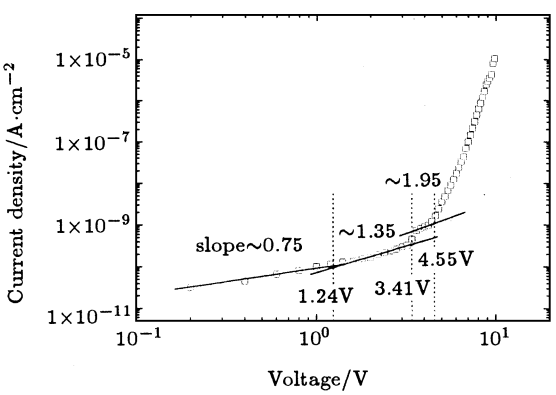


Fig.8. Current density–voltage ($J-V$) characteristics for the samples of Fig.7.

calculated by $J=I/S$, where S is the electrode area. When the voltage is lower than 1.24V, the experimental data can be fitted into a line with a slope of about 0.75. When the voltage increased, the leakage current density increased following a line whose slope is about 1.35 in the range of 1.24–3.41V. When the voltage further increased, the leakage current density increased quickly and reached another increasing line with a slope of about 1.95 until the voltage of 4.55V. It is proposed that the leakage current mechanism follows the SCLC in the low voltage range ($<$ 4.55V). According to SCLC theory,[20] the ohmic mode occurs in insulator film as long as the bulk generated current in the film exceeds the current due to injected free carriers from the electrode. As the applied voltage increases, a strong injection of the charge carriers in the bulk of the film takes place, a square law region appears. For strong injection, the traps in the films filled up and a space charge appears. As the applied voltage increases further, very strong injection of charge carries takes place, all the traps in film will become filled, a second square law region will appear. Therefore, the voltage ranges of 0–1.24V, 1.24–3.41V and 3.41–4.55V correspond to the ohmic, the first and the second square law region, respectively. However, according to the SCLC theory the theoretical values of slope are 1 and 2 in the ohmic region and the square law region respectively. It should be pointed out that the samples measured in our experiments are MIS structures. For MIS structures, when measured under the low voltage, the $C-V$ curves lie in the depletion region (see Fig.3). In this case, the total voltage applies onto the series of the insulator film and the space charge layer of Si surface.[14] Therefore, the voltage applied onto the STO films was only one part of the total voltage, which resulted in the slope with smaller values than the theoretical ones. When the voltage increased, the $C-V$ curves gradually entered into the inversion region, where the total voltage mainly applied onto the insulator layer.[14] The slope 1.95 in the second square law region is very near to the theoretical value 2. Therefore, it is reasonable to draw the conclusion that when the voltage is lower than 4.55V the leakage current mechanism follows SCLC.

From Fig.8, it can also be observed that when the applied voltage was higher than 4.55V the leakage current density increased sharply and the $J-V$ curve displayed a high power law region. This may be due to some type of electron emission. To further analyse the leakage current in this region $\lg J-\sqrt{V}$ was plotted in Fig.9. In the high voltage range ($>$ 4.55V), $\lg J-\sqrt{V}$ can be fitted to a straight line; this fact indicates that the leakage current follows the Schottky emission or

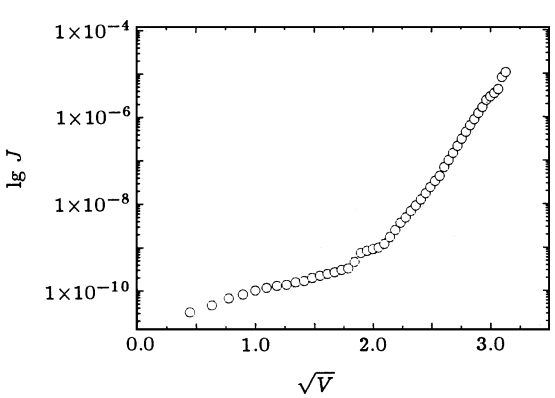


Fig.9. $\lg J-\sqrt{V}$ plot for the samples of Fig.7.

the Poole–Frenkel emission. The current density for both conduction mechanisms can be expressed as[10]

$$J \propto \exp\left(\frac{\beta E^{1/2} - V_{\rm g}}{kT}\right), \tag{3}$$

where

$$\beta = \left(\frac{e^3}{\alpha\pi\varepsilon_0 K_\infty}\right)^{1/2}, \tag{4}$$

$V_{\rm g}$ is the energy interval between the trap level and the bottom of the conduction band in case of Poole–Frenkel emission, or the work function difference between the film and electrode in case of Schottky emission, k is the Boltzmann's constant, T is the temperature in K, e is the electronic charge, ε_0 is the permittivity in vacuum, K_∞ is the high-frequency dielectric constant ($=n^2$, where n is refractive index), and α is a constant whose value equals to 1 or 4 for Poole–Frenkel or Schottky emission respectively. The actually measured β is $\sim 4.67\times10^{-5}$ from Fig.9, while the theoretical value is $\sim 3.8\times10^{-5}$ for Poole–Frenkel emission and $\sim 1.9\times10^{-5}\mathrm{eV\cdot m^{\frac{1}{2}}\cdot V^{-\frac{1}{2}}}$ for Schottky emission by assuming the refractive index n of the film to be ~2.0, which may be reasonable for a film composed of STO (n ~2.4) and some voids. By comparing the values of both measured and estimated β, it may be realized that the conduction in high field region is consistent with the Poole–Frenkel emission mechanism.

The resistivity can be calculated by using the relation[21]

$$\rho = \frac{V}{Jd}, \tag{4}$$

where d is the film thickness. When the voltage increases, the resistivity changes smoothly at first and then sharply decreases, as shown in Fig.10. However,

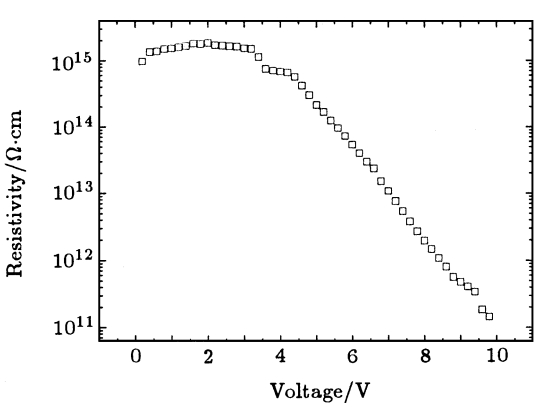


Fig.10. Resistivity–voltage (ρ-V) characteristics for the samples of Fig.7.

all the resistivity is found to be higher than $10^{11}\Omega\cdot$cm under the voltage lower than 10V (corresponding to the electric field of $1.54\times10^3\mathrm{kV\cdot cm^{-1}}$), which indicates that the STO films prepared at 700°C have excellent insulation properties and are appropriate as the insulator of MFIS structures. To further verify it, a preliminary experimental result for MFIS structures is shown in Fig.11. The ferroelectric PZT(52/48) films with thickness 300nm were grown onto STO coated p-Si substrates by RF magnetron sputtering technique. The $C-V$ curves of Si/STO/PZT/Pt MFIS structures displayed a clockwise hysteresis loop with a memory window of 2.6V when the voltage swept from −6V to +6V and then swept back, which originated from the ferroelectric polarization. These results suggested that the films prepared at the substrate temperature of 700°C could be used as the insulator of MFIS structures. Further research on MFIS structures is in progress.

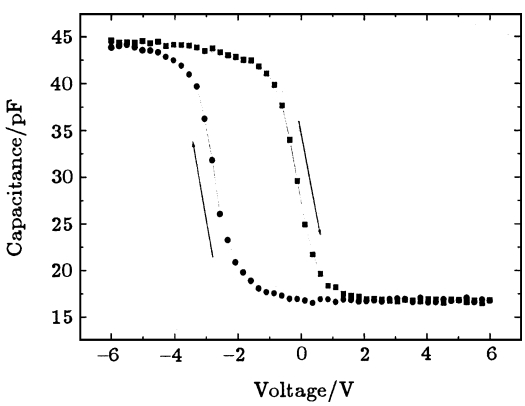


Fig.11. A preliminary $C-V$ result for Pt/PZT/STO/Si MFIS structures.

4. Conclusion

In summary, STO thin films were deposited on p-Si(100) substrates at various substrate temperatures from 300°C to 700°C by RF magnetron sputtering technique. Their structure and electrical properties have been investigated. It was found that the transition from amorphous phase to polycrystalline phase occurred at the substrate temperatures 300–400°C. When the substrate temperatures further increase, the crystallinity of STO thin films become better. Their lattice constants were found to be $a = b = c$=0.393nm. The electric measurements were carried out by using the Si/STO/Pt MIS structures at room temperature. The $C-V$ measurements showed that the fixed charge density decreased and both the interface trap density

and the dielectric constant increased with the increasing substrate temperatures. Only the films prepared at 700°C did not display the $C-V$ hysteresis behaviour. The AES depth profile of the films prepared at 700°C showed a clear and sharp interface between STO films and Si substrates. The $J-V$ measurements for the films prepared at 700°C showed that the leakage current mechanisms followed the SCLC in the low applied voltage range (<4.55V) and the Poole–Frenkel emission in the high one (>4.55V). In addition, the resistivity was higher than $10^{11}\Omega\cdot$cm under the voltage lower than 10V (corresponding to the electric field of 1.54×10^3kV·cm^{-1}). As one preliminary experimental result, the $C-V$ curves of Si/STO/PZT/Pt MFIS structures displayed a memory window of 2.6V when the voltage swept from –6V to +6V and then swept back. These results suggested that the films prepared at 700°C were suitable for acting as the insulator of MFIS structures.

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