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Analysis of the effect of sidewall on the performance of 6H-SiC Schottky barrier source/drain NMOSFETs*

Tang Xiao-Yan(汤晓燕)†, Zhang Yi-Men(张义门),
Zhang Yu-Ming(张玉明), and Gao Jin-Xia(郜锦侠)

Microelectronics Institute, Xidian University, Xi'an 710071, *China*

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Between source/drain and gate of SiC Schottky barrier source/drain MOSFET (SiC SBSD-MOSFET), there must be a sidewall as isolation. The width of sidewall strongly affects on the device performance. In this paper the effect of sidewall on the performance of 6H-SiC SBSD-NMOSFET is simulated with the 2D simulator MEDICI. The simulated results show that a sidewall with width less than 0.1μm slightly affects the device performance. However, when the width of sidewall exceeds 0.1μm, the conduction does not occur until the drain voltage is high enough and saturation current sharply decreases. The effect of the sidewall on device performance can be reduced by decreasing the doping concentration in the epitaxial layer.

Keywords: 6H-SiC, Schottky contact, sidewall, MOSFET
PACC: 7280, 7330, 7340S, 7220

1. Introduction

SiC Schottky barrier source/drain MOSFETs (SiC SBSD-MOSFET) which utilize metal replacing heavily doped SiC within the source/drain regions is a novel SiC device. Compared with conventional MOSFETs, the fabrication process for this kind of device is quite simple, avoiding the steps of ion implantation and annealing at extremely high temperature. Also, it has none of the problems of crystal damage caused by ion implantation and low activation rate of implanted atoms. Both the simple process and lack of crystal damage could facilitate the development of SiC SBSB-MOSFETs,[1−3] but there has been no paper about SiC SBSD-MOSFET fabrication so far.

The SBSD and the conventional MOSFET have very different physical behaviour. Carrier entering into the conduction channel from the source contact takes place mainly by tunnelling through the reverse-biased Schottky barrier at the SiC/metal interface. The width of the Schottky barrier is modulated by the gate voltage, and conduction occurs when the barrier is sufficiently thin.[4] The barrier between source and channel is sufficiently wide when the gate voltage is small so that relatively little tunnelling takes place. For higher gate voltage the Schottky barrier underneath the oxide interface may become sufficiently narrow to allow larger tunnelling current.

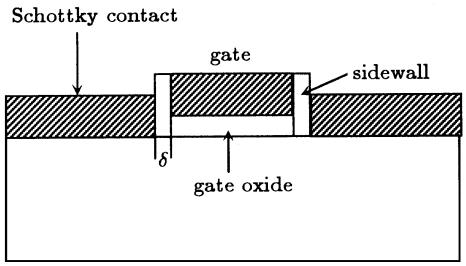


Fig.1. Schematic structure of SBSD-MOSFET.

Between the source/drain and gate of the SiC SBSD-MOSFET, there must be a sidewall as isolation for avoiding electrical short between the source/drain metal and gate (Fig.1). This may cause conduction problems in the channel below sidewalls, especially at the source side. The width of sidewall should be a reasonable compromise between isolation and channel conduction. So it is important to know how sidewalls affect device performance and determine appropriate

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†E-mail: xytang@mail.xidian.edu.cn

width before the device design and manufacture. In this paper the effect of sidewall on the performance of 6H-SiC SBSD-NMOSFET is simulated with the 2D numerical simulator MEDICI and the results are of practical significance for developing this kind of device.

2. Model

The primary function of MEDICI is to solve the three basic equations, Poisson's equation and continuity equations for electrons and holes, self-consistently for the electrostatic potential and for the electron and hole concentrations, respectively.[5] Different models should be chosen for different material and structure. The Schottky contact model is chosen for the special structure and an incomplete ionization model used for the incomplete ionization of SiC material.

In MEDICI the Schottky contacts to semiconductor are defined by a work function of the electrode metal ($W_{\rm m}$) and an optional surface recombination velocity. The surface potential at a Schottky contact is defined by

$$\Psi_{\rm s} = \chi_{\rm s} + \frac{E_{\rm g}}{2q} + \frac{k_{\rm B}T}{2q}\ln\left(\frac{N_{\rm c}}{N_{\rm v}}\right) - W_{\rm m} + V_{\rm applied}, \quad (1)$$

where $\chi_{\rm s}$ is the electron affinity of the semiconductor, and $E_{\rm g}$ the energy bandgap. $N_{\rm c}$ and $N_{\rm v}$ are conduction and valance band effective state density respectively. $V_{\rm applied}$ is applied bias at the electrode, $k_{\rm B}$ is the Boltzmann constant.

The electron and hole current densities at the contact are expressed as follows:

$$\begin{aligned} J_{\rm surfn} &= qv_{\rm sn}\left(n_{\rm surf} - n_{\rm eq}\right), \\ J_{\rm surfp} &= qv_{\rm sp}\left(p_{\rm surf} - p_{\rm eq}\right), \end{aligned} \quad (2)$$

$$v_{\rm surfn} = \frac{A_{\rm n}^* T^2}{qN_{\rm c}}, \qquad v_{\rm surfp} = \frac{A_{\rm p}^* T^2}{qN_{\rm v}}, \quad (3)$$

where $v_{\rm surfn}$ and $v_{\rm surfp}$ are the surface recombination velocities for electrons and holes, $n_{\rm surf}$ and $p_{\rm surf}$ are the actual surface electron and hole densities, and $n_{\rm eq}$ and $p_{\rm eq}$ are the equilibrium electron and hole densities respectively. $A_{\rm n}^*$ and $A_{\rm p}^*$ are the effective Richardson constants for electrons and holes, respectively, considering quantum mechanical reflection and tunnelling.

The Schottky model can also account for field-dependent barrier-lowering mechanisms:

$$\Delta\Phi_{\rm b} = \left[\frac{q}{4\pi\varepsilon_{\rm SiC}}\right]^{1/2} E^{1/2} + \alpha E, \quad (4)$$

where E is the magnitude of the electric field at the interface and $\varepsilon_{\rm SiC}$ dielectric constant of SiC. α is an empirical coefficient, and its value ranges from 1.5nm to 3.5nm:[6,7] 1.5nm is adopted in this paper. Note that the term with the square root dependence on the electric field corresponds to an image force, while the linear term corresponds to the dipole effect. The basic procedure is to solve Poisson's equation normally with the surface potential defined as in Eq.(1). However, using the electric field consistent with the solved potentials, the effective surface potential can be computed as

$$\Psi_{\rm seff} = \Psi_{\rm s} \pm \Delta\Phi_{\rm b}, \quad (5)$$

where the sign '+' is for electrons and the sign '–' for holes. The continuity equations are then solved using Eqs.(2) and (3) as boundary conditions, but with $n_{\rm surf}$, $p_{\rm surf}$, $n_{\rm eq}$ and $p_{\rm eq}$ replaced by the corresponding effective values which are computed using $\Psi_{\rm seff}$.

3. Results and discussion

A 6H-SiC SBSD-NMOSFET has been simulated with 1.5μm channel length, 20nm oxide thickness and an acceptor concentration ($N_{\rm A}$) of $5\times10^{16}{\rm cm}^{-3}$. The work function of metal is 3.9eV.

Figures 2 and 3 show the effect of sidewalls with various widths on the device performance at room temperature. The data show that saturation current and transconductance of the device slightly decrease for the width of sidewall (sidewall) less than 0.1μm. When sidewall width exceeds 0.1μm the device could not turn on normally, while saturation current sharply decreases. Saturation current is only less than 1μA/μm for sidewall=0.3μm.

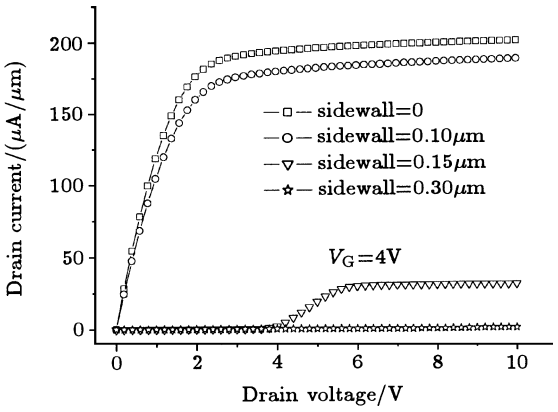


Fig.2. Output characteristics with gate voltage ($V_{\rm G}$) of 4V for various widths of sidewalls.

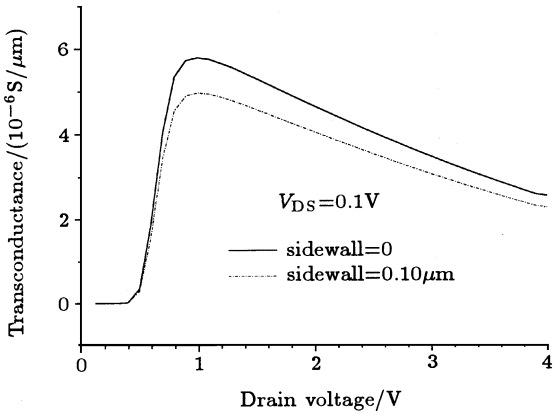


Fig.3. Transconductance versus gate voltage of SBSD-NMOSFET with drain voltage (V_{DS}) of 0.1V for various widths of sidewalls.

There may exist a p–n junction under the sidewall, composed of n-type channel and p-type epitaxial layer. The conduction of the channel below the sidewall can be achieved by expansion of the p–n junction and Schottky barrier space-charge region. The widths of p–n junction and Schottky barrier space-charge region are given by Eqs.(6) and (7), respectively:

$$x_{p-n} = \sqrt{(V_D - V)\frac{2\varepsilon_{SiC}}{q}\left(\frac{1}{n} + \frac{1}{N_A}\right)}, \qquad (6)$$

$$x_S = \left[\frac{2\varepsilon_{SiC}\,|V_b - V|}{qN_A}\right]^{\frac{1}{2}}, \qquad (7)$$

where V_D and V_b are the built-in potential of p–n junction and Schottky barrier, respectively, and n is electron concentration in n-type channel. V is applied bias. For n-channel MOSFET the source is at low potential, and p–n junction and Schottky barrier at source side are reverse-biased ($V < 0$). Thus space-charge regions widen with the increase of drain voltage. This can explain why the conduction does not occur until drain voltage is high enough when the width of sidewall exceeds 0.1μm.

Figure 4 shows the output characteristics of the device for sidewall=0.15μm. The curves show that the higher gate voltage is, the higher the drain voltage needed to conduct channel. This can be explained by electron concentration increasing exponentially with gate voltage so that the space-charge region of the p–n junction becomes narrow at higher gate voltage.

Figure 5 shows the output characteristics of the device with sidewall=0.15μm, V_G=3V for various doping concentration. The lower the doping concentration, the wider the space-charge regions should be by Eqs.(6) and (7). So the effect of sidewall on device performance may be reduced by decrease of the doping.

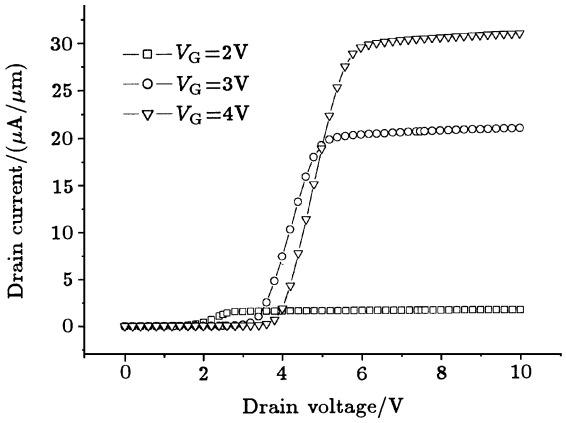


Fig.4. Output characteristics with sidewall=0.15μm for various V_G.

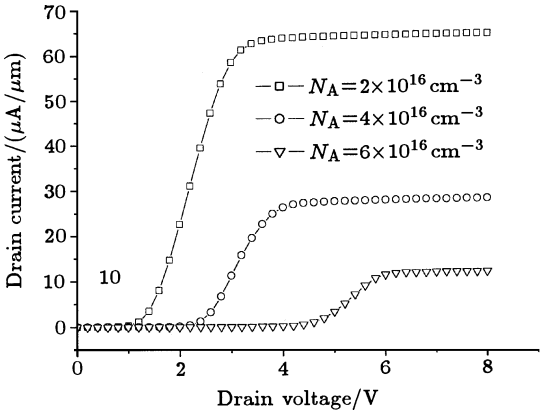


Fig.5. Output characteristics with sidewall=0.15μm and V_G=3V for various doping concentration.

4. Conclusion

Between the source/drain and gate of SiC SBSD-MOSFETs that utilize metal replacing heavily doped SiC with the source/drain regions, there must be a sidewall as isolation. The width of sidewall strongly affects the device performance. The effect of sidewall on the performance of 6H-SiC SBSD-NMOSFET is simulated with a 2D numerical simulator MEDICI. The simulated results show that saturation current and transconductance of the device slightly decrease for the width of sidewall less than 0.1μm. When the width of sidewall exceeds 0.1μm, the conduction does not occur until the drain voltage is high enough, and the saturation current sharply decreases. The effect of the sidewall on device performance can be reduced by decreasing the doping concentration in the epitaxial layer. These results should be of practical significance for device design and fabrication.

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