Vol 13 No 7, July 2004
1009-1963/2004/13(07)/1104-06

Chinese Physics

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A compact I–V model for lightly-doped-drain MOSFETs*

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(Received 4 June 2003; revised manuscript received 1 March 2004)

A novel model for lightly-doped-drain (LDD) MOSFETs is proposed, which utilizes the empirical hyperbolic tangent function to describe the I–V characteristics. The model includes the strong inversion and subthreshold mechanism, and shows a good prediction for submicron LDD MOSFET. Moreover, the model requires low computation time consumption and is suitable for design of MOSFETs devices and circuits.

Keywords: lightly-doped-drain MOSFET, hot carrier effect, velocity saturation, hyperbolic tangent
PACC: 7220, 7230

1. Introduction

It is well known that the hot carrier effect has a significant impact on submicron and deep-submicron scaling down of metal–oxide–semiconductor field-effect transistors (MOSFET). The lightly-doped-drain (LDD) presents an effective structure to improve the hot carrier immunity of MOSFET. However, the parasitic series resistance and parasitic capacitance caused by the lightly doped source/drain (S/D) region can reduce the drain current driving ability and the high frequency performance. The features of channel length modulation (CLM), drain-induced barrier lowering (DIBL), velocity saturation, etc, are of some difference from the features in conventional short-channel devices, thus increasing the complexity of the MOSFET modelling. Most of the recent papers have focused on extraction techniques of the parameters that include series resistance $R_{\rm ds}$, effective channel length $L_{\rm eff}$, effective channel mobility $\mu_{\rm eff}$, threshold voltage $V_{\rm th}$, velocity saturation region length $l_{\rm d}$, etc, in order to improve the model accuracy for LDD MOSFET.[1–5] Fitting parameters lacking physical descriptions were adopted inevitably. Two-dimensional (2D) numerical simulations were also adopted in some papers. The technique was generally used for the device analysis not for circuit level design because of high computation cost.

In this paper, we propose a novel model which is based on velocity saturation theory and combined with a concise hyperbolic-tangent description for intrinsic I–V characteristics of scaling MOSFET. The parasitic resistance due to the lightly doped region is treated as an external parameter. The drain current $I_{\rm ds}$ is obtained by an iteration process. The smooth transition between linear region and saturation region is guaranteed by $\tanh(x)$ description, avoiding the discontinuity of drain conductance $g_{\rm ds}$. Furthermore, the subthreshold mechanism is also involved in the model.

2. Modelling of intrinsic I–V characteristics for LDD nMOSFET

Figure 1 shows the LDD n-channel MOSFET cross section with intrinsic and extrinsic construction. Of the methodology of device analysis, the equivalent-circuit-based short-channel MOS model is widely used due to its clear description of the device mechanism. In this work, the emphasis is put on the analysis of intrinsic short-channel MOSFET with the series resistance treated as an external parasitic parameter. Although the LDD structure reduces the lateral electric field, especially at the fringe of drain n^+ ohmic contact region, it shortens the length of the channel, making it easy for carriers to reach a saturated ve-

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locity. So it is reasonable to characterize the LDD MOSFET with the theory of velocity saturation. Here we develop a novel model which was successfully used in modelling of submicron MESFET.[6] It utilizes a hyperbolic-tangent function to describe the nonlinear current $I_{ds}(V_{gs}, V_{ds})$, given by

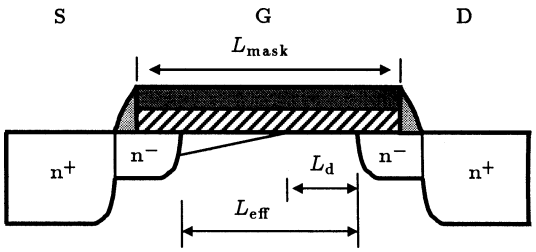


Fig.1. Cross section of LDD n-channel MOSFET.

$$I_{ds}(V_{gs}, V_{ds}) = I_{dsat}(1 + \lambda V_{ds})\text{th}(\alpha V_{ds}), \qquad (1)$$

where I_{dsat} is the critical saturation drain current under different gate-source biases, α is the saturation voltage parameter, and λ is the channel length modulation parameter for short-channel modulation (SCM) effect. These parameters can be derived from the physics of the short-channel MOSFET, given as follows.

2.1. Analysis of the critical-saturated drain current I_{dsat}

According to the MOSFET theory of velocity saturation, I_{dsat} is given by [2]

$$I_{dsat} = W v_{sat} C_{ox}(V_{gs} - V_{th} - \gamma V_{dsat}), \qquad (2)$$

where v_{sat}, C_{ox}, V_{th}, γ and V_{dsat} are electron saturation velocity, oxide capacitance, threshold voltage, bulk charge factor, and saturation drain voltage, respectively.

First of all, we discuss the parameter V_{th} suitable for short n-channel MOSFET. There are various expressions for V_{th} in MOSFET modelling, physically and empirically. We use an improved model [7] with a few fitting parameters available, shown as follows:

$$V_{th} = V_{th0} - \frac{2\left[V_{ds} + V_{bi} + \sqrt{(V_{ds} + V_{bi})e^{(L_{eff}/l)}(V_{bi} - 2\phi_B)}\right]}{e^{(L_{eff}/l)}} \quad (L_{eff} > 5l), \qquad (3)$$

where V_{bi} is the built-in potential of the LDD region (n^-) / substrate (p) junction that has a lower value than a conventional S/D device. L_{eff} is the LDD effective channel length that will be discussed later, and l is the characteristic length, given by

$$l = \sqrt{\frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} x_j}. \qquad (3a)$$

Here we assume that the depletion junction depth x_{dep} equals the junction depth x_j, thus simplifying the computation. The long-channel threshold voltage V_{th0} is given as

$$V_{th0} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_0 \varepsilon_{Si} N_{sub}}}{C_{ox}}\sqrt{(2\phi_B + V_{sb})}. \qquad (4)$$

The flatband voltage V_{FB} and the Fermi potential ϕ_B in Eq.(4) are derived theoretically as

$$V_{FB} = \phi_m - (\chi + \tfrac{1}{2}E_g + \phi_B) - \frac{qN_{ss}}{C_{ox}}, \qquad (4a)$$

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right). \qquad (4b)$$

From Eq.(4), it is only required to evaluate the fixed oxide charge density N_{ss} or measure the V_{FB} directly. Other parameters related to the device structure are determined easily, therefore simplifying computations.

Secondly, the bulk charge factor γ in Eq.(2) is given by [8]

$$\gamma = 1 + \frac{\sqrt{2q\varepsilon_0 \varepsilon_{Si} N_{sub}}}{C_{ox}} \times \frac{0.5}{\sqrt{1 + 2\phi_B + V_{sb}}}. \qquad (5)$$

This is a simple empirical expression.

Thirdly, the critical saturation voltage V_{dsat} is derived with velocity saturation theory as [9]

$$V_{dsat} = L_{eff} E_c\left[\sqrt{1 + \frac{2(V_{gs} - V_{th})}{\gamma L_{eff} E_c}} - 1\right], \qquad (6)$$

where the effective channel length L_{eff}, indicating the actual channel length with lightly doped n^- region considered in LDD MOSFET, is given by [3]

$$L_{eff} = L_g - 2\sigma x_j. \qquad (6a)$$

As is well known, L_{eff} is gate bias-dependent. A strict description of this parameter will complicate the calculations for I–V modelling. Thus a concise expression shown in Eq.(6a) has been adopted widely in many papers with σ being extracted from measurement, which has a value of 0.7–0.75.[3] It is noted that

the different lightly-doped implant process (LDD or Large Angle Tilt Implanted Drain (LATID) process) causes a big difference of junction lateral diffusion, resulting in different values of σ which vary over a large range. In addition, the relation between critical electric field and carrier saturation velocity is shown to be

$$E_{\rm c} = v_{\rm sat}/\mu_{\rm s}. \tag{6b}$$

2.2. Analysis of saturation voltage parameter α

The parameter α indicates the transition of $I_{\rm ds}$ between linear region and saturation region, derived by Eq.(1):

$$\alpha = \frac{\left(\dfrac{\partial I_{\rm ds}}{\partial V_{\rm ds}}|_{V_{\rm ds}\to 0}\right)}{I_{\rm dsat}} = \frac{g_{\rm d0}(V_{\rm gs})|_{V_{\rm ds}\to 0}}{I_{\rm dsat}}, \tag{7}$$

where the linear region drain conductance $g_{\rm d0}$ is given by

$$g_{\rm d0} = \xi\frac{\mu_{\rm s}C_{\rm ox}W}{L_{\rm eff}}(V_{\rm gs} - V_{\rm th} - \gamma V_{\rm ds}), \quad (V_{\rm ds} < V_{\rm dsat}). \tag{7a}$$

It is derived from $\partial I_{\rm ds}/\partial V_{\rm ds}$ of SPICE MOS model LEVEL-3. When $V_{\rm ds} \to 0$, it has a satisfactory accuracy. With the fitting constant ξ, it can be used to describe the average conductance in the linear region (from $V_{\rm ds}$ =0 to $V_{\rm ds} = V_{\rm dsat}$) for short-channel MOSFET, thus simplifying the model computations.

It is noted that the mobility μ_s in Eqs.(6b) and (7a) should be replaced by the effective mobility $\mu_{\rm eff}$ to fit the real condition of devices:[5]

$$\mu_{\rm eff} = \frac{\mu_0}{1 + \theta(V_{\rm gs} - V_{\rm th})}, \tag{7b}$$

where the low-field mobility μ_0 (due to the vertical field) is extracted from measurement; θ is a fitting constant.

2.3. Analysis of channel length modulation parameter λ

This parameter illustrates the CLM effect on saturation region drain current in which the saturation region drain conductance $g_{\rm ds} > 0$ when $V_{\rm ds} > V_{\rm dsat}$. From Eq.(1), it is obtained that

$$\lambda = \frac{\left(\dfrac{\partial I_{\rm ds}}{\partial V_{\rm ds}}|_{V_{\rm ds}\geq V_{\rm dsat}}\right)}{I_{\rm dsat}} = \frac{g_{\rm ds}(V_{\rm gs}, V_{\rm ds})|_{V_{\rm ds}\geq V_{\rm dsat}}}{I_{\rm dsat}}, \tag{8}$$

where the saturation drain conductance $g_{\rm ds}$ is given by

$$g_{\rm ds} = \frac{I_{\rm dsat}}{V_{\rm ds}} \times \frac{l_{\rm d}E_{\rm c}}{(L_{\rm eff} - l_d)E_{\rm c} + V_{\rm dsat}}, \quad (V_{\rm ds} > V_{\rm dsat}). \tag{8a}$$

This is consistent with channel length modulation mechanism theoretically, where $l_{\rm d}$ is defined as velocity saturation region length (shown as $L_{\rm d}$ in Fig.1), an important parameter in channel saturation-state. Different from the simple empirical model [10] of $l_{\rm d}$=0.22 $t_{\rm ox}^{1/3}x_j^{1/2}$, it is given by an accurate model from 2D analysis [11]

$$l_{\rm d} = l\ln\left[\frac{V_{\rm ds} - V_{\rm dsat}}{lE_{\rm c}} + \frac{E_{\rm m}}{E_{\rm c}}\right], \tag{8b}$$

where the maximum electric field at drain terminal of the channel is obtained as follows:

$$E_{\rm m} = \sqrt{\left(\frac{V_{\rm ds} - V_{\rm dsat}}{l}\right)^2 + E_{\rm c}^2}. \tag{8c}$$

In addition, it is noted that Eqs.(8b) and (8c) are only valid in the saturation region. And they should be modified by substituting saturation voltage $V_{\rm dsat}$ with the parameter $V_{\rm dsx}$ in order to fit the condition in the linear region. The $V_{\rm dsx}$ with only one fitting constant A is given by [5]

$$V_{\rm dsx} = V_{\rm dsat}\{1 - [\ln(1 + {\rm e}^A)]^{-1} \times [1 + {\rm e}^{A(1 - V_{\rm ds}/V_{\rm dsat})}]\}. \tag{8d}$$

3. Modelling of source and drain parasitic series resistance in LDD nMOSFET

In conventional MOSFET, the parasitic series resistance of source region (or drain region) consists of three parts:

$$R_{\rm s}(R_{\rm d}) = R_{\rm sh} + R_{\rm co} + R_{\rm sp}, \tag{9}$$

where $R_{\rm sh}$, $R_{\rm co}$ and $R_{\rm sp}$ are sheet resistance, ohmic contact resistance, and spreading resistance, respectively. In LDD MOSFET, however, $R_{\rm sp}$ and $R_{\rm sh}$ are significantly large because of the low-doped region (i.e. the n^- region). For simplicity, $R_{\rm s}$ ($R_{\rm d}$) of LDD MOSFET can be given by [1]

$$R_{\rm s}(R_{\rm d}) = R_{\rm co} + \frac{2\rho S}{x_{\rm j}W}, \tag{9a}$$

where ρ is the fitting resistivity of the low-doped region, S is the spacer thickness, i.e. the thickness of side wall, and x_j is the junction depth of the LDD

region. In fact, the contact resistance R_{co} cannot be calculated exactly because it is dependent on the manufacture process. So the parasitic resistance is usually extracted from the measurement and then optimized in the model with their calculations *in situ*. This technique has found wide application in the measurement-based model. Under the influence of the parasitic series resistance, the actual output current I_{ds} is significantly less than the intrinsic drain current. From the equivalent circuit of the device model, the relationship between intrinsic and external gate and drain voltage is given as

$$V_{gs}(\text{intrinsic}) = V_{gs}(\text{external}) - I_{ds}R_s;$$
$$V_{ds}(\text{intrinsic}) = V_{ds}(\text{external}) - I_{ds}(R_s + R_d). \quad (10)$$

Substituting Eq.(10) in Eq.(1), the iteration algorithm is used to obtain I_{ds}. In order to obtain a good convergence in iteration, Gauss–Newton and Levenberg–Marquardt optimization are used to solve the nonlinear function $f(I_{ds}) = I_{ds} - I_{dsat}(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) = 0$.

4. Modelling in subthreshold region

The previous description is suitable for the strong inversion state. When $V_{gs} - V_{th} \leq 0$, the weak inversion state appears, and the device works in the subthreshold region. The drain current I_{ds} decreases to zero smoothly, by no means abruptly in this region, according to the device physics. For this purpose, some empirical methods have been developed to fit the smooth trend by adjusting the overdrive voltage $(V_{gs} - V_{th})$.[2,5] This technique avoids a complicated analysis of the surface potential in device physics. In this work, an equivalent gate overdrive voltage is proposed to describe the device mechanism in the subthreshold region, shown as

$$(V_{gs} - V_{th})_{eff} = \ln[1 + e^{\delta(V_{gs} - V_{th})}]/\delta, \quad (11)$$

where δ is a fitting constant that indicates the velocity of the drain current decrease in the subthreshold region. In a weak inversion state, $(V_{gs} - V_{th})_{eff}$ decreases smoothly to zero value. In a strong inversion state, V_{gs} is large enough and $(V_{gs} - V_{th})_{eff} \to (V_{gs} - V_{th})$, which is consistent with the previous assumption. The smooth transformation between zero and $(V_{gs} - V_{th})$ is guaranteed by the logarithmic and exponential functions, following the idea of behaviour model which finds wide application in the nonlinear modelling of devices. Substituting the modified $(V_{gs} - V_{th})$ into the previous model, we can easily describe the mechanism of devices in the subthreshold region.

5. Simulation results and analysis

We verify the simulation of the model by the measurements of the submicron LDD MOSFET in Ref.[5]. The necessary extracted parameters are adopted in our simulations to improve the accuracy of the model. During simulation, the convergence monitor shows that it only requires 10–12 steps of iteration for each calculated point of drain current, indicating a very low computation consumption.

Figure 2 gives the simulated results of LDD MOSFET with drawn channel length $L_{mask} = 0.72\mu$m. The extracted effective channel length $L_{eff} = 0.56\mu$m has been given in Ref.[5], and the other extracted parameters are: t_{ox}=18nm, x_j=0.25μm, N_A=2.2×10^{16}cm^{-3}, N_D=1×10^{18}cm^{-3}, μ_0=665cm^2/(V·s), v_{sat}=5.76×10^{6}cm/s, and the parasitic series resistance R_S (R_d)=38Ω. In Fig.2(a), the comparison between simulated and measured I–V characteristics shows a good agreement. The related fitting constants in our model are A=2 in Eq.(8d), ξ=2/3 in Eq.(7a), and δ=7 in Eq.(11). Also in Fig.2(b), the simulated drain conductance demonstrates an excellent smooth transition between linear and saturation regions, indicating the effectiveness of the hyperbolic-tangent model. Figure 2(c) gives the simulated and the measured transconductance characteristics, showing good fitting results. The transconductance continuity is correctly predicted in the strong inversion region ($V_{gs} > V_{th}$) and in the subthreshold region ($V_{gs} \leq V_{th}$). It is noted that there exists an abrupt transconductance change under a very small drain-source bias. The reason is that the formation of a critical channel causes the significant increase of current near the region of $V_{gs} = V_{th}$, thus increasing the g_m. After the formation of the channel, the increment of channel current is not so large. This mechanism is more relevant with the vertical electric field distribution from gate to substrate. When a large V_{ds} is biased, the change of transconductance g_m is not so obvious after the channel formation. In Fig.2(d), the I_{ds}–V_{gs} characteristics from subthreshold to strong inversion are simulated, where the linear and the saturation regions are all included. The results show clearly the continuity of the drain current, consistent with the physics of MOSFETs.

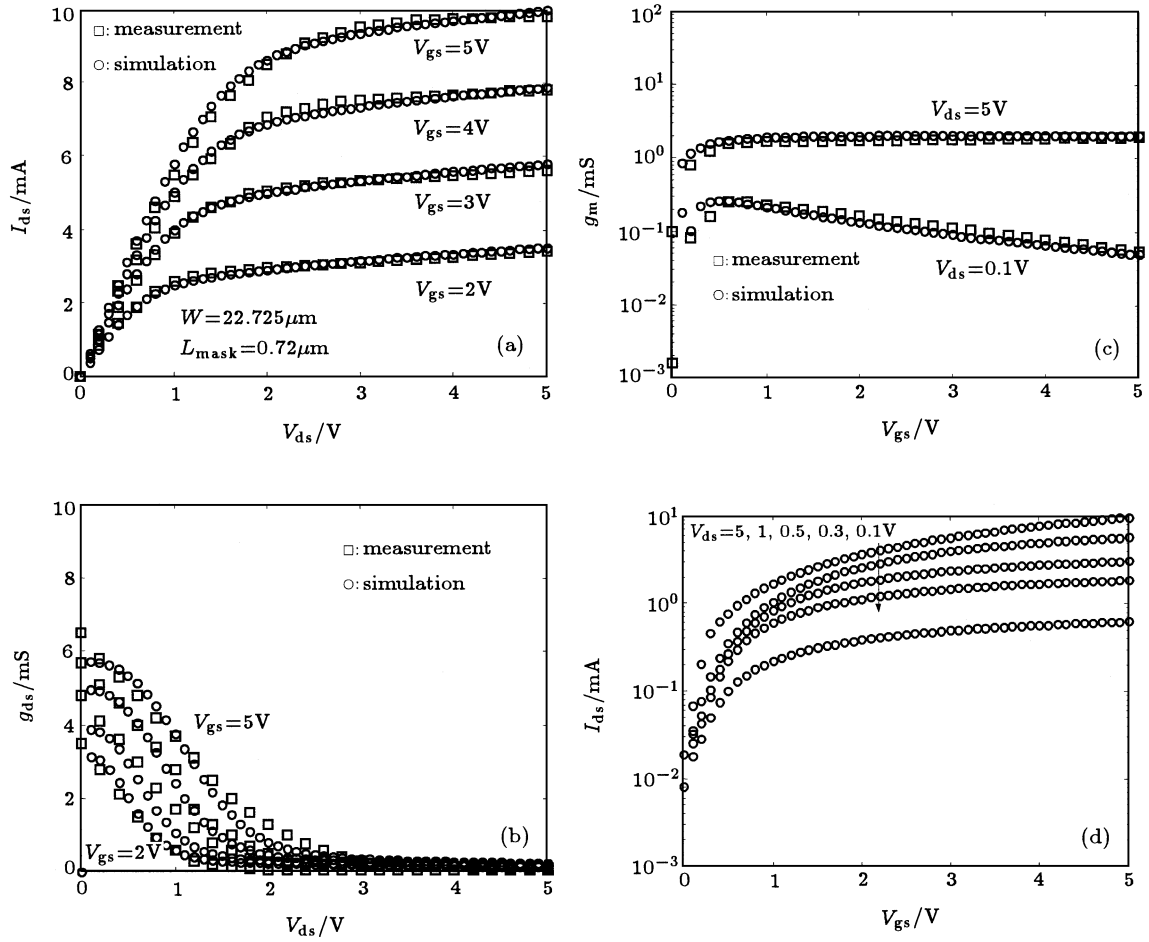


Fig.2. Simulated and measured electrical characteristics of W/L=22.7μm/0.72μm LDD MOSFET, where the strong inversion and subthreshold conditions are included. (a) Comparison between the simulated and the measured output drain current characteristics. (b) Comparison between the simulated and the measured output drain conductance characteristics. (c) Simulated and measured transconductance in linear region and saturation region. (d) Simulated I_{ds}–V_{gs} characterization in strong inversion and subthreshold, where V_{ds} changes from linear to saturation region.

For application in deep submicron devices, the electrical characteristics of the 0.4μm gate length MOSFET are simulated with the present model. Figure 3 illustrates the simulated results of 0.4μm LDD MOSFET, in which the extracted effective channel length L_{eff} equals 0.29μm, and the other extracted parameters are: t_{ox}=9nm, x_j=0.18μm, N_A=3.0×10^{16}cm^{-3}, N_D=1.1×10^{18}cm^{-3}, μ_0=605cm^2/(V·s), v_{sat}=3.6×10^{6}cm/s, and the parasitic series resistance R_S (R_d)=30Ω. The related fitting constants in our model are A=2, ξ=1/3, and δ=10. Good agreements between simulations and measurements show the robustness of this improved model for short-length LDD MOSFETs.

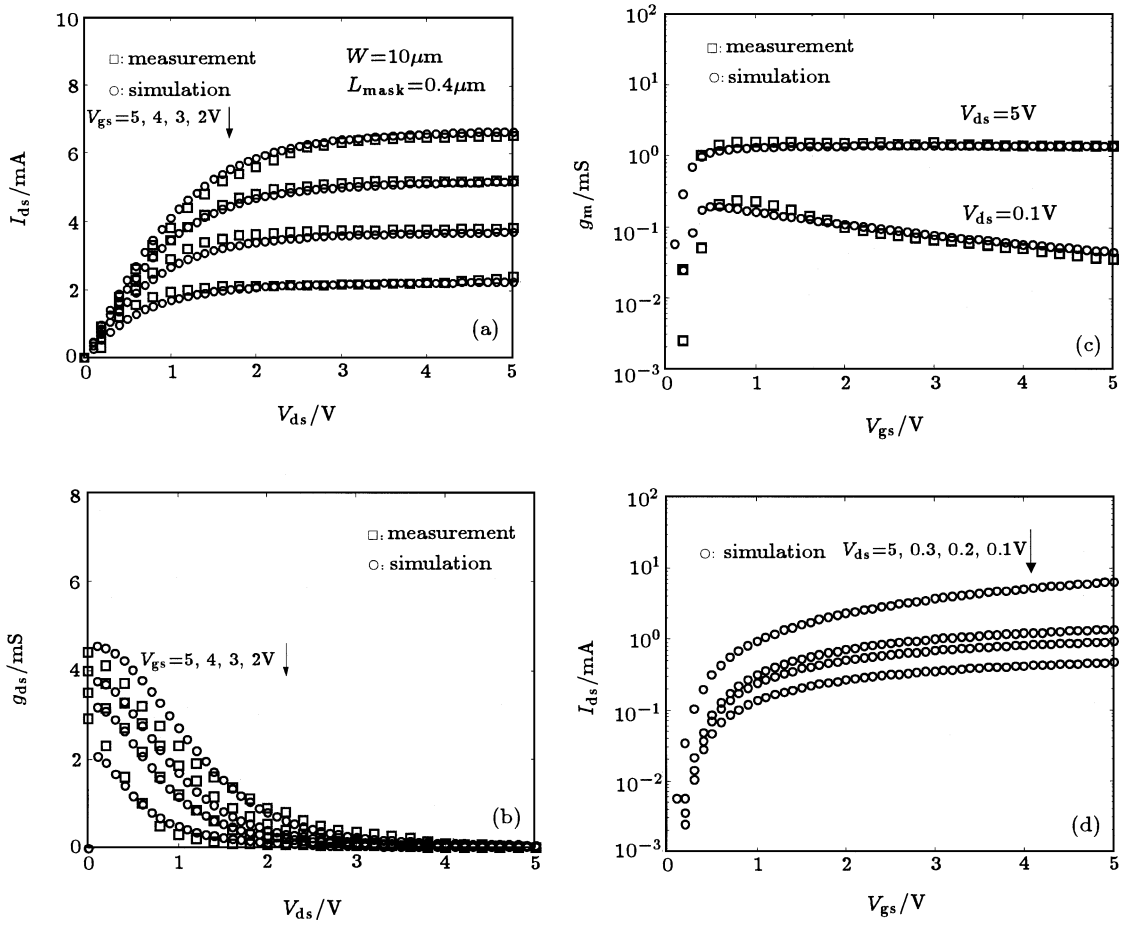


Fig.3. Simulated and measured electrical characteristics of W/L=10μm/0.4μm LDD MOSFET, where the strong inversion and subthreshold conditions are included. (a) Comparison between the simulated and the measured output drain current characteristics. (b) Comparison between the simulated and the measured output drain conductance characteristics. (c) Simulated and measured transconductance in linear region and saturation region. (d) Simulated I_{ds}–V_{gs} characterization in strong inversion and subthreshold, where V_{ds} changes from linear to saturation region.

6. Conclusion

A novel compact I–V model for submicron and deep submicron LDD MOSFETs has been developed, in which the carrier velocity saturation theory and the hyperbolic-tangent description are adopted. The model deals with the I–V characteristics in either strong inversion or the subthreshold region. Also, the smooth transition between linear and saturation regions is taken into account. The modelling is based on the methodology for the physical model and the empirical model, thus decreasing the computation consumption, maintaining the accuracy, and clarifying the mechanism of devices. The comparison between simulations and measurements for submicron and deep submicron LDD MOSFET shows an excellent agreement. With this methodology, the substrate current and the gate current parameters can be easily embedded in the model to match the related device measurement [12] and explore the hot carrier degradation of the deep submicron devices.

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