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Low frequency effects of surface states on 4H-SiC metal-semiconductor field effect transistor*

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The process-related surface state effect is investigated the fabrication of SiC devices, and a nonlinear model for 4H-SiC power metal-semiconductor field effect transistor (MESFET) is proposed, which takes into account the surface-related parameters. The frequency- and temperature- dependent transconductance dispersion is readily demonstrated in terms of the improved model. Simulation results show that larger dispersion and higher transition frequency occur in 4H-SiC MESFET than in GaAs MESFET. The advantage of this analytical model over the two-dimensional numerical simulation is the simplicity of calculations, therefore it is suitable for the processing improvement of SiC devices.

Keywords: silicon carbide, MESFET, surface states, transconductance
PACC: 2560, 7210, 7220

1. Introduction

Silicon carbide (SiC) is a promising wide bandgap material for power radio frequency devices, because it has high values of breakdown electric field, electron saturation velocity, thermal conductivity and antiradiation. The excellent figure of merit of 4H-SiC metal-semiconductor field effect transistor (MESFET) makes it a potential candidate for applications in high-definition television systems, phased array radars and the next generation telecommunication base stations, etc.

SiC MESFET has much more difficulties in fabrication than GaAs FET because of higher annealing temperature (more than 1500°C for ion implantation and near 1000°C for ohmic contact) and limited, etching. The recess gate processing, which is commonly used in microwave power MESFET suffers surface degradation in 4H-SiC MESFET. The reason is that the, etching of the SiC materials is limited to the dry-etch, i.e. reactive ion, etching (RIE), wherein the, etching damage occurs and increases the surface state density. The surface states yield the dispersion of Schottky barrier high at gate region and decreasing source-drain resistance at un-gate region. Although the process such as SacOx or ICP has been used after, etching, it is hardly to eliminate the damage. Additionally, surface passivation required for power MESFET increases the SiO_2/SiC interface effects. Thus the influence on the characterization of MESFET has to be taken into account. It is of same importance as the bulk trapping effect occurring at the interface of channel/buffer and in a p-buffer layer. However, few papers published in recent years have considered physically the effect of surface states on the output characterization in modelling of 4H-SiC MESFET, mainly because SiC is the immature material and the SiC-based devices are still under research. Some related papers demonstrated the evidence only in measurements.[1,2] But for GaAs-based microwave devices, more detailed analysis, physically and numerically, are shown in Refs.[3–5]. Some measurement-based large-signal nonlinear models find wide applications in power MESFET, including GaAs and SiC. However, these models cannot de-embed the surface effects because the relevant parameters do not come from physics but from data extraction. For the design and fabrication of SiC MESFET, it is necessary to develop a physical model for the description of surface state effects. In this paper, an advanced analytical model for 4H-SiC power MESFET is proposed, which takes into account the surface state effects. The steady-state and transient analysis show the frequency- and temperature- dependent output characterization clearly and simply, compared with

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the complicated two-dimensional numerical simulations.

2. Fabrication process and surface state formation

Figure 1 shows the cross-section view of power 4H-SiC MESFET. The channel between source and drain is, etching-recessed to increase the output power and decrease the noise. One p-buffer layer commonly used in SiC MESFET has different thickness in different substrate types, i.e., 5–8μm for conducting substrates (0.01$\sim$0.02 ohm-cm, $\sim 10^{18}\mathrm{cm}^{-3}$ doping), less than 1μm for semi-conducting substrates ($> 1 \times 10^{15}$ ohm-cm). This layer may yield an obvious bulk trapping effect. The traps are at the channel/buffer interface or in buffer and substrate occurring as deep level traps, accordingly they have the heavy impact on output characteristics. Emphasis in this paper is put on the surface state effect that is determined mainly by the fabrication process. The 4H-SiC material with N/P/N/N^+ multi-layer is used to fabricate power MESFET. The conventional process includes: mesa and recess gate region formation, source and drain ohmic contact formation with metal Ni deposition and annealing, gate metal Ti/Pt/Au deposition, interconnection and air bridge formation, surface passivation. Only the dry, etching (RIE or plasma, etch) method could be used in the recess region of 4H-SiC MESFET, thus yielding lattice damage and increasing the surface state density. As a result, not only could there exist a transitional interfacial layer between gate metal and SiC, but also the interface states would change the energy spectrum in the energy bandgap. Consequently, the ideal Schottky contact boundary condition is changed and the dispersion of Schottky barrier high ϕ_{bi} arises. At the un-gate region, the thin depletion layer caused by the surface states increases the source and drain resistance, and this trend is frequency- and temperature- dependent. Simultaneously, the lateral surface electron mobility in the channel is decreased by surface roughness scanning. So the practical channel mobility has a magnitude smaller than that obtained in Hall measurements. In fact, the electron saturation velocity also decreases, but the change is very small. As the reverse bias on the gate is increased, the gate leakage current also increases as a consequence of either tunnelling or thermionic emission. The emitted electrons are trapped by surface states, causing the build-up of a large amount of negative surface charges. The more the surface states that are available to trap electrons, the greater the reduction of the lateral electric field between the gate and the drain. This will change the field-dependent mobility and complicate the carrier transportation, but increase the gate-to-drain breakdown voltage.

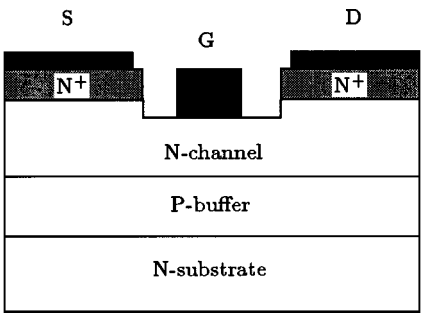


Fig.1. The cross-section view of a power 4H-SiC MESFET.

3. Modelling of surface-state related parameters

What is described above is considered in the device basic parameters to investigate the effect of surface states physically. Equation (1) shows the bulk resistances of gate-source, gate-drain and channel under gate, which are very important for the output characterization of MESFET.

$$R_{\mathrm{gs}} = L_{\mathrm{gs}}/(q\mu N_D^+ W a),$$

$$R_{\mathrm{gd}} = L_{\mathrm{gd}}/(q\mu N_D^+ W a),$$

$$R_{\mathrm{ch}} = L_{\mathrm{g}}/[q\mu N_D^+ W(a - W_R)], \qquad (1)$$

where L_{gs}, L_{gd}, L_{g}, a,μ, N_D^+, W_R and W are the gate-source space, gate-drain space, gate length, channel thickness, ionized channel doping, gate width and the zero bias depletion width under gate, respectively. Under the influence of surface states, a depletion layer with width W_0 forms because of the surface electrons congregation. W_0 is approximately equal to W_R theoretically[3] and experimentally.[2] Additionally, a small low-frequency ac signal modulates the gate voltage V_{gs} in the transconductance measurement. This will cause the capture of electrons and thereby increase another change of depletion layer thickness ΔW_0, given as follows:

$$\Delta W_0 = \frac{\Delta n_s(f,T)}{N_D^+}, \qquad (2)$$

where $\Delta n_s(f,T)$ is the surface state occupancy. It is frequency-and temperature-dependent from the

Laplace transform, as in Ref.[5]:

$$\Delta n_s(f,T) = \frac{n_0}{n_0+N_c} N_{ss} \frac{1}{1-j\dfrac{e_n}{\omega}}, \tag{3}$$

where n_0, N_c, N_{ss} and ω are the surface electron concentration, conduction band effective density of states, surface state density and angular frequency, respectively; e_n is the emission rate of the surface electron trap, given by

$$e_n = N_c c_n \exp\left(-\frac{E_{\rm T}}{k_B T}\right), \tag{4}$$

where c_n is the capture coefficient of surface electrons, and E_T is the activation energy. As described above, we can modify the bulk resistance as follows:

$$R_{\rm gd} = L_{\rm gd} \Big/ \left\{ q\mu N_D^+ W \left[a - \left(W_0 + \frac{\Delta n_s(f,T)}{N_D^+} \right) \right] \right\},$$

$$R_{\rm gs} = L_{\rm gs} \Big/ \left\{ q\mu N_D^+ W \left[a - \left(W_0 + \frac{\Delta n_s(f,T)}{N_D^+} \right) \right] \right\}. \tag{5}$$

Theoretically, the pinch-off voltage $V_p = qN_D a^2 / 2\varepsilon_r\varepsilon_0$ will change because of decreasing the effective channel thickness. We assume the pinch-off voltage unchanged in this paper. The reason is that the effect of surface states occurs clearly in the large output current region which is far apart from the pinch-off region. Practically, V_p is very complicated and is different from the above calculation.[6] It may be affected easily by the bulk trap in p-buffer layer but not by surface states. The experimental evidence has been shown in Ref.[2].

The relation between electron mobility and the channel lateral electric field is of great complexity. Equation (6) gives the experimental expression[7] and the precision depends on the fitting coefficient β.

$$\mu(E) = \frac{\mu_0}{\left(1+\left(\dfrac{\mu_0 E}{\nu_{\rm sat}}\right)^{\beta}\right)^{1/\beta}}. \tag{6}$$

It is not rigorous to analyse the surface-related mobility with the above fitting expression. The reason is that we cannot extract the surface-state effect from the coefficient β. Here we only use the low-field mobility μ_0 in modelling the short gate length (0.5–0.7μm) SiC-MESFET because the theory of velocity saturation is suitable for the analytical models and only the low-field mobility is concerned (described in section 4). The assumed smaller low-field mobility than that published in other papers is used here for the description of surface state effect on lateral electron mobility.

4. Analytical model for 4H-SiC power MESFET

The relevant parameters described above are embedded in the analytical model of I-V characteristics[8] to demonstrate the steady-state and transient state phenomena caused by the surface states, shown as:

$$I_{\rm ds}(V_{\rm gs}, V_{\rm ds}) = I_{\rm dsat} \cdot (1+\lambda \cdot V_{\rm ds}) \cdot \tanh(\alpha \cdot V_{\rm ds}), \tag{7}$$

where

$$I_{\rm dsat} = qN_D^+ \nu_{\rm sat} a W (1-u_m),$$

$$\lambda = g_{\rm ds}(V_{\rm gs}, V_{\rm ds}) / I_{\rm dsat}(V_{\rm gs}),$$

$$\alpha = g_{\rm d0}(V_{\rm gs}) / I_{\rm dsat}(V_{\rm gs}).$$

From the relation between intrinsic and extrinsic bias voltages, shown as $V_{\rm gs}({\rm int.})=V_{\rm gs}({\rm ext.})-I_{\rm ds}R_{\rm s}$ and $V_{\rm ds}({\rm int.})= V_{\rm ds}({\rm ext.})-I_{\rm ds}(R_s+R_{\rm d})$, it is clear that Eq.(7) is in an iterative form. All the above parameters are not fitting coefficients but calculated theoretically. So the developed model can guarantee the physical analysis of the surface state mechanism.

From Eq.(7), one can easily calculate the steady-state or the frequency-related output I-V characteristics and transconductance. The theoretical low-frequency dispersion of transconductance for GaAs MESFET is given as follows[3,5]:

$$g'_m(f,T) = \frac{\dfrac{V_{\rm gs}\varepsilon W}{L_{\rm g} W_R}\mu(T)}{\left[1+\dfrac{R_{\rm gs}+R_{\rm gd}}{R_{\rm ch}}\right]^2}, \tag{8}$$

Equation (8) is suitable for describing GaAs devices in the linear region under very small $V_{\rm gs}$ and $V_{\rm ds}$ conditions, thus $V_{\rm gs} \approx V_{\rm ds}$. In our model, the expression is slightly different for the transconductance in 4H-SiC MESFET is different from that in GaAs FET. This parameter is directly extracted from the I-V characteristics utilizing the definition $g_m = \partial I_{\rm ds}/\partial V_{\rm gs}|_{V_{\rm ds}={\rm cons}}$.

5. Simulation results and analysis

Equations (1)–(5) are implemented in the developed analytical model (7). The frequency- and temperature- dependent I-V characteristics and the extracted transconductance can easily be derived. Figure 2 demonstrates the steady-state I-V curve for large current. The low-frequency dispersion is

not included but the lower mobility caused by surface states is shown. The relevant material parameters and device structure for calculation is given in Refs.[9] and [10]: E_T=240meV, $N_{SS}=10^{11} \sim 10^{12}\text{cm}^{-2}$, $C_n = 5\times10^{-7}\text{cm}^3/\text{s}$, $n_0 = 10\times N_D^+$, $N_D = 1.7\times10^{17}\text{cm}^{-3}$, L_g=0.7μm, L_{gs}=0.5μm, L_{gd}=2.5μm, a=0.27μm, W=150μm. V_{bi} and N_C are temperature-dependent and can be calculated theoretically.[6] The ionized channel doping N_D^+ can be derived from the properties of 4H-SiC material.

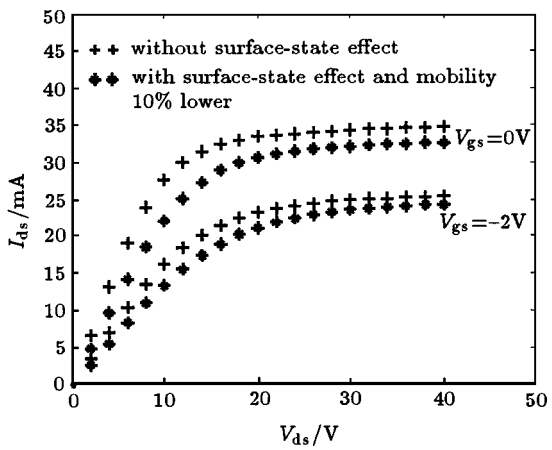


Fig.2. The steady-state I-V output characteristics with and without surface state effect. The lower electron mobility describes the effect of surface scanning.

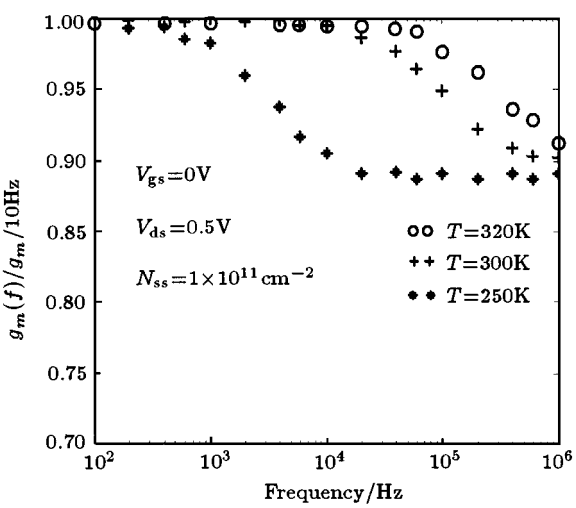


Fig.3. The normalized transconductance versus gate signal frequency at different temperature. For 4H-SiC MESFET, the quiescent bias V_{gs}=0V, V_{ds}=0.5V is in the linear region.

Shown in Fig.3 is the normalized transconductance $g_m(f)/g_m(10\text{Hz})$. It is obvious that there exists a dispersion in the low-frequency region, compared with the radio frequency and microwave applications. Also shown in the curve is the heavy impact of the temperature on the transconductance dispersion. Compared with the applications of GaAs power MESFETs, the SiC power MESFETs can work in higher temperature range, the transition-frequency point moves in turn to the higher frequency region and affects the microwave characterizations negatively.

Figure 4 illustrates the normalized transconductance versus surface state density N_{SS}. The large N_{SS} can cause a serious effect. If the density decreases below 10^{11}cm^{-2}, the dispersion becomes very small. The dispersion is very sensitive to N_{SS}, thus the processing-caused surface states must be considered carefully in device fabrications.

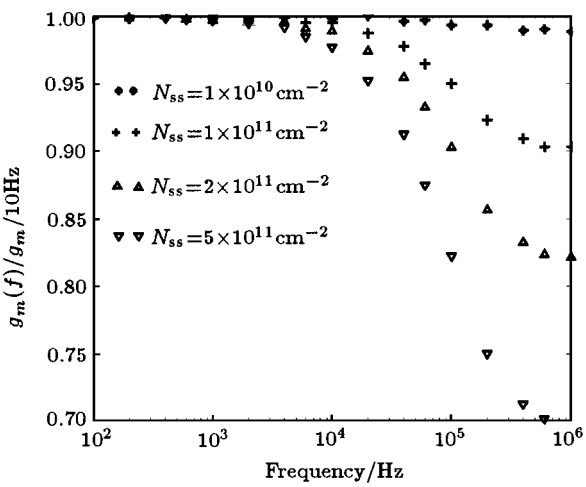


Fig.4. The transconductance dispersion under different surface state densities. It nearly disappears when $N_{SS} < 10^{11}\text{cm}^{-2}$.

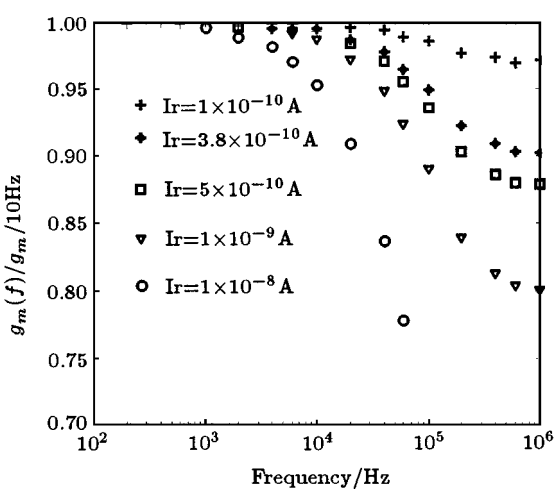


Fig.5. The impact of gate reverse leakage current Ir on transconductance. The large leakage current results heavy dispersion.

The electron congregation in a very thin layer (about 5–10nm) at the surface can form a surface conduction channel that yields the reverse leakage current

and thus degrades the performance of devices. Figure 5 displays the influence of gate reverse leakage current Ir on transconductance. The results show that the leakage current must be controlled in processing, otherwise heavy degradation would occur.

6. Conclusion

Because of more difficult processing in SiC MESFET fabrications, there exists the heavy effect of surface states on the performance of devices compared with GaAs MESFET. In this paper, we have developed an improved model to investigate the surface state effect theoretically. The degradation of output I-V characteristics and the low frequency- and temperature- dependent transconductance dispersion are derived from the model. The calculations are simple compared with commonly used two-dimensional numerical simulations. The simulation results show that the low-frequency dispersion of transconductance occurs at the higher-frequency region (10^4Hz–10^5Hz at 300K) because of lower activation energy of 4H-SiC than that of GaAs. Meanwhile, the dispersions of transconductance are larger. These will have great influence on the radio frequency and microwave applications of SiC MESFETs.

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