Vol 11 No 9, September 2002
1009-1963/2002/11(09)/0944-04
Chinese Physics
© 2002 Chin. Phys. Soc.
and IOP Publishing Ltd

The charge storage of the nc-Si layer*

Dai Min(戴 敏), Zhang Lin(张 林), Bao Yun(鲍 云),
Shi Jian-Jun(石建军), Chen Kai(陈 铠), Li Wei(李 伟),
Huang Xin-Fan(黄信凡), and Chen Kun-Ji(陈坤基)

State Key Laboratory of Solid State Microstructures and Department of Physics, Nanjing University, Nanjing 210093, *China*

(Received 2 February 2002; revised manuscript received 15 May 2002)

Sandwiched structures (a-SiN_x/a-Si/a-SiN_x) have been fabricated by the plasma enhanced chemical vapour deposition technique. A Si nanocrystal (nc-Si) layer was formed by crystallization of an a-Si layer according to the constrained crystallization principle after quasi-static thermal annealing at 1100°C for 30 min. Transmission electron microscopy (TEM) and Raman scattering spectroscopy clearly demonstrated that nc-Si grains were formed in the as-deposited a-Si layer after annealing. The density of nc-Si grains is about $10^{11}cm^{-2}$ as shown by TEM photographs. Using capacitance–voltage (C–V) measurements we investigated the electrical characteristics of the sandwiched structures. The charge storage phenomenon of the nc-Si layer was observed from the shift of flat-band voltage (V_{FB}) in C–V curves at a high frequency (1 MHz). We estimated the density of nc-Si grains to be about $10^{11}cm^{-2}$ from the shift value of V_{FB}, which is in agreement with the result of TEM photographs. At the same time, we found that the shift of V_{FB} increased with the increase of the applied constant dc voltage or the thickness of the nc-Si layer.

Keywords: nc-Si, thermal annealing, C–V characteristics, charge storage
PACC: 7360N

1. Introduction

With the development of nano-electronics, considerable attention is focused on nc-Si electronic devices because of their potential applications.[1−3] The key technology for making nc-Si devices is the fabrication of nc-Si quantum dots, whose size, distribution and density can be artificially controlled. By means of various annealing methods, some researchers have obtained nc-Si thin films of high density and uniform size according to the constrained crystallization principle.[4,5]

In this paper, we report on the fabrication of sandwiched structures (a-SiN_x/a-Si/a-SiN_x) using the plasma enhanced chemical vapour deposition (PECVD) technique. Following this, the a-Si layer in the structure is crystallized to form the nc-Si layer according to the constrained crystallization principle after quasi-static thermal annealing.

Moreover, capacitance–voltage (C–V) measurements are one of the most widely used means in the study of electrical properties and fabrication quality of semiconductor devices. Some important parameters, such as film thickness, substrate impurity density, fixed charges, interface state density and so on, can be estimated from C–V curves. Recently, these have also been used to discuss the charge storage of nc-Si structures.[6,7] In this way, we have studied the electrical characteristics of the a-SiN_x/a-Si/a-SiN_x sandwiched structure and observed the charge storage of the nc-Si layer.

2. Experiment

The sandwiched structures (a-SiN_x/a-Si/a-SiN_x) were deposited on a substrate of p-type (100) crystalline silicon (6–8Ω·cm) in the PECVD system at 250°C with a radio-frequency (rf) power of 40 W. Pure silane was used to deposit the a-Si layer while a gas mixture of silane and ammonia was used to deposit the SiN_x layer. The deposition rate for both layers was about 6nm/min. All wafers were treated with diluted hydrofluoric acid before deposition. Figure 1 shows a schematic cross section of the samples of sandwiched structures. A series of samples, in which the thickness of a-Si layers varied from 2, 4, 7 to 10nm, was sandwiched between two layers of 30nm thick a-SiN_x

*Project supported by the National Natural Science Foundation of China (Grant Nos 90101020 and 60071019), the Natural Science Foundation of Jiangsu Province, China (Grant Nos BK2001028 and BG2001002), the State Key Programme of Basic Research of China (Grant No 2001CB610503), and in part by Korea MOST through TND Project.
†Author to whom correspondence should be addressed. E-mail: kjchen@netra.nju.edu.cn

that served as double barriers. Then, the crystallization of samples was performed by furnace annealing at 1100°C for 30 min in N_2 atmosphere.

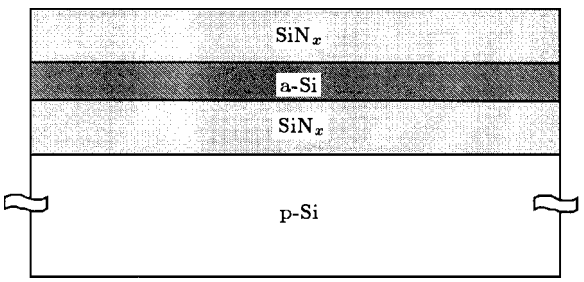


Fig.1. A schematic diagram of the cross section of the a-SiN$_x$/a-Si/a-SiN$_x$ sandwich-structured sample.

After this, we verified the crystallization of the a-Si layer in the annealed samples by transmission electron microscopy (TEM) and Raman scattering spectroscopy, and we investigated the electrical characteristics of the sandwiched structures at room temperature using C–V measurements.

3. Results and discussion

3.1. Structural analysis of samples

The top and bottom layers of a-SiN$_x$, as the effect of double barriers in the sandwiched structure, confined the crystallization of the a-Si layer in the annealing process. Due to the constrained crystallization, the nc-Si grains crystallized in the a-Si layer may be arranged in a monolayer, and their mean size is close to the thickness of the a-Si layer if this thickness is thin enough. Meanwhile, the density and mean size can be controlled by the time and temperature of annealing.[4] In our case, to achieve the goal of controlling the density and mean size of nc-Si we have changed the thickness of the a-Si layer as the time and temperature of annealing are fixed.

Figure 2 shows the TEM photographs of the annealed samples, the thicknesses of which are 2 nm (a) and 4 nm (b). The nano-sized grains can be observed and their densities are about $0.8\times10^{11}\,\mathrm{cm}^{-2}$ in Fig.2(a) and $1.7\times10^{11}\,\mathrm{cm}^{-2}$ in Fig.2(b). The density of the sample with a thicker layer is approximately two times that of the thinner. It can be assumed that the bulk density of nuclei formed in the crystallization is equal under the same annealing conditions, so that the surface density doubles correspondingly with the volume doubled.

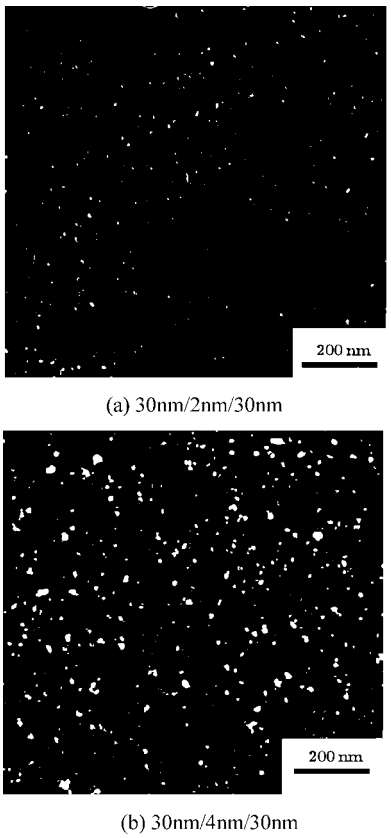


Fig.2. TEM photographs of the annealed samples.

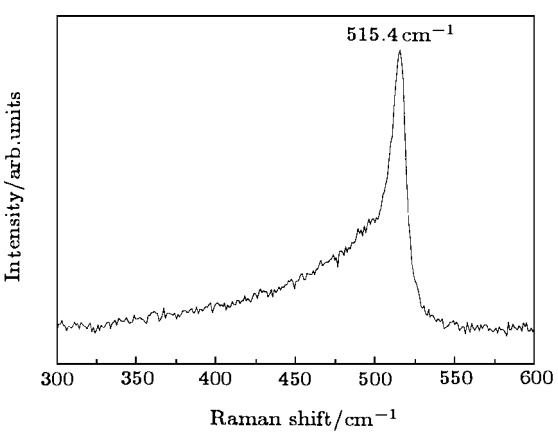


Fig.3. The Raman scattering spectrum of 30 nm/10 nm/30 nm annealed sample.

Figure 3 illustrates the Raman scattering spectrum of the annealed sample containing a 10 nm thick as-deposited a-Si layer. The sharp peak appearing at $514.5\,\mathrm{cm}^{-1}$ clearly confirms our expectation that the grains are nc-Si grains in the TEM photographs. We estimated the crystallization ratio (ρ), which is about 35%, through the well-known formula

$$\rho = \frac{\rho_0}{(\rho_m + \rho_0)}, \tag{1}$$

where ρ_0 and ρ_m are the areas of crystalline and amorphous peaks, respectively.

The above result indicates that we have obtained nano-sized nc-Si grains with high density in the a-Si layer after annealing.

3.2. C–V characteristics

In order to discuss the dynamic model of charges in the a-SiN_x/nc-Si/a-SiN_x structure, the C–V characteristics were measured by a HP4294A precision impedance analyser at room temperature. The high-frequency (1 MHz) and low-frequency (1 kHz) C–V curves were measured first. In the annealed samples, we obtained quasi-static curves while in the unannealed samples we did not. This demonstrates that after annealing the quality of the samples is improved. Table 1 shows the flat-band voltage (V_{FB}) and interface state density (N_{it}) of two series of samples, unannealed and annealed. The results show that samples with 2nm or 4nm thick as-deposited a-Si layer have a better quality than the others with whatever V_{FB} or N_{it}. However, annealing does not improve the property of V_{FB}; that is, it has no distinct effect on the fixed charges. So we believe that the qualities of interfaces in annealed samples are fine.

Table 1. N_{it} and V_{FB} of unannealed and annealed samples.

Thickness of as-deposited a-Si layer/nm		2	4	7	10
V_{FB}/V	unannealed samples	0.035	−0.15	—	−8.6
	annealed samples	−1.46	−1.7	−4.4	−3.4
$N_{it}/10^{10}cm^{-2}\cdot eV^{-1}$	unannealed samples	—	—	—	—
	annealed samples	3.4	3.9	—	5.3

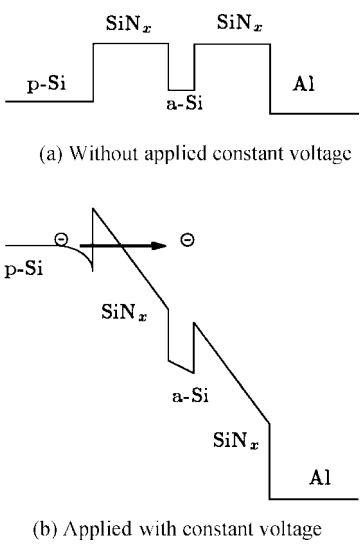


Fig.4. Schematic band diagram of sandwiched sample.

Furthermore, a constant dc voltage was imposed on the samples for some time to investigate the charge storage by succeeding C–V measurements. In metal–oxide–semiconductor (MOS) structures, V_{FB} is an important parameter to manifest the fixed charges in oxide. Recently, it was reported that, in the C–V measurements of samples with nc-Si grains embedded in the oxide, the carriers may tunnel to nc-Si grains due to the effect of applied constant dc voltage and they may be trapped. Thus, they act as fixed charges in the oxide layer and then shift the V_{FB}. Hence, the charge storage effect can be observed from the shift of V_{FB} through C–V measurements.[8,9] But there is a 30 nm thick SiN_x barrier layer in our samples so that the probability of tunnelling is low. Nevertheless, tunnelling may occur when a constant dc voltage is imposed, in view of the quite low potential barrier of the SiN_x layer. Figure 4 shows the model of possible tunnelling. It can be seen that the actual width of the barrier decreases because of the sloping of the energy band and hence the possibility of tunnelling increases.

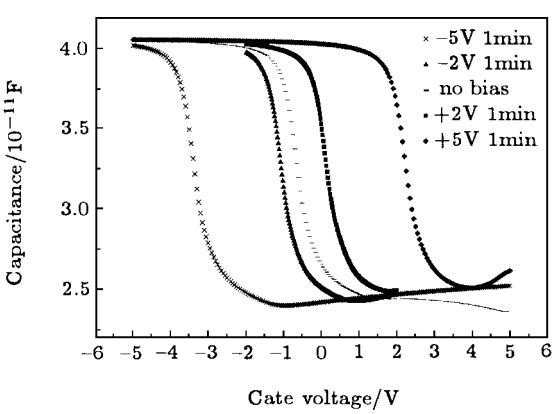


Fig.5. The C–V characteristics of a 30 nm/2 nm/30 nm annealed sample with different constant voltages applied.

We applied different voltages on the annealed samples with various thicknesses of nc-Si layers, and a distinct charge storage phenomenon was observed in all of the annealed samples. Figure 5 shows the C–V curves (at 1 MHz) of the sample which has a 2nm thick nc-Si layer. The dc voltage initially imposed was −5 V, −2 V, +2 V and +5 V, respectively, for 1 min.

We also gave the original curve without the voltage initially imposed, and found that the higher the voltage applied, the greater the V_{FB} shifted, indicating that the more charges were stored through tunnelling. However, such a phenomenon was not observed in the unannealed samples. The only distinction between the two kinds of sample is whether or not there are nc-Si grains in the as-deposited a-Si layer. Therefore, it can be considered that the charge storage relates directly to the nc-Si grains in the annealed samples.

At the same time, we found that the shift of V_{FB} increased with the thickness of the nc-Si layer. The density of nc-Si grains could be estimated from the shift of V_{FB} (ΔV_{FB}), by assuming that only one carrier was trapped by an nc-Si grain. The formula is as follows

$$\sigma = \Delta C \cdot \Delta V_{\mathrm{FB}}/(q \cdot s), \qquad (2)$$

where s is the area of top contact, and ΔC is the difference between maximum and minimum capacitance. In this way, we obtained the density (σ) of nc-Si grains to be about the order of $10^{11}\mathrm{cm}^{-2}$ in the 2nm or 4nm thick nc-Si layers, which was consistent with the results of TEM photographs.

4. Conclusions

In summary, we have utilized Raman scattering spectroscopy and TEM to investigate the structural properties of a-SiN_x/a-Si/a-SiN_x sandwiched samples after annealing, confirming that the as-deposited a-Si layer has crystallized to form the nc-Si layer. Using C–V measurements, the movement of carriers was studied in the sandwiched structures, and it is observed that the shift of V_{FB} increased with the increase of applied constant dc voltage or the thickness of nc-Si layer in the annealed samples. Hence we believe that the shift is related to the nc-Si grains and the phenomenon of charge storage does exist.

Acknowledgments

The authors gratefully thank Professor Zhao Xiao-Ning for the TEM observation.

References

[1] Gu X F, Qin H, Lu H, Chen K J and Huang X F 1996 *J. Non-Cryst. Solids* **227-230** 1168

[2] Qin H, Gu X F, Lu H, Liu J H, Huang X F and Chen K J 1999 *Solid State Commun.* **111** 171

[3] Ma S Y, Qin G G, You L P and Wang Y Y 2001 *Acta Phys. Sin.* **50** 1580 (in Chinese)

[4] Wang L, Li J, Huang X F, Xu J, Li W and Chen K J 2000 *Appl. Surf. Sci.* **165** 85

[5] Choi S and Ellima R G 1999 *Appl. Phys. Lett.* **75** 968

[6] Tsybeskov L, Grom G F and Megnea N 2000 *Mater. Sci. Eng.* B **69-70** 303

[7] Baron T, Gentile P and Megnea N 2001 *Appl. Phys. Lett.* **79** 1175

[8] Ishikawo Y, Kosugi M and Kumezawa M 2000 *Thin Solid Films* **369** 69

[9] Dons E M and Skowronski C S 1998 *Appl. Phys. Lett.* **73** 2712