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Double threshold behaviour of I–V characteristics of $CoSi_2$/Si Schottky contacts*

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The forward current–voltage (I–V) characteristics of polycrystalline $CoSi_2$/n-Si(100) Schottky contacts have been measured in a wide temperature range. At low temperatures (≤200K), a plateau-like section is observed in the I–V characteristics around 10^{-4}A·cm^{-2}. The current in the small bias region significantly exceeds that expected by the model based on thermionic emission (TE) and a Gaussian distribution of Schottky barrier height (SBH). Such a double threshold behaviour can be explained by the barrier height inhomogeneity, i.e. at low temperatures the current through some patches with low SBH dominates at small bias region. With increasing bias voltage, the Ohmic effect becomes important and the current through the whole junction area exceeds the patch current, thus resulting in a plateau-like section in the I–V curves at moderate bias. For the polycrystalline $CoSi_2$/Si contacts studied in this paper, the apparent ideality factor of the patch current is much larger than that calculated from the TE model taking the pinch-off effect into account. This suggests that the current flowing through these patches is of the tunnelling type, rather than the thermionic emission type. The experimental I–V characteristics can be fitted reasonably well in the whole temperature region using the model based on tunnelling and pinch-off.

Keywords: Schottky barrier height, metal–semiconductor contact, inhomogeneity
PACC: 7330, 7340N

1. Introduction

The observed current–voltage (I–V) characteristics of real Schottky diodes usually deviate from the ideal thermionic emission (TE) mode, such as the strong dependence of both the Schottky barrier height (SBH) and the ideality factor on temperature, the difference in SBHs determined from different methods, the nonlinearity of the Richardson plots and the double threshold behaviour in the I–V characteristics at low temperatures, etc. Traditionally, many mechanisms, such as generation-recombination current, tunnelling current, leakage current and the effect of image force lowering, have been taken into account in order to explain these deviations.[1] However, in many cases, the magnitude of the observed deviations is too large to be explained by the above mechanisms. Recently, it has been pointed out that the barrier height is inhomogeneous in the metal–semiconductor (M–S) interface.[2–7] It may contain patches with low barrier height. The total current is the sum of the currents through all of these patches and the current through the whole junction area. Moreover, if the patch area is small (less than, or comparable to, the depletion region), the pinch-off effect should be taken into account, i.e. the effective reduction of the SBH between the patch and the surrounding area is smaller than its original drop in the M–S interface.[4,5] In the literature, both currents (through patches and through the whole junction area) are usually assumed to be thermionic emission. At high temperatures (>200K) or in the large bias region at low temperatures, the combination of both currents can be approximately described by a Gaussian distribution of the SBH.[7,8] The total current has a similar expression as the traditional TE model but with an apparent barrier height and an apparent ideality factor, both of which are temperature dependent. On the other hand, I–V characteristics at low temperatures may be dominated by the current through a few relatively large patches at the small bias region. However, these patch currents

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may saturate with increasing bias voltage due to the large local series resistance and the high current density near the patch; thus a flexion in the I–V curves at moderate bias can be observed. This phenomenon is called the "double threshold behaviour".

The patches and their distribution are obviously dependent on diode parameters and the contact fabrication process. Our previous studies on various $CoSi_2$/Si contacts have shown that the double threshold behaviour depends significantly on $CoSi_2$/Si interface quality.[8] For a high-quality epitaxy $CoSi_2$/Si diode, no double threshold phenomenon is observed. For some epitaxy $CoSi_2$/Si diodes, the excess current is relatively small and can be explained by the patch current with thermionic emission.[7] However, for polycrystalline $CoSi_2$/Si diodes, the excess current is relatively large and the corresponding slope of the ln$I$–V plot is small. That is, the apparent ideality factor of the patch current is much larger than that calculated from the pinch-off model of Tung[4] where the patch current is assumed to be of TE type. Recently, Aniltürk *et al.*[9] reported that the patch current is of tunnelling rather than thermionic type. Using this assumption, and also taking the pinch-off effect into account, the experimental I–V characteristics can be fitted reasonably well in the whole temperature region.

2. Experimental details

The substrates used in this work were n^-/n^+ epitaxial Si(100) wafers (phosphor doped). The doping level of the epitaxial layer was about $8\times10^{15}\mathrm{cm}^{-3}$. Square windows with different areas were opened using standard lithography and wet etching procedures. After standard RCA cleaning and dipping in a diluted hydrofluoric acid (HF) solution, the wafers were immediately loaded into the chamber of an Oxford sputtering system with a base pressure of about 1×10^{-4}Pa. Cobalt was deposited with different thickness of 2.5, 10 and 20nm. The $CoSi_2$ silicide was formed by a two-step rapid thermal annealing (RTA) with an interval selective etching step: firstly 600°C for 1min, and secondly 800°C for 1min.

The I–V measurements were made automatically using a Keithley 619 electrometer and a multifrequency LCR HP 4274A meter. The diode was cooled by liquid N_2 and the variation of the temperature was better than ±4K during each temperature point of measurement.

The ultra-thin $CoSi_2$/Si contacts were also measured by ballistic electron emission microscopy (BEEM) and spectroscopy (BEES), which were carried out using an AIVTB-4 system of surface/interface using a Pt–Ir tip in air at −30°C.

3. Results and analysis

Figure 1(a) shows forward I–V characteristics of one of the polycrystalline $CoSi_2$/Si diodes at temperatures ranging from 91K to room temperature. The diode was formed from Co(20nm)/Si and the diode area (A) was $6.084\times10^{-3}\mathrm{cm}^{-2}$. Other diodes (with different $CoSi_2$ thicknesses or different areas) have similar I–V characteristics. Firstly, the experimental data were fitted by an equation based on the TE theory[1]

$$I_{\mathrm{th}} = AA^{**}T^2\exp(-q\Phi_{\mathrm{b}}/k_{\mathrm{B}}T) \times \exp[q(V - IR_{\mathrm{s}})/nk_{\mathrm{B}}T] \quad (V \geq 3k_{\mathrm{B}}T/q), \tag{1}$$

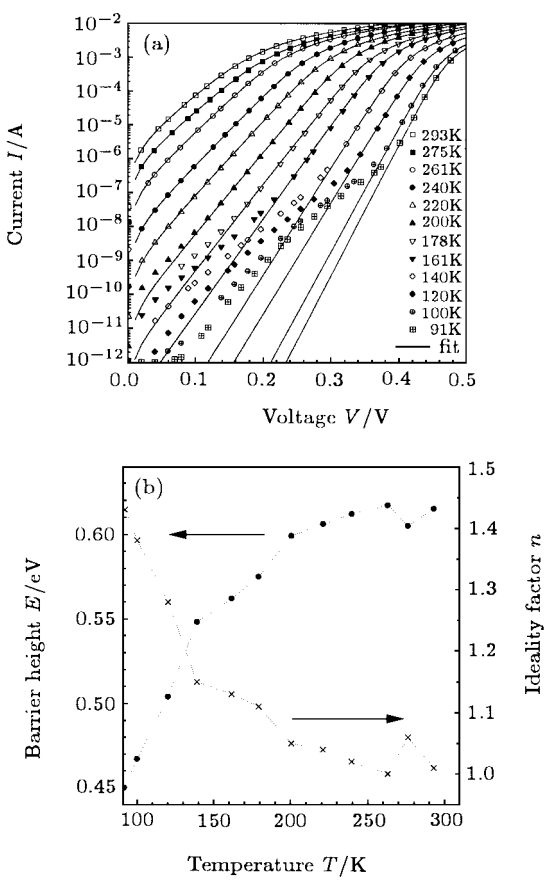


Fig.1. (a) The forward I–V characteristics at temperatures from 91 to 293K of a polycrystalline $CoSi_2$/n-Si diode formed from 20nm Co with a contact area of $6.1\times10^{-3}\mathrm{cm}^{-2}$ and their fitting curves based on the TE model. (b) The apparent barrier height (•) and the apparent ideality factor (×) deduced from the fitting as a function of temperature.

where A^{**}, T, q, k_B, Φ_b, n and R_s are the effective Richardson constant ($\approx$117.7A·cm^{-2}·K^{-2} for n-type Si), temperature in Kelvin, the electronic charge, the Boltzmann constant, the apparent barrier height, the apparent ideality factor and the diode series resistance, respectively. A least-squares fitting was carried out using a computer program using Φ_b, n and R_s as adjustable parameters. The fitting lines are also shown in Fig.1(a). These match the experimental data quite well at high temperatures ($\geq$200K) or in the large bias region at low temperatures. The value of R_s is about 14$\sim$16Ω, almost independent of temperature. Both Φ_b and n are temperature dependent, as shown in Fig.1(b), which can be explained by a Gaussian distribution of the SBH.[3,8,10] A detailed analysis of this has been reported in our previous paper.[8]

Here we pay attention to the plateau-like section in low-temperature I–V characteristics around 10^{-6}A. The experimental current in the small bias region at low temperatures significantly exceeds that expected by the above-mentioned modified TE model. Such a double threshold phenomenon has also been observed by other authors[11] and in our studies on other M–S contacts (Au/n-Si and PtSi/n-Si). In the literature, the excess current is attributed to the generation-recombination current or the leakage current in the diode edge. We find that it cannot explain our experimental results. Firstly, we have measured diode capacitance at different frequencies (10, 50, 100 and 500kHz) and we have found that the capacitance is independent of frequency, indicating the absence of a measurable amount of deep levels in the silicon substrate. Secondly, carrier recombination is expected to occur in the depletion region at the periphery of the diode,[12] so diodes with a smaller area-to-periphery ratio are expected to exhibit a larger carrier recombination current. However, no significant difference is found between the diodes with different areas in our experiments. Thirdly, the recombination mechanism depends on the quality of the depletion region of the silicon substrate, rather than the quality of the $CoSi_2$ films. However, our results show that the double threshold behaviour depends significantly on the quality of $CoSi_2$ films. For some high-quality epitaxial $CoSi_2$/Si diodes, no double threshold phenomenon has been observed, even when the same silicon substrates are used.

In our previous studies on epitaxial $CoSi_2$/Si diodes,[7] the excess current is attributed to the current through a few relatively large patches with reduced barrier height. The current is assumed to be of TE type and the normal pinch-off model is used. However, for the polycrystalline $CoSi_2$/Si diodes studied in this paper, the excess current is relatively large and the corresponding slope of the ln$I$–V plot is small (i.e. the apparent ideality factor is large). It is difficult to fit this by the normal pinch-off model with thermionic emission. For example, the apparent ideality factor of the patch current at 91K in Fig.1(a) is about 2.4, while the value calculated from the normal pinch-off model is about 1.6; even the parameter of the patch is assumed to be as large as 10×10^{-4}cm$^{2/3}$V$^{1/3}$. Apparently, the experimental data can be fitted well if an artificial ideality factor n_a is introduced additionally in the equation obtained from the pinch-off model:[3]

$$I_p = A_{eff}A^{**}T^2\exp(-q\Phi_{eff}/k_BT) \times \{\exp[q(V - I_pR_{sr})/n_ak_BT] - 1\}, \quad (2)$$

where R_{sr} is the series resistance through the patch. Φ_{eff} and A_{eff} are the effective SBH and the effective area of the patch, respectively. Both of these depend on the parameter of the patch γ

$$\gamma = 3(\Delta R_0^2/4)^{1/3}, \quad (3)$$

where R_0 is the patch radius, and Δ is the barrier height reduction at the M–S interface. The fitting results of the above diode are shown in Fig.2. The total junction current is composed of two parts: $I = I_{th} + I_p$. Here, I_{th} is the current through the whole junction with a Gaussian distributed SBH (calculated by Eq.(1), shown in Fig.1(a)), and I_p is the current through a patch with $\gamma \approx 4.7\times10^{-4}cm^{2/3}V^{1/3}$ (calculated by Eq.(2)), represented by the dotted lines in Fig.2. The curvature of the patch current results from the relatively large series resistance R_{sr}, which can be approximated to be a spreading resistance of a circular contact spot:[13] $R_{sr} \approx \rho_s/4\pi R_0$, where ρ_s is the local resistivity of the patch. It is difficult to determine accurate values of both ρ_s and R_0 from the experiment. Fortunately, R_{sr} is not sensitive to the current in the low bias region in which we are interested. In our case, the bulk resistivity is about 1Ω·cm and R_0 is between tens of nanometres to a hundred nanometres and R_{sr} can be assumed to be $\approx 5\times10^4\Omega$. The experimental data can be fitted by this approach quite well in the whole bias region and at all temperatures. The value of n_a varies from 1.39 to 1.22 with the temperature increasing from 91 to 178K, respectively. The larger than unity artificial ideality factor

and its temperature dependence indicate that charge carriers flow through the patch with a different current mechanism.

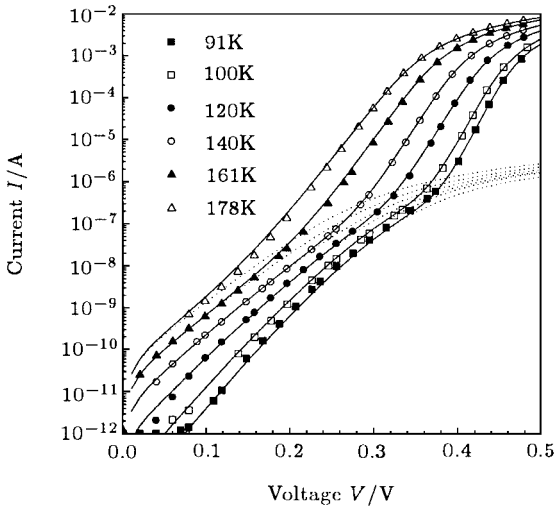


Fig.2. The measured and calculated I–V characteristics of the diode in Fig.1 at temperatures from 91 to 178K. The dotted lines represent patch currents calculated based on the modified pinch-off model with $\gamma \approx 4.7 \times 10^{-4}\mathrm{cm}^{2/3}\mathrm{V}^{1/3}$ and n_a=1.39, 1.37, 1.34, 1.31, 1.27 and 1.22, respectively. The solid lines represent the total currents.

Recently, Aniltürk *et al.*[9] have suggested that the current through patches may be of tunnelling type. In their approach, the characteristic energy for the tunnelling process (E_{00}) and the patch area (A_p) were used as adjustable parameters. But the barrier height in the patch is assumed to be the same as the surrounding area. In this paper, we assume that the patch has a low SBH and that the current flows through the patch by tunnelling. Taking the pinch-off effect into account, the patch has an effective barrier height Φ_eff and an effective area A_eff. For simplification, we use the same expressions of Φ_eff and A_eff as those deduced from Tung's pinch-off model where the TE theory is used. Then we can use one parameter γ to determine both Φ_eff and A_eff. In addition, we use the standard expression for tunnelling in a uniform M–S contact,[1] but with Φ_eff and A_eff instead of a single barrier height Φ and the contact area A. Then the patch current can be described approximately by following expressions

$$I_\mathrm{p} = I_\mathrm{s}\exp[(V - I_\mathrm{p}R_\mathrm{sr})/E_0] \times \{1 - \exp[-q(V - I_\mathrm{p}R_\mathrm{sr})/k_\mathrm{B}T]\} \quad (4a)$$

and

$$I_\mathrm{s} = \frac{A_\mathrm{eff}A^{**}T^2 q\,\exp(-q\Phi_\mathrm{n}/k_\mathrm{B}T)[\pi E_{00}(\Phi_\mathrm{eff} - V - \Phi_\mathrm{n} - I_\mathrm{p}R_\mathrm{sr})]^{1/2}}{k_\mathrm{B}T\cosh(qE_{00}/k_\mathrm{B}T)} \times \exp[-(\Phi_\mathrm{eff} - \Phi_\mathrm{n})/E_0], \quad (4b)$$

where Φ_n is the difference between the equilibrium Fermi level and the band edge. E_0 is given by

$$E_0 = E_{00}\coth(qE_{00}/k_\mathrm{B}T) \quad (5)$$

and E_{00} is expressed as

$$E_{00} = (h/4\pi)(N_\mathrm{d}/m^*\varepsilon_\mathrm{Si})^{1/2}, \quad (6)$$

where h is the Planck constant, N_d is the dopant concentration, m^* is the carrier effective mass and ε_Si is the dielectric constant of silicon. The parameter of the patch γ and the characteristic energy for the tunnelling process E_{00} are used as adjustable parameters to fit the excess current in Fig.1(a). The use of E_{00} as an adjustable parameter is based on the fact that the tunnelling mechanism can be enhanced by an increase of electric field and the interface states.[14] Since the patches are related to defects, grain boundaries, facets, etc, and have different properties compared to the surrounding area of the junction, E_{00} may be much larger than that calculated from Eq.(6). The best computer fit generated using Eq.(4) is shown by the dotted curve in Fig.3. The solid curves represent the total currents of I_p+I_th. These match the experimental data quite well at all temperatures. The γ value used for all temperatures is $3.64\times10^{-4}\mathrm{cm}^{2/3}\mathrm{V}^{1/3}$ and the E_{00} values are 1.60, 1.75, 1.85, 2.05, 2.18, 2.30 and 2.45×10^{-2}eV for temperatures of 91, 100, 120, 140, 161, 178 and 200K, respectively. The slight increase of E_{00} with temperature may be explained by the fact that more interface states or defects are excited with increasing temperature, thus the tunnelling enhancement effect is increased. The effect of patch current gradually decreases as the temperature increases and becomes negligible (i.e. $I_\mathrm{p} < I_\mathrm{th}$ in the whole bias region) above 200K.

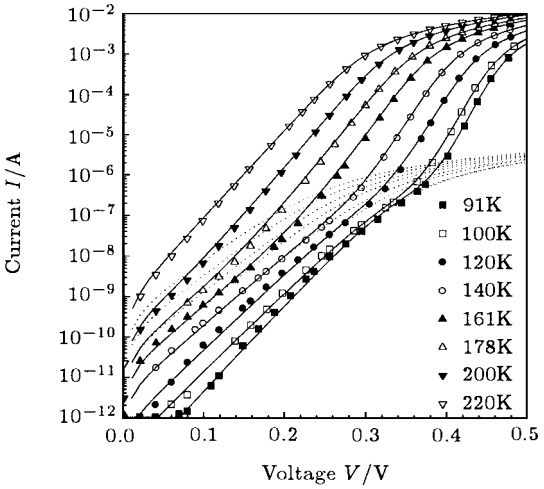


Fig.3. The measured and calculated I–V characteristics of the diode in Fig.1 at temperatures from 91 to 220K. The dotted lines represent patch currents calculated on the basis of the tunnelling and pinch-off model, and the solid lines represent the total currents.

The forward I–V characteristics of two other types of polycrystalline $CoSi_2$/Si diodes are also analysed using the above model, and the results are shown in Figs.4(a) and 4(b), respectively. Fig.4(a) shows a $CoSi_2$/Si diode formed from 10nm Co on n-Si(100) and Fig.4(b) shows an ultra-thin $CoSi_2$/Si diode formed from 2.5nm Co on n-Si(100). The dotted lines represent the patch current by tunnelling and the dashed lines represent the current through the whole junction with a Gaussian distributed SBH by thermionic emission. The solid lines are the sum of above two components. They both match the experimental data quite well at all temperatures. For temperatures above 200K, the total currents are dominated by thermionic emitted transport over the whole junction and are not shown in Fig.4. The fitting parameters are γ=3.8×10^{-4}cm$^{2/3}$V$^{1/3}$ and E_{00}=0.0165∼0.0240eV for the diode in Fig.4(a) and γ=4.1×10^{-4}cm$^{2/3}$V$^{1/3}$ and E_{00}=0.025∼0.030eV for the ultra-thin $CoSi_2$/Si diode in Fig.4(b). The patch current component of the ultra-thin $CoSi_2$/Si diode is more significant than for the other two diodes. This can be explained by the fact that the ultra-thin $CoSi_2$ film has larger variation of the relative thickness and may also contain discontinuities in the ultra-thin film.

The barrier height properties of ultra-thin $CoSi_2$/Si diodes can also be studied by BEEM at low temperatures. Fig.5 shows the spatial distribution of local SBHs for the above ultra-thin $CoSi_2$/Si diode. The local SBH is deduced from the BEEM spectrum according to a Kaiser–Bell quadratic law and taking the thermal broadening correction into account.[15,16] In total, 107 BEEM spectra are acquired, spreading over the whole contact area randomly at −30°C. In some locations, no BEEM current can be measured due to local defects, surface contamination or the $CoSi_2$ film discontinuity. Those locations may be related to the patch with different SBHs and are not included in our statistics. The histogram of the measured SBH distribution obeys a Gaussian distribution approximately with a mean value of SBH of 637meV and the standard deviation of 19meV, in agreement with the results deduced from the I_{th} component of the experimental I–V data.

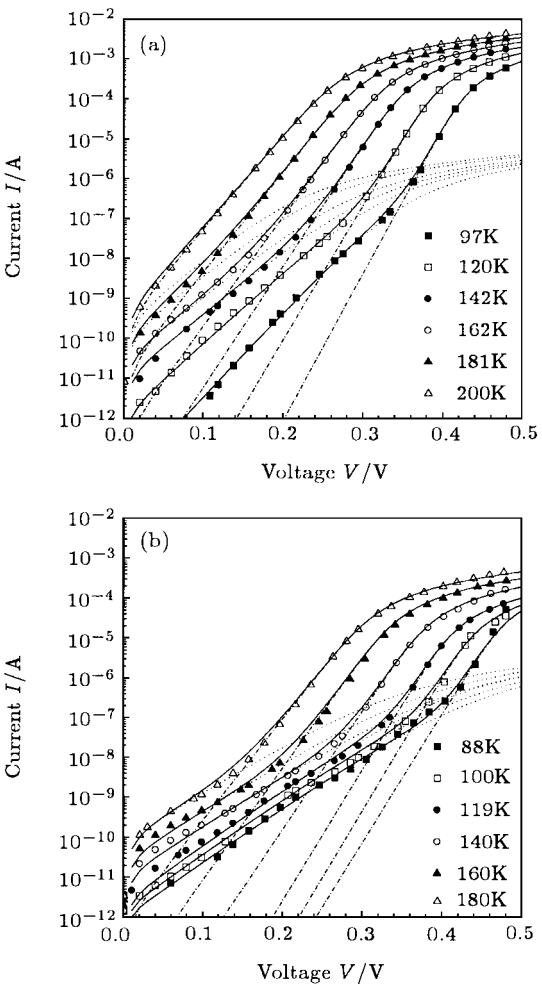


Fig.4. The measured and calculated I–V characteristics of: (a) the $CoSi_2$/n-Si diode formed from 10nm Co; (b) the ultra-thin $CoSi_2$/Si diode formed from 2.5nm Co at low temperatures. The dotted lines represent patch currents calculated based on the tunnelling and pinch-off model. The dashed lines represent the TE currents through the whole junction with a Gaussian distributed SBH. The solid lines represent the total currents.

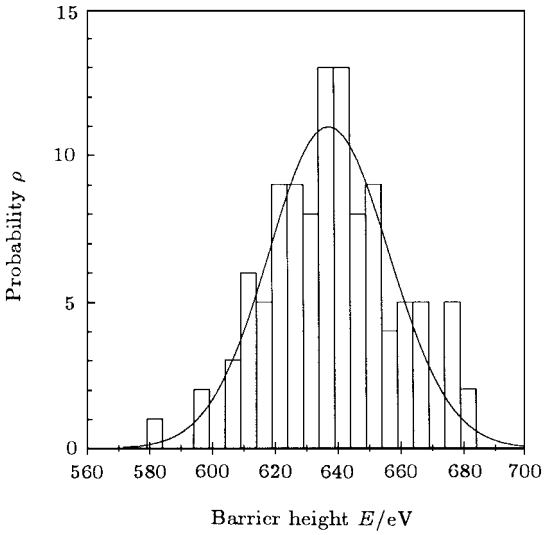


Fig.5. Statistical SBH distribution and its Gaussian fit of the ultra-thin $CoSi_2$/n-Si diode. In total, 107 BEEM spectra were measured at −30°C.

4. Discussion

Our pinch-off and tunnelling model differs from the pinch-off and TE model of Tung[4] and the tunnelling model of Aniltürk *et al.*[9] Tung's model regards the patch current as thermionic emission and uses γ as the adjustable parameter. Aniltürk *et al.* assume that the current flows through the patch by tunnelling with the same barrier height between the patch and the surrounding area, and E_{00} and A_p are used as adjustable parameters. Our model combines above models, using γ and E_{00} as adjustable parameters. To compare these three models, I–V traces are calculated at temperatures between 80 to 220K with a step of 20K based on these three models, and are shown in Figs.6(a)–6(c). The diode parameters are Φ_0=0.62eV, N_d=1.0×10^{16}cm^{-3}, R_{sr} = 5 × 10$^4\Omega$ and the adjustable parameters are γ = 3.6 × 10^{-4}cm$^{2/3}$V$^{1/3}$, E_{00}=0.025eV, A_p=1.0×10^{-5}cm^{-2}. This shows clearly that our pinch-off and tunnelling model gives the closest I–V–T characteristics to the experimental data at the small bias region. At the lowest temperature (80K), the I–V trace calculated by the tunnelling model is close to the pinch-off and tunnelling model. Both models give an apparent ideality factor of about 3–4, close to the experimental result. Whereas the pinch-off and TE model gives a much smaller current and the apparent ideality factor is about 1.4. The patch current is dominated by the tunnelling process at that low temperature. However, the current calculated by the pinch-off and TE model increases quickly with increasing temperature. It is close to that calculated by the pinch-off and tunnelling model at 220K. On the other hand, the tunnelling current depends weakly on temperature, especially at high temperatures. Thus the barrier height difference of the patch and the pinch-off effect cannot be neglected.

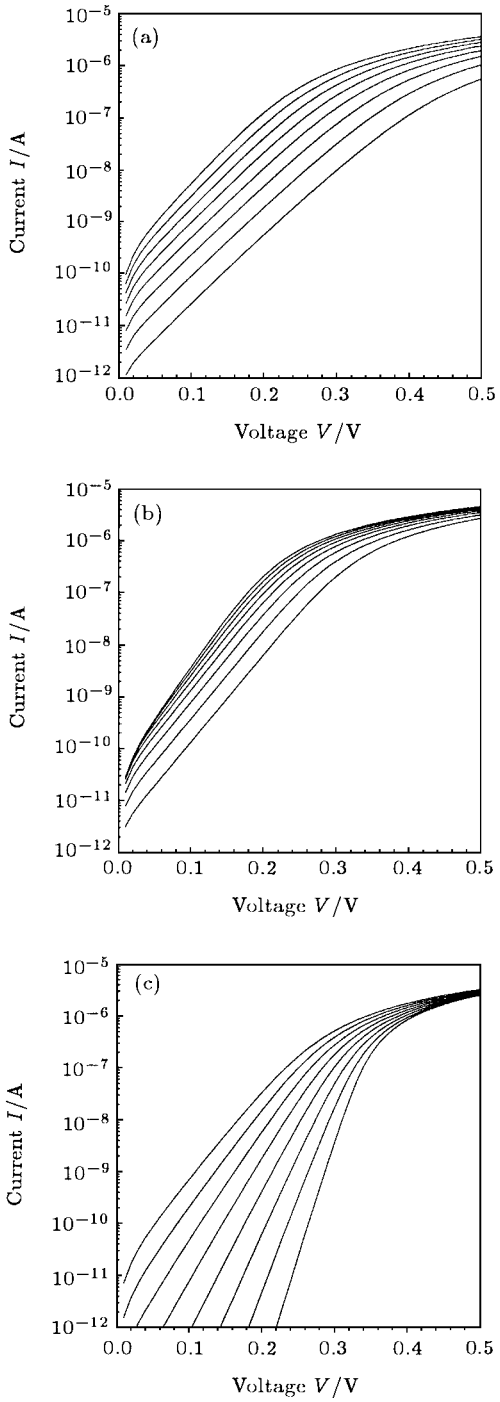


Fig.6. I–V traces at 80 to 220K with a step of 20K calculated by three models: (a) the tunnelling and pinch-off model; (b) the tunnelling model; (c) the pinch-off and TE model. The diode parameters are Φ_0=0.62eV, N_d=1.0×10^{16}cm^{-3}, R_{sr}=5×10$^4\Omega$ and the adjustable parameters are γ=3.6×10^{-4}cm$^{2/3}$V$^{1/3}$, E_{00}=0.025eV, A_p=1.0×10^{-5}cm^{-2}.

Both pinch-off (TE and tunnelling) models give a γ value of about $3.6\times10^{-4}\mathrm{cm}^{2/3}\mathrm{V}^{1/3}$. If the barrier height decrease at the M–S interface is assumed to be about 0.3eV, the patch area calculated from Eq.(3) is about $7\times10^{-11}\mathrm{cm}^{-2}$. This is of the same magnitude as the effective area of the patch (A_{eff}), which is weakly dependent on bias and temperature and has a value of around $2\times10^{-11}\mathrm{cm}^{-2}$. This value is about five orders of magnitude smaller than the patch area (A_{p}) assumed in the tunnelling model. However, in the BEEM studies a barrier height variation in the region of tens of nanometres is observed. Moreover, no large defect ($\sim 10^{-5}\mathrm{cm}^{-2}$) is observed in the $CoSi_2$ films by photomicroscopy. The low-SBH patch is believed to have a small area.

5. Conclusions

The double threshold behaviour of I–V characteristics in polycrystalline $CoSi_2$/Si diodes is explained by the pinch-off and tunnelling model. The total junction current is made up of two components. One component (I_{th}) is the thermionic emission current through the whole junction with a Gaussian distributed barrier height. The other (I_{p}) is the current through some small low-SBH patches by tunnelling. At low temperatures, I_{th} dominates in the large bias region and I_{p} dominates in the small bias region, thus a double threshold behaviour is observed. At high temperatures, I_{th} dominates in the whole bias region and the contribution of the small patches can be neglected. Using this model, the I–V characteristics of various polycrystalline $CoSi_2$/Si diodes can be fitted reasonably well in the whole temperature region.

References

[1] Rhoderick E H and Williams R H 1988 *Metal–Semiconductor Contacts* 2nd edn (Oxford: Clarendon)

[2] Song Y P, Van Meirhaeghe R L, Laflere W H and Cardon F 1986 *Solid State Electron.* **29** 633

[3] Werner J H and Güttler H H 1991 *J. Appl. Phys.* **69** 1522

[4] Tung R T 1992 *Phys. Rev.* B **45** 13 509

[5] Sullivan J P, Tung R T, Pinto M R and Graham W R 1991 *J. Appl. Phys.* **70** 7403

[6] Lahnor P, Seiter K, Schulz M, Dorsch W and Scholz R 1995 *Appl. Phys.* A **61** 369

[7] Zhu S Y, Van Meirhaeghe R L, Detaveriner C, Cardon F, Ru G P, Qu X P and Li B Z 2000 *Solid State Electron.* **44** 663

[8] Zhu S Y, Detaveriner C, van Meirhaeghe R L, Cardon F, Ru G P, Qu X P and Li B Z 2000 *Solid State Electron.* **44** 1807

[9] Aniltürk Ö S and Turan R 2000 *Solid State Electron.* **44** 41

[10] Chand S and Kumar J 1997 *J. Appl. Phys.* **82** 5005

[11] Hatzikonstantinidon S, Wikman P, Zhang S L and Petersson C S 1996 *J. Appl. Phys.* **80** 952

[12] Wittmer M 1991 *Phys. Rev.* B **43** 4385

[13] Cox R H and Strack H 1967 *Solid State Electron.* **10** 1213

[14] Horvath Z J 1996 *Solid State Electron.* **39** 176

[15] Kaiser W J and Bell L D 1988 *Phys. Rev. Lett.* **60** 1406

[16] Zhu S Y, Detaveriner C, van Meirhaeghe R L, Qu X P, Ru G P, Cardon F and Li B Z 2000 *Semicond. Sci. Technol.* **15** 349