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COULOMB BLOCKADE OSCILLATIONS OF Si SINGLE-ELECTRON TRANSISTORS*

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Coulomb blockade oscillations of Si single-electron transistors, which are fabricated completely by the conventional photolithography technique, have been investigated. Most of the single-electron transistors clearly show Coulomb blockade oscillations and these oscillations can be periodic by applying negative voltages to the in-plane gates. A shift of the peak positions is observed at high temperatures. It is also found that the fluctuation of the peak spacing cannot be neglected.

Keywords: single-electron tunnelling, Coulomb blockade, quantum dots
PACC: 7335C, 7340G, 7360

I. INTRODUCTION

Coulomb blockade oscillations (CBOs) through quantum dots have been intensively investigated. The amplitude of the CBOs can be modulated either by the coherent resonant tunnelling[1] or by the coupling between quantum dots.[2] The CBOs are periodic for single dot structures with a large number of electrons. As the number of electrons in the dot is reduced, the CBOs cannot be periodic. This can be more easily understood by adding electrons into the dot one by one from zero.[3] These experiments have been performed on III–V semiconductor materials.[4] Here we report the CBOs of Si single-electron transistors, operated above 4.2K.

We have combined the in-plane gate technique and the split-gate technique, and developed these into a nanoelectrode-pair technique.[5] By using this technique, we have fabricated Si single-electron transistors with in-plane point-contact metal (IPPCM) gates by using a self-aligned process. Point contacts were formed by etching a constriction with a designed length of 100nm and a width of 10–100nm. The effective width of the conducting area can be modified by biasing the IPPCM gates. The pattern was defined by conventional photolithography and mesa-etching.[5]

II. EXPERIMENTAL DETAILS

A (001) oriented p-type silicon-on-insulator (SOI) substrate, with 3Ωcm resistivity, prepared by the separation by implanted oxygen (SIMOX) technique was employed. First, a channel was realized by two etched trenches with a shape of point contacts by electron-cyclotron-resonance (ECR) plasma etching. Then the wafer was subjected to thermal oxidation in dry oxygen ambient. The oxidation was mainly used to increase the potential fluctuations in the channel. The thickness of the thermal oxide was about 10nm. By using a self-aligned process, IPPCM gates were deposited. This was realized by rotating the wafer to expose the two sides of the channel during its evaporation. A layer of silicon dioxide with a thickness of 80nm was deposited and finally a top metal gate was formed. The oxide layer was used to insulate the IPPCM gates and the top gate. Two-dimensional electron gas can be formed at the inversion layer by applying a positive voltage to the top gate, which is used to control the electrostatic potential of the SET dot. Several samples with designed channel widths ranging from 100 to 10nm were fabricated. Figure 1 shows the schematic view of the SETs with IPPCM gates. The threshold voltage shifts as the channel width is reduced. We applied a negative bias to the back-side substrate in order to fix the threshold voltages to zero. In this way, we tried to fix the electron number at this point to zero. This may be important in the study of the shell structures in "artificial atoms".[3]

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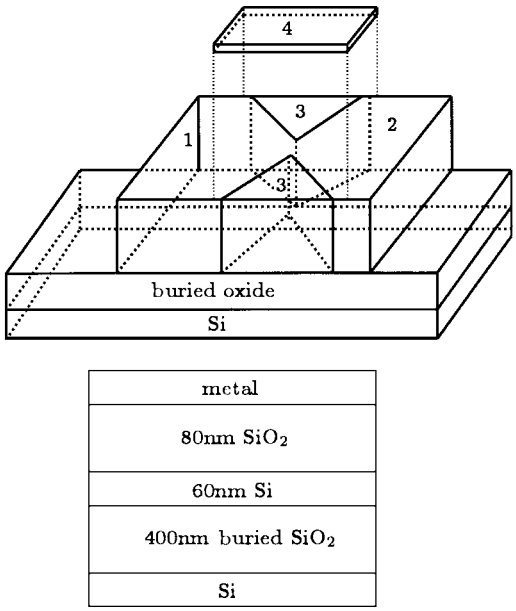


Fig.1. A schematic illustration of the fabricated device. The source and the drain are indicated by 1 and 2, the in-plane gates by 3, and the top gate by 4.

The CBOs of the single-electron transistors with wide channels exhibit irregular CBOs by setting V_3=0. With decreasing V_3, the CBOs become periodic. The Coulomb blockade staircases can only be clearly observed when the two barriers are asymmetric. The I_2–V_2 always shows single-electron switching at different values of V_4, which is called the Coulomb blockade effect. It has been found that the CBOs become more regular as the channel width is reduced. The observation of the irregular peaks and the Coulomb blockade effects is due to the single-electron tunnelling through the multiple-dot structure. Here, we discuss the CBOs of two devices with the channel widths of 80 and 30nm.

Ⅲ. RESULTS AND DISCUSSION

Figure 2 shows the CBOs under various values of V_{42}. At V_3=–0mV, I_2 oscillates and decreases significantly with scanning V_4. The amplitude of the background current changes a little at V_4 <5.0V for V_3=–90mV, and at V_4 <8.8V for V_3=–120mV. The sudden change in the amplitude of the background current is due to the reduced number of the current paths through the channel wire. At V_3=–150mV, the background current changes little with scanning V_4, and the CBOs are periodic at V_4 <8.8V.

Figure 3 shows the I_2 versus V_4 characteristic of the single-electron transistor with a 30nm wide channel at V_3=–60mV. I_2 oscillates with increasing V_4. These oscillations are confirmed to be the CBOs by the observation of clear Coulomb blockade effects. The oscillations are not strictly periodic. The fluctuations of the peak spacing are more serious in some region of the gate voltage V_4. The average period of the CBOs is about 0.55V. However, the last two peaks at 7.7 and 8.4V have a voltage separation of 0.70V. Also, the peaks at 1.0 and 1.7V have a voltage separation of 0.71V. There are also fluctuations of voltage shift between the other adjacent peaks. These fluctuations are probably related to the confinement effect of the dot and the noise level in our measurement.

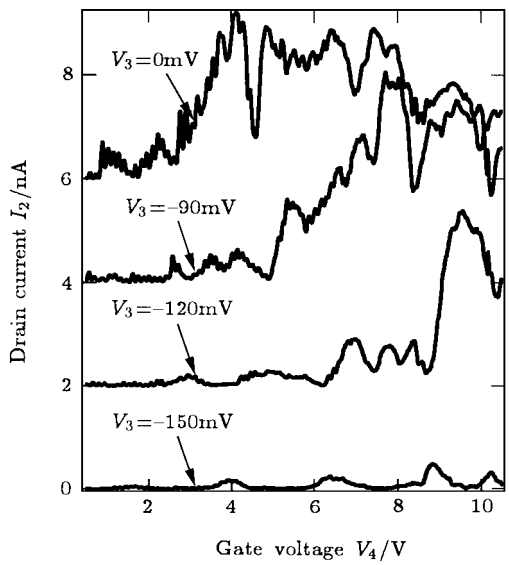


Fig.2. The I_2 versus V_4 characteristic of the device with a 80nm wide channel at V_2=1mV and T=4.2K with V_3=0, –90, –120, –150mV.

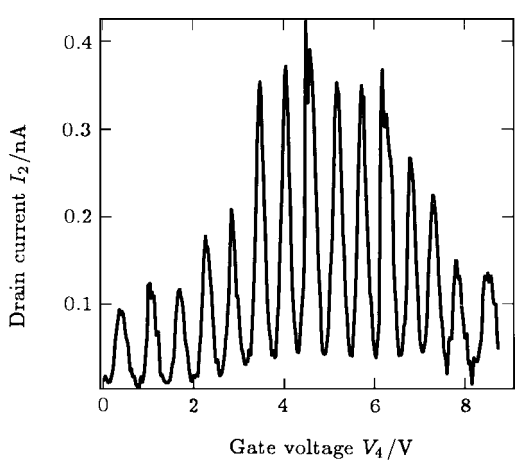


Fig.3. The CBOs of the devices with a 30nm wide channel at V_2=1mV, V_3=–60 mV, and T=4.2K.

In Fig.3, we have also observed a shift of the peak position as the temperature is raised. The shift in the range of temperature from 4.2 to 60K is small and can

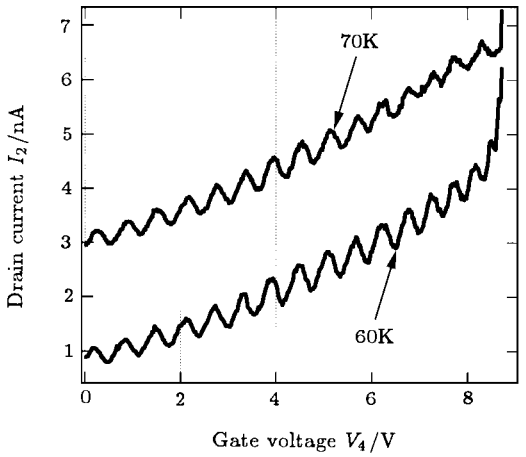


Fig.4. The CBOs of the devices with a 30nm wide channel at V_2=1mV, V_3=–60mV, and T=60 and 70K.

be neglected. However, the shift above 60K is large. Figure 4 shows the CBOs at 60 and 70K. At low temperatures, the source-drain conductance is determined by the tunnelling of the electrons with energies near the Fermi level. At high temperatures, the conductance is expected to be dominated by activated transport. The shift of the peak positions can also occur due to the charging in the nearby dots.[6] But this cannot be used to explain the data in Fig.4. We argue that the peak shift is due to the activated transport at high temperatures.

The formation of dots[7] could arise from: (1) thickness fluctuations of the SOI layer; (2) fluctuation of the channel width; (3) pattern-dependent oxidation; (4) strain produced by etching and oxidation; (5) localized states; (6) Si nanoparticles at the interface between the SOI layer and the buried oxide layer. These have been discussed in Ref.[7] and it was found that the considerable band gap shrinkage[8] from the oxidation-induced compressive strain probably accounts for the formation of the dots in our devices.

IV. SUMMARY

We have investigated the CBOs of Si single-electron transistors with in-plane point-contact metal gates. By applying negative voltages to the in-plane gates, these devices showed clear periodic CBOs. The peak position shifts with increasing temperature at high temperatures.

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