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HOT-CARRIER GENERATION MECHANISM AND HOT-CARRIER EFFECT IMMUNITY IN DEEP-SUB-MICRON GROOVED-GATE PMOSFETS*

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Based on the hydrodynamic energy transport model, immunity from the hot-carrier effect in deep-sub-micron grooved-gate p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs) is analysed. The results show that hot carriers generated in grooved-gate PMOSFETs are much smaller than those in planar ones, especially for the case of channel lengths lying in the deep-sub-micron and super deep-sub-micron regions. Then, the hot-carrier generation mechanism and the reason why grooved-gate MOS devices can suppress the hot-carrier effect are studied from the viewpoint of physical mechanisms occurring in devices. It is found that the highest hot-carrier generating rate is at a medium gate bias voltage in three stress areas, similar to conventional planar devices. In deep-sub-micron grooved-gate PMOSFETs, the hot-carrier injection gate current is still composed mainly of the hot-electron injection current, and the hole injection current becomes dominant only at an extremely high gate voltage. In order to investigate other influences of the hot-carrier effect on the device characteristics, the degradation of the device performance is studied for both grooved-gate and planar devices at different interface states. The results show that the drift of the device electrical performance induced by the interface states in grooved-gate PMOSFETs is far larger than that in planar devices.

Keywords: grooved-gate PMOSFETs, mechanism of hot-carrier generation, hot-carrier effect, interface states

PACC: 0750, 6170T, 7340Q, 7200

I. INTRODUCTION

As metal–oxide–semiconductor (MOS) devices are scaled down to the deep-sub-micron region, serious punch-through and short-channel effects, as well as hot-carrier effects, are encountered. In order to suppress these effects, many new device structures and processes are explored.[1–5] Among them, the grooved-gate MOS structure is proposed as the most promising candidate for the deep-sub-micron and super deep-sub-micron regions.[5–8] Some papers[5–8] have described the performance enhancements in this structure. However, the mechanism of its operation and the possibility of applying it to the deep-sub-micron regime are still unknown. On the other hand, current studies are focused on n-channel devices, and to our knowledge there are few studies on p-channel devices.

The hot-carrier effect is negligible in p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs) with long channels. However, as MOS devices are scaled down, the degradation of the drain current and transconductance increases significantly. Thus, the influence of degradation of PMOSFETs on CMOS circuits cannot no longer be ignored. It is necessary to study their characteristics and operation mechanisms.

Based on the hydrodynamic energy transport model, using the device simulation tool, Medici,[9] the immunity from the hot-carrier effect in grooved-gate PMOSFETs is studied first. Then our work is focused on the mechanism of hot-carrier generation in deep-sub-micron grooved-gate PMOSFETs. Finally, the degradation of device electric characteristics induced by the interface states of grooved-gate PMOSFETs is explored and compared with that of corresponding conventional planar ones.

II. HOT-CARRIER EFFECT IMMUNITY IN DEEP-SUB-MICRON GROOVED-GATE PMOSFETS

Figure 1 shows schematically the cross section of grooved-gate PMOSFETs. In our study, the source/drain junction depth is 0.02 μm above the bottom of the groove (forming a 0.02 μm negative junction). The bottom concave corner is 45°. The gate oxide thickness is 4 nm. The effective channel lengths are 0.05, 0.13, 0.50 and 0.80 μm, respectively. In all the

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simulated devices, the fixed interface state density is $10^{10}cm^{-2}$, the doping concentration of the substrate is $5.0\times10^{16}cm^{-3}$, and the maximum doping concentration at the surface is $6.0\times10^{18}cm^{-3}$ for source/drain region. The groove depth is $0.1\,\mu m$. The parameters in planar devices are the same as those described above.

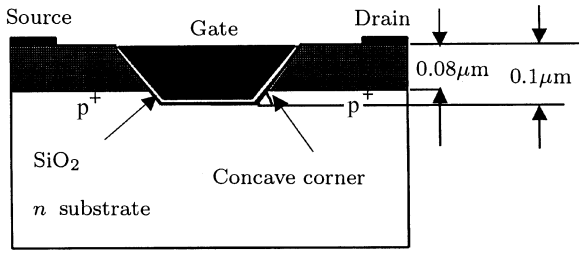


Fig.1. Schematic diagram of grooved-gate PMOSFETs.

The gate current is considered as a good criterion of hot-carrier reliability in small size PMOSFETs. Figure 2 shows the hot-carrier injection gate current [HE(gate)] for grooved-gate and conventional planar PMOSFETs with different channel lengths. It is clear that the hot-carrier effect increases obviously in both structure devices with the decrease of the channel length. But the immunity from the hot-carrier effect in grooved-gate devices is much better than that in planar ones because the gate current of the former is far smaller, especially in short-channel devices. When the channel length is $0.05\,\mu m$, the maximal gate current in grooved-gate devices is 1.54% of that in planar ones. When the channel length is $0.80\,\mu m$, the corresponding parameter is 15.1%. The simulation results also indicate that, in grooved-gate devices with different channel lengths, the gate current reaches its peak value at almost the same gate voltage, which is a little lower than the half drain voltage. This demonstrates that the hot-carrier generation rate reaches its peak at this point. In planar devices, although similar to the grooved-gate ones, this voltage value decreases slightly as the channel length decreases. This is mainly because, with the decrease of the channel length, the electric field in the channel is increased and the electron velocity evidently increases, so the amount of injected hot carriers reaches its peak at a low bias voltage. This implies that the short-channel effect is more serious in planar devices.

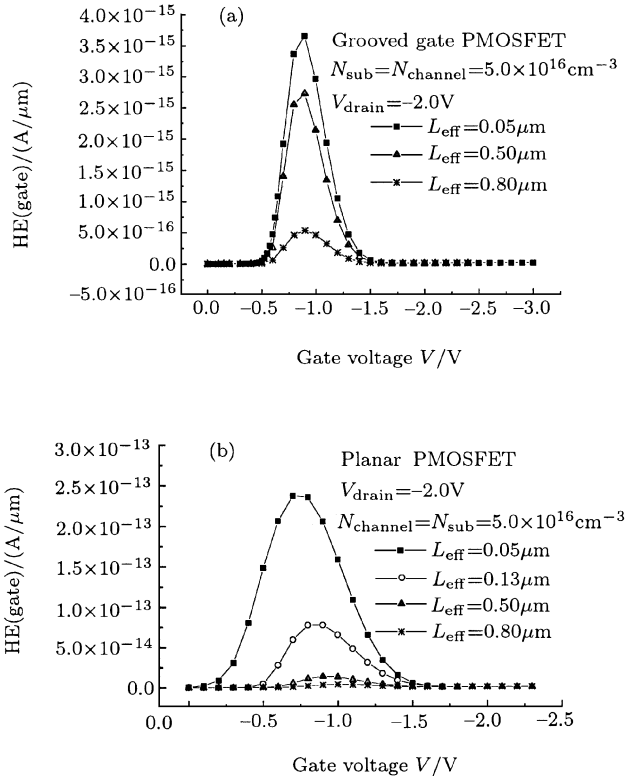


Fig.2. Hot-carrier injection gate currents in (a) grooved-gate and (b) conventional planar PMOSFETs with different channel lengths.

The corner effect is the basic reason why the hot-carrier effect is smaller in grooved-gate devices. There is one potential barrier formed at each concave corner. While the carriers move to the drain electrode, they have to not only surmount the potential barriers, but also change their moving directions. Therefore, the impact ionization generation rate is far smaller than that in planar devices. A low impact ionization rate brings about a small gate current, showing a good immunity from the hot-carrier effect in grooved-gate devices. In addition, the current lines are dispersed in them because the longitudinal electric field near the drain is inversed. So the carriers are far away from the gate, and it is difficult for them to get to the gate. Thus, the hot-carrier injection gate current is further decreased.

III. MECHANISM OF GENERATION OF HOT-CARRIER EFFECT IN GROOVED-GATE PMOSFETS

In this section, using grooved-gate devices with a $0.13\,\mu m$ channel length as an example, we discuss the distribution of some physical parameters related to the hot-carrier effect and analyse the hot-carrier effect generation mechanism. Figure 3 shows the distribution of the parallel component of the electric field

along the current intensity direction at different gate voltages. It shows that the potential barriers of the parallel component increase with the increase of the gate voltage. Besides the transverse electric field, there are other two factors affecting the hot-carrier effect. One is that the hot-carrier injection gate current increases with the increase of the gate voltage, since it is easy for the carriers to arrive at the interface and to get to the gate through the gate oxide layer. The other is that the amount of hot carriers decreases with the increase of the gate voltage because of the higher potential barrier. The interaction of these three factors causes the hot-carrier injection gate current to reach its peak value at a certain gate voltage near the medium voltage stress area. This means that most hot carriers are generated in the medium voltage stress area.

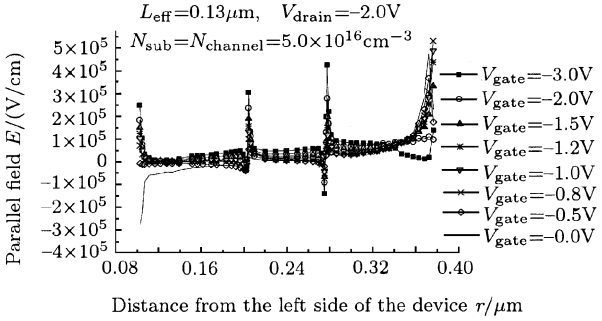


Fig.3. The parallel component of the electric field distribution along the Si/SiO_2 interface in grooved-gate PMOSFETs at different gate bias voltages.

Figure 4 shows the hot-electron mean velocity distribution along the Si/SiO_2 interface. It is obvious that the electron velocity reaches its maximum almost at the medium gate voltage stress region ($V_{\rm gate} \approx 0.5V_{\rm drain}$), which coincides with the above analyses for the hot-carrier generation rate.

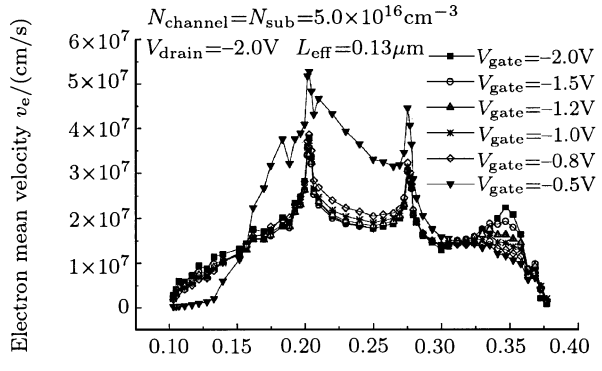


Fig.4. The hot-electron mean-velocity distribution along the Si/SiO_2 interface in grooved-gate PMOSFETs at different gate voltages.

Figure 5 shows the total hot-carrier and electron injection gate current in grooved-gate PMOSFETs at different gate voltages. It manifests that the hot-carrier injection current is composed mainly of the hot-electron injection current and almost the total of the injection occurs in the region near the drain. It also can be found that the hole injection current plays an important role only at an extremely high gate voltage, but it is nearly 20 orders smaller than that of hot electron at the general gate voltage stress. From the above analyses, we can conclude that, in deep-sub-micron grooved-gate PMOSFETs, the hot-carrier damage at a normal gate voltage is mainly induced by the hot-electron injection and occurs near the drain, and the damage induced by the hot-hole injection plays an important role only at an uttermost high gate voltage. In addition, it is proven that the damage rate is the largest when the gate voltage is about half of the drain voltage.

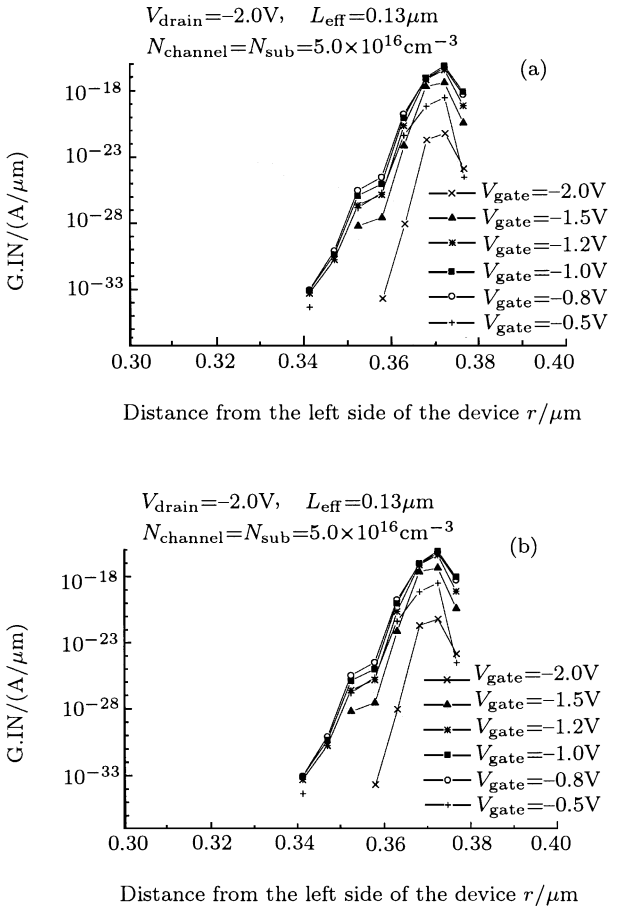


Fig.5. Hot-carrier injection gate current initiated from each point in A/μm versus distance along the Si/SiO_2 interface through the device in grooved-gate PMOSFETs: (a) hot-electron injection gate current; (b) total hot-carrier injection gate current.

IV. THE DEGRADATION INDUCED BY INTERFACE STATES IN DEEP-SUB-MICRON GROOVED-GATE PMOSFETS

Although the amount of hot carriers generated in grooved-gate devices is much smaller than that in planar ones, one may ask whether the degradation induced by hot carriers is smaller. We will discuss that in this section.

It is known that there are three hot-carrier degradation mechanisms in deep-sub-micron PMOSFETs.[10] The interface state generated by the hot-carrier injection influences the device performance strongly. Fast interface states are classified as donor or acceptor of electrons (n) or holes (p). At first, we analyse the influence of acceptor interface states on the characteristics of PMOSFETs.

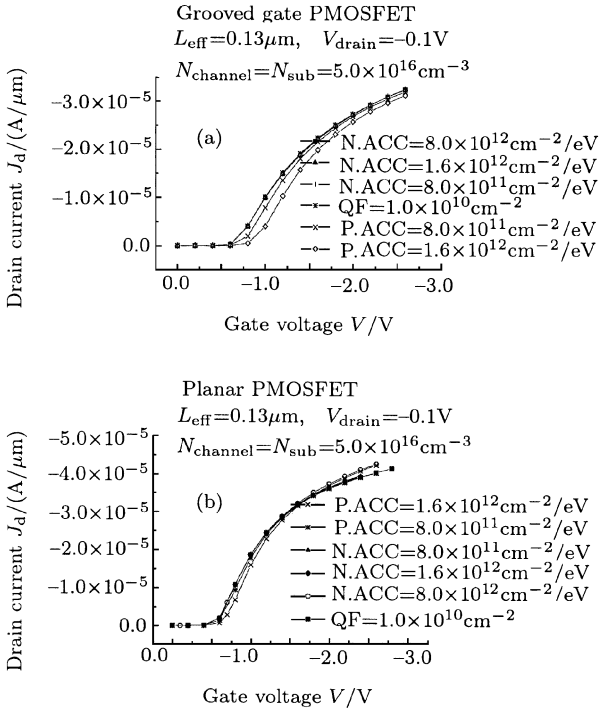


Fig.6. Gate characteristics for (a) grooved-gate and (b) conventional planar PMOSFETs with different acceptor interface state densities in the region near the drain.

Figure 6 gives the gate characteristics of grooved-gate and planar PMOSFETs when some electron and hole acceptor interface states are put on their interface near the drain region. The drift of gate characteristics can be observed clearly in Fig.6. The results show that the drift of the gate characteristics in grooved-gate PMOSFETs is larger than that in planar ones at the same interface state density, and the drift of the gate characteristics induced by the hole acceptor interface states is larger than that induced by the electron interface states with the same density in both structure devices. The gate characteristics curve moves to the right evidently as the hole acceptor interface state density (P.ACC) increases, which leads to the rapid increase of the threshold voltage and sub-threshold swing factor, and brings on significant degradation in sub-threshold characteristics. However, the transconductance characteristics are improved. This is because, with the injection of hot carriers into the interface near the drain region and the accumulation of the positive charge (hole acceptor interface states), a repulsive force is acting on the majority of carrier holes. It also can be deduced that the drain current driving capability would be degraded with the increase of the hole acceptor interface state density, which is confirmed by our following studies. On the contrary, the electron acceptor interface states cause the gate characteristics to shift towards the left and the threshold voltage is reduced slightly. The reason is that, with the accumulation of the negative charge (electron acceptor interface) in the interface near the drain, an attractive force is exerted on the holes, which makes the drain region extend into the channel and shortens the effective channel length. The drain current driving capability would be improved for the same reason. The influence of interface states on the planar device characteristics can be explained likewise.

Figure 7 shows the drain characteristics curves at different interface states for grooved-gate and planar PMOSFETs. The simulation results manifest that, in both structure devices, the maximum saturation drain current is decreased due to the effect of the hole acceptor interface states. The influence of electron interface states on the drain characteristics is opposite to that of the hole type. Similar to the effect on the gate characteristics, the shift of the drain characteristics induced by the hole acceptor interface states is larger than that induced by the electron acceptor interface states with the same density, and the drift of the drain characteristics caused by the same interface states in grooved-gate PMOSFETs is much larger than that in planar ones.

Furthermore, we have also analysed the effect of donor interface states on the device characteristics. Our study proves that the influence of the hole donor interface states on the characteristics is far smaller than that of the electron donor interface states, and the drift of the characteristics in grooved-gate PMOSFETs is larger than that in planar ones at the same interface state density. The influence of the electron

donor interface states is similar to that of the hole acceptor interface states, or inversely, the influence of the hole donor interface states is similar to that of the electron acceptor interface states.

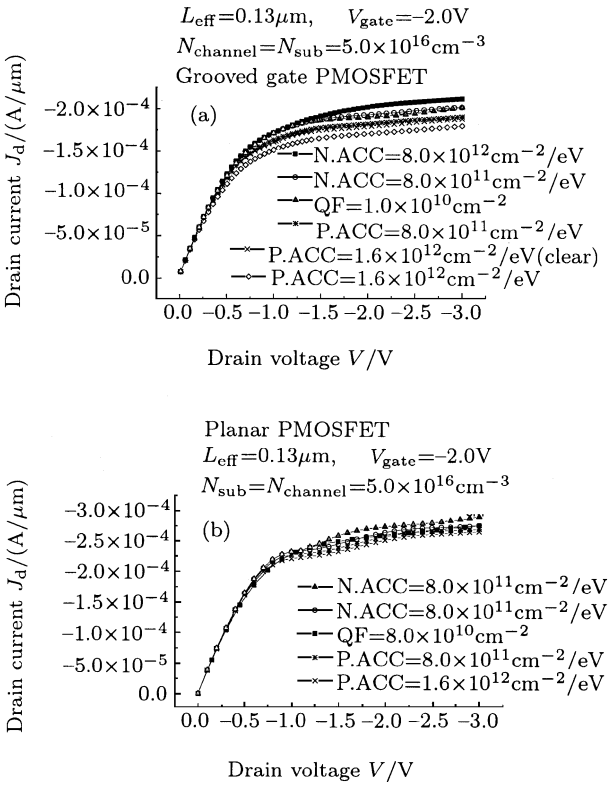


Fig.7. Drain characteristics for (a) grooved-gate and (b) conventional planar PMOSFETs with different acceptor interface state densities in the region near the drain.

V. DISCUSSION AND CONCLUSION

Firstly, the hot-carrier effect in grooved-gate and planar devices has been explored. The research results prove that, compared with planar devices, grooved-gate devices can suppress the hot-carrier effect deeply, especially for the case of short-channel ones. Although the hot-carrier effect in grooved-gate devices is small, our study finds that the influence of the same interface states on characteristics of grooved-gate devices is much larger than on those of planar ones, since there are less hot carriers generated in grooved-gate devices, and the immunity of devices from the hot-carrier effect is still better than the planar devices. So the grooved-gate structure is beneficial to improving the performance and the immunity from hot-carrier effect in deep-sub-micron and super deep-sub-micron regions.

Secondly, the mechanism of the hot-carrier generation in deep-sub-micron grooved-gate PMOSFETs is analysed. From the results, we can conclude the following. 1) Similar to planar devices, in grooved-gate devices the generation of hot carriers is related to the bias voltage directly and the hot-carrier effect also reaches its peak at a medium gate voltage. 2) In deep-sub-micron PMOSFETs, usually the main component of the hot-carrier injection gate current is the hot-electron injection current, but it is the hole injection current at a very high gate voltage. 3) The hole injection current at a very high gate voltage is far smaller than the electron injection current at a low gate voltage.

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