
# Heavy-ions-induced failure mechanisms and structural damage in SiC MOSFETs under complex irradiation conditions

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# Heavy-ions-induced failure mechanisms and structural damage in SiC MOSFETs under complex irradiation conditions

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The failure mechanisms and structural damage of SiC MOSFETs induced by heavy ion irradiation were demonstrated. The findings reveal three degradation modes, depending on the drain voltage. At a relatively low voltage, the damage is triggered by the formation and activation of gate latent damage (LDs), with damage concentrated in the gate oxide. The second degradation mode involves permanent leakage current degradation, with damage progressively transitioning from the oxide to the SiC material as the drain voltage escalates. Ultimately, the device undergoes catastrophic burnout above certain voltages, characterized by the lattice temperature reaching the sublimation point of SiC, resulting in surface cavity and complete structural destruction. This paper presents a comprehensive investigation of SiC MOSFETs under heavy ion exposure, providing radiation resistance methods of SiC-based devices for aerospace applications.

**Keywords:** heavy ion irradiation, silicon carbide (SiC) MOSFETs, structural damage, failure mechanism

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## 1. Introduction

As lunar exploration and sampling missions increasingly demand higher performance from spacecraft, silicon carbide (SiC) power devices are expected to replace silicon counterparts.[1–3] This is due to their superior critical breakdown field strength, wide energy bandgap and high thermal conductivity, which enable the development of the whole electronic system towards more lightweight, compact, and lower power consumption.[4]

Current research indicates that SiC MOSFETs exhibit insensitivity to total ionizing dose (TID) effects.[5] In radiation-intensive environments, these devices can still remain functionality at the radiation dose reaching 300 krad (Si).[6] However, a critical barrier to their adoption in space applications stems from single-event effects (SEE) caused by high-energy heavy ions.[7] Notably, the occurrence of SEE and associated degradation modes exhibit a strong dependence on drain voltage levels.[8] When operating below 40% of the rated voltage, SiC MOSFETs suffer catastrophic single-event burnout (SEB), causing complete loss of electrical characteristics.[9,10] At approximately 20% of the rated voltage, single-event leakage current (SELC) occurs,[11] creating irreversible leakage paths that lead to a permanent increase in leakage current during irradiation exposure. Even with voltage reduction, maintaining safe operating area (SOA) remains challenging. Recent studies reveal that despite no noticeable change in leakage current during irradiation, latent damages (LDs) are still introduced at sensitive locations of the device.[12,13] These LDs can evolve under post-irradiation gate stress (PIGS), leading to premature oxide breakdown.[14] Such damage from complex irradiation conditions compromises system reliability and raises concerns regarding SiC MOSFETs operational stability.

To date, the ion-induced degradation patterns have been identified. However, due to incomplete damage morphology characterization, corresponding failure mechanisms and sensitive regions remain insufficient. Additionally, the potential correlations between these degradation modes have not been discussed.

In this study, the heavy ion-induced failure mechanisms and corresponding damage morphology of SiC MOSFETs under different drain voltages were systematically investigated. Through comprehensive electrical analysis, the device degradation behavior was characterized, and scanning electron microscopy (SEM) was employed to examine the failure morphology, thereby providing insights into single-event hardening strategies for SiC MOSFETs.

## 2. Samples and experimental setups

Devices under test (DUTs) are commercial planar SiC MOSFETs manufactured by CETC Co., Ltd., exhibiting a die area of approximately 3.13 mm×3.69 mm. Moreover, samples employ a strip-cell architecture, with the cell pitch of approx-

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imately 9 μm. Figure 1 shows the cross-sectional SEM view and schematic diagram of the sample. DUTs have a maximum breakdown voltage of approximately 1560 V measured by Keithley source meters. The epitaxial layer thickness is about 10 μm and the gate oxide thickness is about 50 nm. Samples were packaged in TO-257 housings featuring open-cavity surfaces to enable ion penetration while minimizing energy loss.

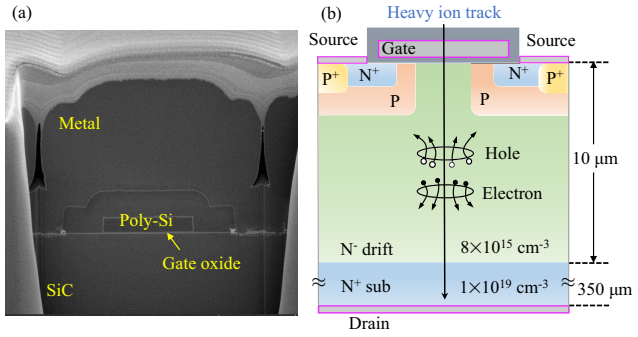


**Fig. 1.** (a) SEM cross-sectional view of the devices used in this experiment. (b) Schematic view (not in scale) of the SiC MOSFET.

The irradiation experiments were conducted at the Space Environment Simulation Research Infrastructure (SESRI) of Harbin Institute of Technology. The accelerator operated in pulsed mode with 12-second cycles (3-second exposure windows), delivering an average ion flux of about $1.5\times1^4$ ions/cm$^2$·s. $^{73}$Ta ions with 1864-MeV energy were used, exhibiting a linear energy transfer (LET) of $\sim$80.7 MeV·cm$^2$/mg and a penetration depth of 70.2 μm (SiC), exceeding the device's epitaxial layer thickness. Keithley 2470 and 2450 source meters provided bias voltages and monitored current in real-time. Moreover, the experiments were conducted at room temperature and under atmospheric conditions, and the setup is shown in Fig. 2.

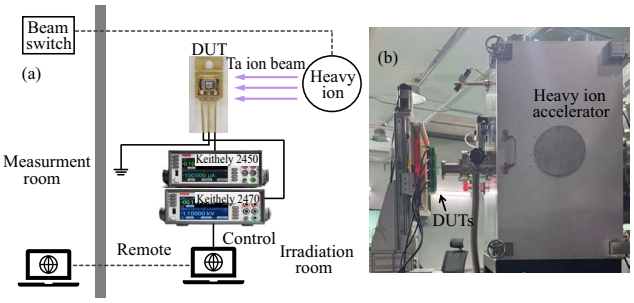


**Fig. 2.** (a) Schematic diagram of the on-line testing systems. (b) Experimental setup.

During irradiation, two experimental protocols were implemented. The first involved stepwise drain voltage ramping to assess degradation behaviors and determine the device's failure voltage. Under this protocol, the gate voltage ($V_{GS}$) was fixed at 0 V while the drain voltage ($V_{DS}$) was swept from 0 V to 600 V in 10-V increments, with each voltage level held for 12 s to synchronize with the ion pulse cycle. The test terminated when the drain current reached 100 mA. The second protocol employed constant drain voltage testing at the failure voltage identified from the first experiment, enabling investigation of the corresponding failure mechanisms.

## 3. Results and analysis

### 3.1. Stepwise-increase drain voltage results

Figure 3 depicts the evolution of $I_D$ and $I_G$ as a function of drain bias during irradiation, the total fluence is $6.75\times10^6$ ions/cm$^2$. It can be seen that the current behavior is typical for SiC MOSFETs, which exhibits three distinct regions:[15] (i) charge collection: from 0 V to 100 V, where both the $I_D$ and $I_G$ remained significantly unchanged despite increasing drain voltage; (ii) SELC: from 100 V to 52 V, where permanent current degradation occurs during irradiation, indicating the presence of ion-induced leakage path in the device, which can be further divided into SELC I with $I_D = I_G$ and SELC II with $I_D > I_G$; (iii) catastrophic SEB over 520 V.

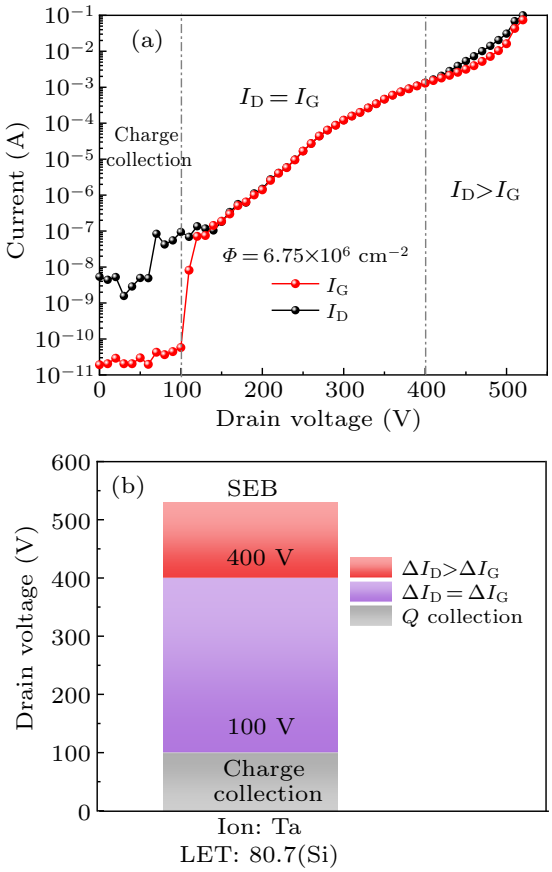


**Fig. 3.** (a) Evolution of the $I_D$ and $I_G$ as a function of drain bias during irradiation, (b) failure voltage distribution of the tested device.

Figure 4(a) illustrates the post-irradiation drain-blocking characteristics. It is evident that both gate and drain current exhibit significant degradation compared to pre-irradiation values. Notably, $I_D$ is equal to $I_G$ at low drain bias, and $I_D$ begins to exceed $I_G$ when the drain bias surpasses the specific threshold of 20 V, suggesting the presence of D–G and D–S leakage paths after irradiation. Similarly, as shown in Fig. 4(b), the

post-irradiation gate leakage characteristics reveal a consistent degradation trend of $I_D$ and $I_G$, reflecting the ion-induced oxide damage is located above the JFET region, which does not involve additional G-S leakage path.

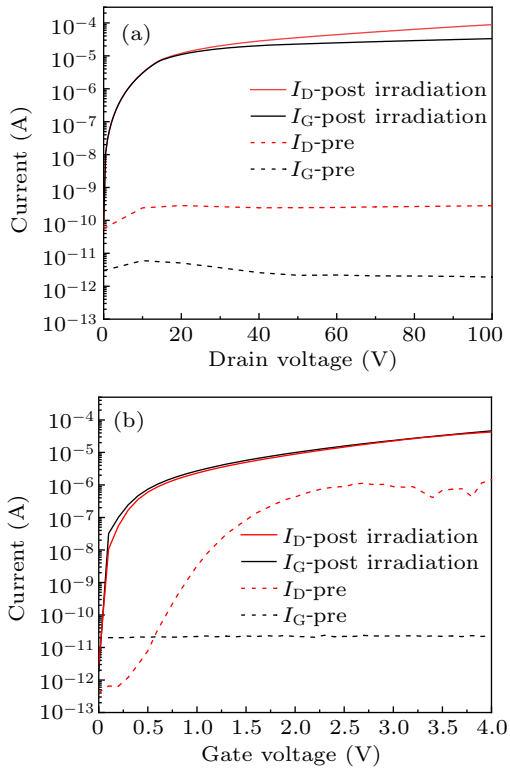


**Fig. 4.** (a) Post-irradiation blocking characteristics, (b) post-irradiation gate leakage characteristics.

### 3.2. Constant drain voltage results

#### 3.2.1. Under low drain bias (90 V)

DUT-1 was exposed under a 90-V drain bias with a total ion fluence of $\sim 1.57 \times 10^5$ cm$^{-2}$. As shown in Fig. 5(a), transient gate leakage current spikes were observed in DUT-1, corresponding to ion-induced charge collection. Notably, $I_G$ returned to pre-irradiation levels after beam termination, suggesting intact gate oxide integrity during irradiation.

Following irradiation, PIGS test was performed on DUT-1 to investigate the effect of gate LDs and assess the gate oxide integrity. The test employed a gate voltage sweep from 0 V to 25 V in steps of 0.1 V, with a 100-μA gate current compliance. In Fig. 5(b), it can be seen that the gate oxide suffers transient breakdown at $V_{GS} = 12.5$ V, which is significantly lower than the oxide breakdown voltage prior to irradiation. This observation suggests that heavy ion irradiation has introduced LDs in the gate oxide along the incident trajectory. The blocking characteristics after oxide breakdown in Fig. 5(c) revealed that both $I_G$ and $I_D$ exhibit identical trends with increasing drain voltage, indicating the formation of permanent leakage path from gate to drain, which confirms that the oxide damage is located above the JFET region.[16]

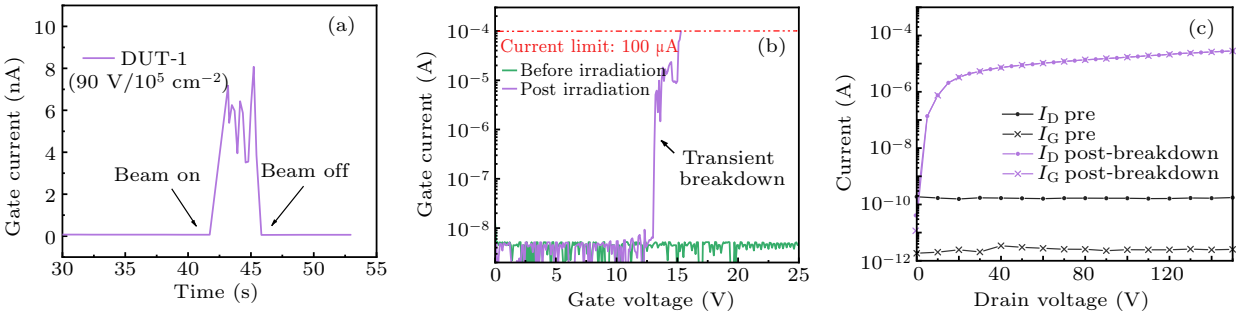


**Fig. 5.** (a) Variation of $I_G$ as a function of time during irradiation for DUT-1, (b) PIGS results of DUT-1 after irradiation, (c) blocking characteristics of DUT-1 after oxide breakdown.

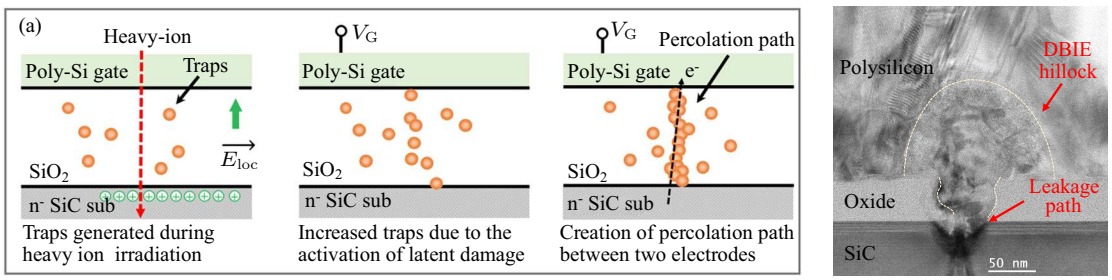


**Fig. 6.** (a) Schematic diagram of gate oxide damage evolution mechanisms during PIGS test, (b) detailed gate oxide damage morphology.

Figure 6(a) illustrates the schematic diagram of gate oxide damage evolution mechanisms during PIGS test. The LDs originating from transient electric field generated by hole accumulation at the SiC/SiO$_2$ interface.[17] When gate voltages are applied across the oxide, these LDs become progressively activated through the stretching and breaking of weakened Si–O bonds, thereby leading to the increase of localized latent damage sites. Upon the trap densities reach the critical threshold, a percolation path forms between the gate and SiC epilayer, triggering gate oxide breakdown, corresponding to the

abrupt increase of $I_G$ in Fig. 5(b).

The detailed oxide damage morphology is shown in Fig. 6(b), revealing concentrated gate oxide failure path, which serves as the primary sensitive site under low-drain-voltage irradiation conditions. Additionally, a hillock is found in the poly-Si gate region, which is attributed to the dielectric breakdown induced epitaxy (DBIE) effects, where melted atoms undergo migration and re-nucleation along the oxide leakage path.[18]

### 3.2.2. Under medium bias (350 V and 450 V)

To investigate the SELC I effect, DUT-2 was irradiated under a medium drain bias of 350 V, with a total fluence of $\sim 1\times10^6$/cm$^2$. As shown in Fig. 7(a), unlike the transient current pulse observed in Fig. 5(a), DUT-2 exhibits stepwise current increases during ion strikes, indicating the formation of direct leakage path during irradiation. These progressive current steps are caused by individual ion impacts. Furthermore, the gate and drain currents show identical magnitudes, confirming the ion-induced leakage path resides within the oxide layer. Figure 7(b) shows the post-irradiation gate leakage current evolution, which reveals a continuous growth of $I_G$, where the oxide suffers a complete destruction. In Fig. 7(c), blocking characteristics is similar to DUT-1 but exhibit severely degraded performance. This reflect that the SELC I damage was consistent with PIGS failure, but exhibited a more exacerbated pattern under the medium-drain-voltage irradiation conditions.

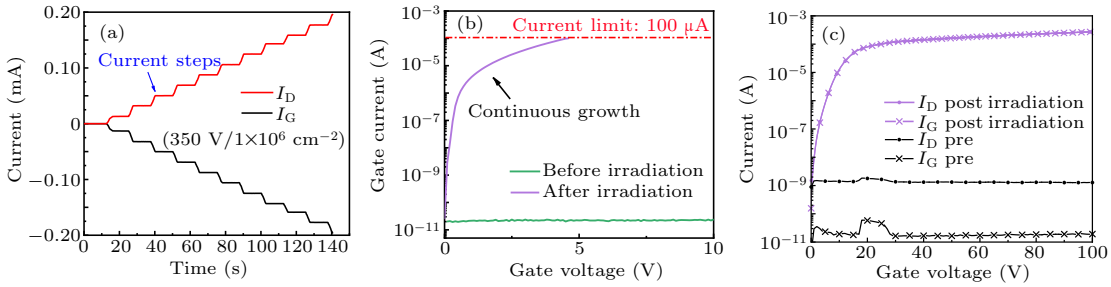


**Fig. 7.** (a) Variation of $I_G$ and $I_D$ as a function of time during irradiation for DUT-2, (b) post-irradiation gate leakage characteristics, (c) post-irradiation blocking characteristics.

To investigate the SELC II effect, DUT-3 was irradiated under an elevated drain voltage of 450 V, with a total ion fluence of $\sim 1.94\times10^5$/cm$^2$. As shown in Fig. 8(a), the drain current surges three times larger than gate current after irradiation, indicating that the high drain bias not only sustains the G–D leakage path but also induces an additional leakage path. Furthermore, drain current exhibit a slight increase after beam termination, suggesting an unstable state of the device, which may be related to the ion-induced localized thermal instability. In Fig. 8(b), the post-irradiation gate voltage collapses to approximately 3 V at a 100-μA current limit. Notably, the post-irradiation blocking characteristics in Fig. 8(c) reveal a distinct current behavior from DUT-2, where the $I_D$ and $I_G$ were equal at low $V_{DS}$, and $I_D$ began to exceed $I_G$ at high $V_{DS}$. This differential behavior suggests that compared to SELC I, in addition to oxide, SELC II damage transitioning to the SiC p–n junction, resulting in a more severe degradation of $I_D$ compared to $I_G$.[19,20]

Figure 9 reveals the SEM cross-sectional view of DUT-3, which is obtained from the gate EMMI hotspot. It can be seen that the damage was not only in the oxide, but cracks between source metal and insulator layer deposition (ILD) interface also exists, which is attributed to the current crowding effects.[21] While these interfacial cracks do not directly contribute to $I_D$ degradation, which stems from permanent structural modification in the SiC p–n junction. However, the corresponding SEM cross-sectional view from the drain-EMMI hotspot is not observed, which may be related to the localized lattice temperature is insufficient directly induce SiC damage, and presence in the form of permanent extended defects (ED), such as different dislocations, stacking faults, and so on.[22]

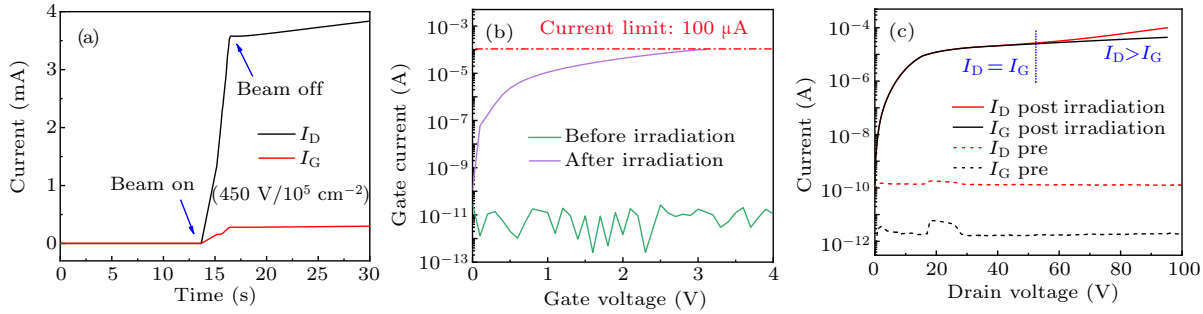


**Fig. 8.** (a) Variation of $I_G$ and $I_D$ as a function of time during irradiation for DUT-3, (b) post-irradiation gate leakage characteristics, (c) post-irradiation blocking characteristics.

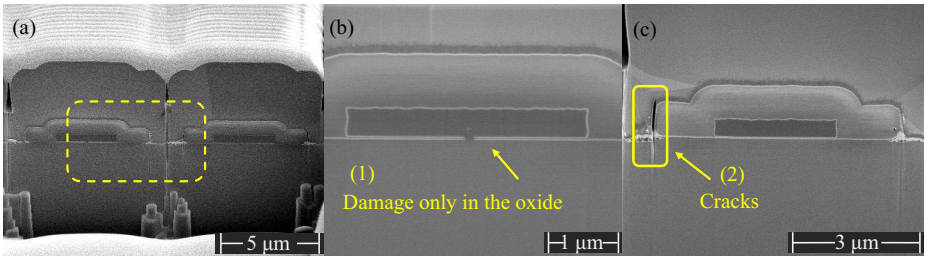


**Fig. 9.** (a) Detailed damage morphology characterization of DUT-3, (b) oxide damage, (c) interfacial cracks between ILD and source metal.

### 3.2.3. Under high bias (600 V)

Figure 10 plots the drain and gate leakage currents as a function of time during irradiation. The drain voltage was set to 600 V to investigate the SEB effects. During irradiation, two devices were irradiated with distinct drain current limits: 10 mA at DUT-4 and 100 μA at DUT-5. This experimental design aimed to evaluate the SEB degradation behaviors through controlling the localized thermal effects during ion strikes, enabling comparative analysis of failure mechanisms under high-drain-bias conditions.

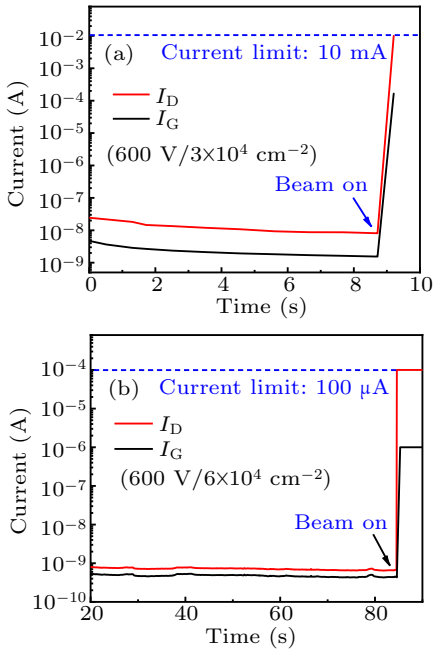


**Fig. 10.** Drain and gate leakage currents as a function of time during irradiation: (a) DUT-4 with 10-mA limits and (b) DUT-5 with 100-μA limits.

Figure 11 depicts the post-irradiation blocking characteristics of DUT-4 and DUT-5. For DUT-4, the resistor-like current behavior is observed, which is indicative of a typical burnout effect. In contrast, when the ion-induced drain current is reduced to 100 μA, DUT-5 shows degradation trends analogous to DUT-3, confirming damage is dominated by the SELC II modes. Consequently, SEB originates from SELC II degradation and are further intensified under electrothermal stress conditions.

Figure 12 presents the post-irradiation gate leakage characteristics of DUT-4 and DUT-5. For DUT-4, the gate current demonstrated a linear dependence on gate bias, indicating complete gate oxide failure due to the occurrence of SEB. In contrast, DUT-5 exhibited similar gate current behaviors to SELC modes, with $I_G$ remaining several orders of magnitude lower than DUT-4 at same gate bias. This divergence reflects that the controlling the ion-induced current amplitudes effectively governs damage severity.

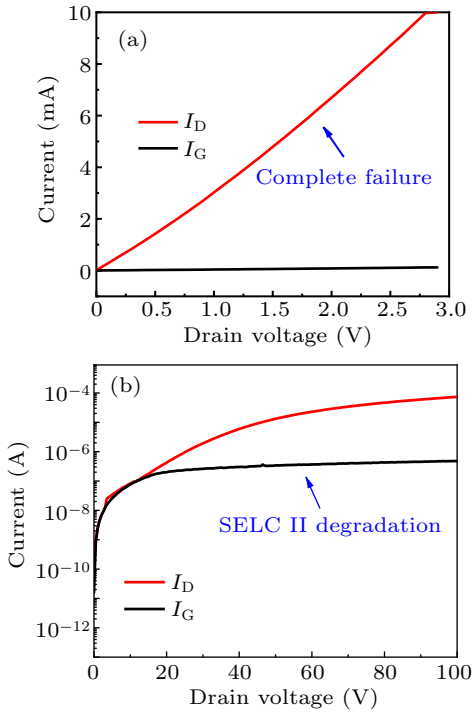


**Fig. 11.** Blocking characteristics after irradiation: (a) DUT-4 with 100-mA limits, (b) DUT-5 with 10-μA limits.

When a complete SEB occurs, significant morphological alterations are observed on the die surface, as depicted in Fig. 13(a). The SEB damage is induced by micro-explosion, where rapid thermal decomposition of the SiC lattice results in cavity formation. In Fig. 13(b), the deepest cavity is located at the source contact of the device, which is main location for ion energy deposition. The cavity generated by the damage extends over more than two gate stripes, measuring approximately 30 μm in length and 20 μm in width. Cross-sectional analysis reveals that the damage was mainly confined to epi region, reaching a maximum depth of around 15 μm, with a slightly extension into the substrate, as shown in Fig. 13(c). This damage profile creates a drain-to-source short circuit, resulting in irreversible device failure. More-

over, thermo-mechanical stresses from cavity expansion induce cracks at the N–N junction,[12,23,24] further exacerbating lattice structural integrity.

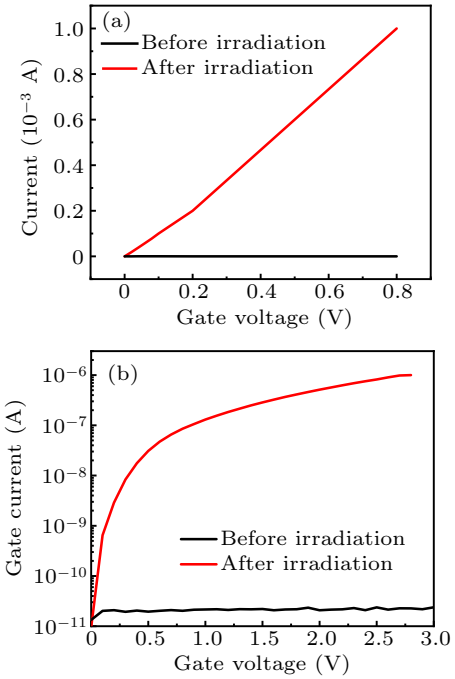


**Fig. 12.** Gate leakage characteristics after irradiation: (a) DUT-4 with 10-mA limits, (b) DUT-5 with 100-μA limits.

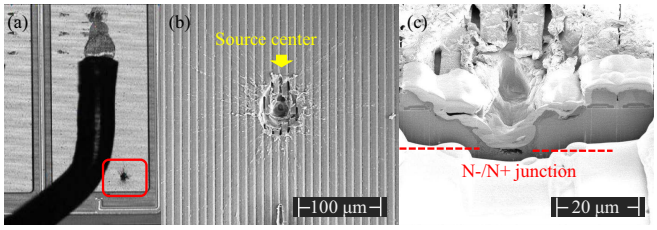


**Fig. 13.** (a) EMMI results of SEB damage for DUT-5, (b) magnification view of the surface damage, (c) SEM cross-sectional view of SEB damage.

### 3.2.4. TCAD simulations

To investigate the internal dynamics during ion strikes, TCAD simulations were performed using a structure and parameters identical to the DUTs shown in Fig. 1. The physical models are based on previous papers,[8,10] including Incomplete Ionization, Enormal for mobility, Auger and SRH for generation and recombination, Okuto–Crowell for avalanche, and thermodynamic considering the thermal distribution. Simulations modeled ion incident vertically from the center of the device using an LET value of 0.54 pC/μm. The temporal profile featured a Gaussian distribution peaking at 5 ps, with a radial distribution of 0.05 μm. Throughout the irradiation process, the ion-induced oxide electric field and lattice temperature are examined.

Figure 14(a) depicts the evolution of maximum oxide electric field under varying drain voltages, which influences the oxide integrity. The oxide electric field exhibits a significant increase during ion strikes, with the peak value occurring at 10 ps. Notably, the peak electric field magnitude increases with higher drain voltages. Under 90-V bias, the peak filed is about 10.7 MV/cm, which is insufficient to trigger oxide rupture but leads to the formation of LDs in the gate oxide. Conversely, when the drain bias exceeds 350 V, the peak field raises to 30.2 MV/cm, well surpassing the critical breakdown field strength of approximately 12 MV/cm. As a result, the oxide has been damaged during irradiation, accompanied by a notable increase in gate current.

Figure 14(b) illustrates the evolution of maximum lattice temperature under varying drain voltages, which influences the SiC lattice integrity. The lattice temperature evolves on a nanosecond timescale, occurring later than the electric field dynamics. For drain biases below 600 V, the highest temperatures remain below the SiC sublimation point of 3000 K and return to initial levels after several hundred nanoseconds or longer. This indicates that the SiC lattice remains intact and SEB is not triggered under low-to-medium bias conditions, even when the oxide damage has already occurred.

To further explore the distribution of hotspots that determining the device failure under 600-V bias, the lattice temperature distribution at 100 ns is shown in Fig. 14(c). It can be seen that two isolated hotspots emerge, which are located at the N–N junction and the gate/source surface corner, respectively. The temperature at the corner is about 1800 K while at the junction is 3000 K. The combination of these two hotspots lead to the final burnout of the device. Furthermore, the critical temperature in the junction induces transient decomposition of SiC lattice, causing micro-explosion effects that generate a damage hole at the surface of the chip.

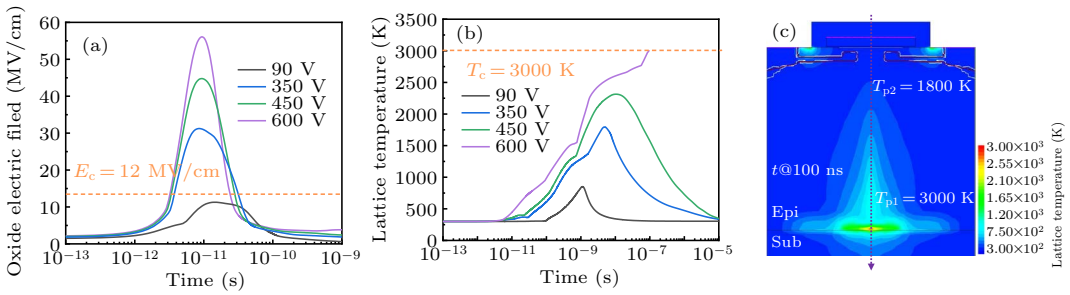


**Fig. 14.** Evolution of the ion-induced physical parameters under varying drain voltages: (a) maximum oxide electric field, (b) maximum lattice temperature, (c) spatial distribution of lattice temperature at 600 V after 100-ns striking.

## 4. Discussion

The above results demonstrate that the heavy ion-induced damage in SiC MOSFETs exhibit significant dependence on the drain voltage.

(i) Under low drain bias levels (10%–20% of the rated voltage), the failure mode is identified as gate LDs, characterized by negligible current degradation during irradiation but premature oxide breakdown under subsequent PIGS test. In this mode, the sensitive region identified in the oxide above the JFET region.

(ii) Under medium drain bias levels (20%–40% of the rated voltage), SELC occurs, characterized by current degradation during ion strikes. Based on the drain/gate current magnitudes, the damage is further divided into SELC I and SELC II. A detailed comparison of these two modes is provided in Table 1.

(iii) Under high drain bias levels (above 40% of the rated voltage), catastrophic SEB is trigged, resulting in complete device failure. Post-failure analysis reveals significant damage voids at the die surface and complete loss of functionality.

Moreover, these three degradation modes exhibit progressively severe damage patterns, as shown in Fig. 15. For gate LDs and SELC I, the gate oxide is particularly vulnerable, with SELC-I representing an escalated damage manifestation of gate LDs. In contrast, when degradation transitions to SELC-II under medium-to-high drain bias, the sensitive region extends beyond the oxide into the SiC material, where SEB is identified as a more exacerbated pattern of SELC II effects, highlighting the consistency and regularity of heavy ion irradiation across varying drain voltages.

Consequently, to mitigate single-event effects on SiC MOSFETs, comprehensive device optimization should focus on structural and packaging enhancements. On the one hand, geometric modifications play a significant role in reducing the susceptibility of radiation damage. For instance, reducing the JFET region width or using split-gate structure as alternative, which aims to minimize the damage to the gate oxide by decreasing the area exposed to ion strikes. Moreover, optimizing the epilayer thickness or concentrations to balance the hotspot at surface and N–N junction, which may reduce the SEB damage risk when irradiated at high bias. On the other hand, in the choice of encapsulation form, the use of plastic-sealed samples instead of metal encapsulation can effectively reduce the penetration depth of the ions, thus mitigating the SEE effects.

**Table 1.** A comparison of SELC I and SELC II degradation modes.

| Degradation modes | Current behaviors during rradiation | Post-irradiation blocking behaviors | Sensitive region |
|---|---|---|---|
| SELC I | $I_D = I_G$ | $I_D = I_G$ | oxide |
| SELC II | $I_D > I_G$ | $I_D = I_G$ at low $V_{DS}$, $I_D > I_G$ when $V_{DS}$ exceeds specific value | oxide and SiC p–n junction |

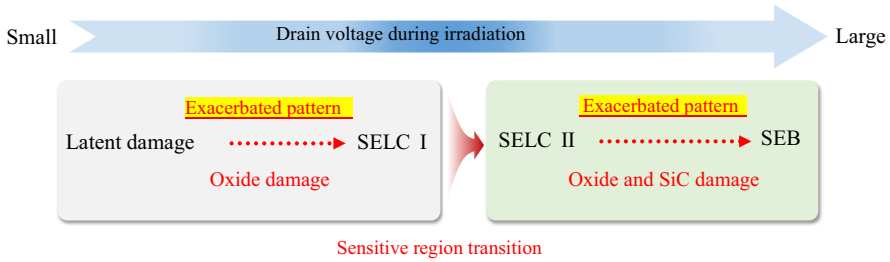


**Fig. 15.** Relationship between latent damage, SELC and SEB degradation modes.

## 5. Conclusion and perspectives

This work presents an exploration of single-event degradation mechanisms and corresponding damage morphology in SiC MOSFETs under complex heavy ion irradiation conditions. The failure mechanisms intricately linked to applied drain voltage. Initially, at minimal voltage levels, damage is predominantly localized within the oxide, with subtle degradation only discernible through PIGS test. As drain voltage incrementally increases, SELC degradation modes emerges, characterized by escalating leakage current and material damage transitioning from oxide to SiC. Despite this evolving damage mechanism, the induced lattice thermal conditions remain insufficient to enable direct visualization of SiC alterations, with only cracks between source metal and ILD interface. When drain voltage surpasses a specific threshold, SEB effect was triggered, which is a more exacerbated pattern of SELC modes. Concurrently, thermal conditions dramatically intensify, approaching the SiC sublimation temperature. This thermal escalation precipitates catastrophic device failure, manifesting as surface cavity formation and structural disintegration.

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