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Chemical Vapor Deposition Growth of Large-Area Monolayer MoS_2 and Fabrication of Relevant Back-Gated Transistor *

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A closed two-temperature-zone chemical vapor deposition (CVD) furnace was used to grow monolayer molybdenum disulfide (MoS_2) by optimizing the temperature and thus the evaporation volume of the Mo precursor. The experimental results show that the Mo precursor temperature has a large effect on the size and shape transformation of the monolayer MoS_2, and at a lower temperature of $<760^{\circ}C$, the size of the triangular MoS_2 increases with the elevating temperature, while at a higher temperature of $>760^{\circ}C$, the shape starts to change from a triangle to a truncated triangle. A large-area triangular monolayer MoS_2 with a side length of 145 μm is achieved at 760°C. Further, the as-grown monolayer MoS_2 is used to fabricate back-gated transistors by means of electron beam lithography to evaluate the electrical properties of MoS_2 thin films. The MoS_2 transistors with monolayer MoS_2 grown at 760°C exhibit a high on/off current ratio of 10^6, a mobility of 1.92 cm^2/Vs and a subthreshold swing of 194.6 mV/dec, demonstrating the feasible approach of CVD deposition of monolayer MoS_2 and the fabrication of transistors on it.

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Two-dimensional materials such as graphene and transition metal dichalcogenides (TMDs)[1,2] have attracted great attention because of their unique features compared with conventional bulk materials. Molybdenum disulfide (MoS_2), as a TMD, has an adjustable band gap and high on/off ratio compared with graphene, which means that photoelectric devices based on a back-gated MoS_2 transistor have broadband spectrum detection, lower dark current and high photoresponsivity.[2] There have been many reports on the fabrication of MoS_2 thin film, with micro-exfoliation being one of the earliest ways to prepare it.[3–5] However, exfoliation is not a reliable fabrication method as the size and thickness of the produced MoS_2 flakes are uncontrollable. As an alternative, the chemical vapor deposition (CVD) method was employed and has been demonstrated to produce large-area and high-quality MoS_2 films.[6–11] The sulfurization of solid molybdenum trioxide (MoO_3) is the most common mechanism of CVD synthesizing MoS_2. Yet, the CVD growth of MoS_2 is influenced by many factors. Yang *et al.* reported a systematical study of low-pressure CVD growth of high-quality crystals of monolayer MoS_2.[12] Cao *et al.* investigated the influence of Ar flow rate on the morphology evolution.[13] Wang *et al.* used the shape transformation model to explain the shape change during the growth of MoS_2 thin films by CVD.[14] Xie *et al.* used MoO_2 as a precursor to grow large-area and high-quality monolayer MoS_2.[15] All of the above works were performed by placing S and Mo sources in a single temperature-zone furnace tube without considering the effects of their respective temperature. In a closed environment, the amount of reactants is mainly determined by the evaporation temperature, and changing the precursor temperature can affect the area of CVD-deposited thin films.[16] By heating S and Mo sources separately in the tube, the reaction between S and Mo sources can be accurately controlled. Usually, the observed edge structures for the MoS_2 flakes are Mo zigzag (Mo-zz) and S zigzag (S-zz) terminations, which are supposed to be the most energetically stable structures. As reported, the shape of the monolayer MoS_2 results from the two types of zigzag edge terminations and can be changed by varying the amount of S and Mo sources.[17] Therefore, in this work, the effects of temperature on the growth of monolayer MoS_2 are investigated using a two-temperature-zone furnace tube and keeping the S source temperature unchanged and changing the Mo source temperature, so as to control the amount of supplied Mo precursor. The shape of the MoS_2 film is changed from a triangle to a truncated triangle when a large quantity of Mo precursor is provided. By optimizing the temperature, a large scale of over 120 μm or even 145 μm MoS_2 triangular islands are formed at a Mo source temperature of 760℃ and an S source temperature of 220℃. Various microanalysis techniques are employed to characterize the structure, thickness and morphologies of the as-grown MoS_2 thin films, including Raman and photoluminescence (PL) spectra, atomic force microscopy (AFM) and scanning electron microscopy (SEM). The shape transformation is explained using the dependence on the atom ratio of Mo to S, which can provide a practical guide for growing large-area MoS_2 thin films. Finally, back-gated transistors based on the as-grown monolayer MoS_2 are fabricated to evaluate the electrical properties of the devices.

Heavily doped p^+ silicon with a resistivity of ∼0.01 Ω·cm was used as the starting substrate. 30 nm SiO_2 was thermally grown on the Si substrate by dry oxidation. Prior to the MoS_2 growth, the SiO_2/Si

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substrate was treated by oxygen plasma with a power of 60 W for 5 min, followed by CVD MoS_2 growth in a two-zone furnace system as shown in Fig. 1(a). An alumina boat with 500 mg S powders (99.99% Aladdin) was placed upstream in the low-temperature zone. Another alumina boat containing 5 mg MoO_3 powders (Ourchem) was placed downstream in the high-temperature zone. The SiO_2/Si target substrate of 12 mm × 12 mm was face down placed on the top of the MoO_3 boat. The distance between the two alumina boats was 20 cm. This long distance was to ensure that the S vapor concentration gradient on the SiO_2/Si substrate could be ignored, as compared with the MoO_3 concentration gradient. The S and MoO_3 sources were heated to 220℃ and 720℃–780℃, respectively, under 100 sccm N_2 carrier gas. Figure 1(b) shows the temperature programming process of the MoO_3 and S precursors. After keeping the temperature for 1 min, the furnace was naturally cooled down to room temperature. Raman and PL spectra were collected by a Horiba LabRAM HR 800 Raman microscopic system, where the power of the solid-state excitation laser was 0.5 mW with a wavelength of 532 nm and a 100× objective was used to focus the laser beam. The SEM images were taken by a Gemini SEM 300-71-12 with an accelerating voltage of 10 kV. The shape and thicknesses of the MoS_2 thin film were characterized by an AFM (Bruker Dimension Edge SPM System). The as-grown MoS_2 triangular islands were used to fabricate the back-gated transistors using electron beam lithography. Poly(methyl methacrylate) and methyl methacrylate were spin-coated on the MoS_2 thin film successively, followed by 150℃ baking. After pattern writing and development, Cr/Au (10/50 nm) were deposited by electron beam evaporation, and then an anneal was performed at 300℃ for 10 min in 95%N_2+5%H_2 atmosphere to reduce the contact resistance between the Cr/Au and MoS_2. The current–voltage (I–V) curve of the devices was measured using a Keithley4200-SCS parameter analyzer at room temperature in a dark ambient circumvent.

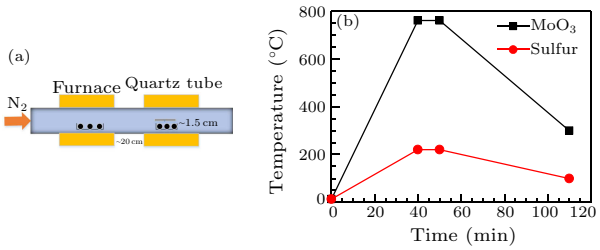

Fig. 1. (a) CVD furnace setup for the MoS_2 growth, and (b) the temperature programming process of MoO_3 and S precursors.

Figures 2(a) and 2(b) show the optical and SEM images of those MoS_2 triangular islands synthesized at a Mo source temperature of 760℃, where the largest side length is 146 μm. Figure 2(c) shows the AFM image of the MoS_2 triangular islands. Its step height is ∼0.65 nm (Fig. 2(d)) along the black line in Fig. 2(c), which is consistent with the thickness of the monolayer MoS_2 grown on a SiO_2/Si substrate.[18] Further, the Raman spectrum is analyzed to confirm the MoS_2 structure. As shown in Fig. 2(e), two characteristic Raman vibration modes can be observed, where the E^1_{2g} mode represents the in-plane vibration molybdenum and the A_{1g} mode is related to the out-of-plane vibration of sulfur atoms.[19] The peak difference between these two modes depends on the layer number of MoS_2. It can be seen that these two modes are located at 384.1 cm^{-1} and 404.9 cm^{-1}, respectively, with a difference of $\Delta k = 20.8\,cm^{-1}$ ($\Delta k = A_{1g} - E^1_{2g}$), which agrees well with that of the CVD-grown monolayer MoS_2.[7–10,18–20] Also, the PL spectrum of the MoS_2 thin film is measured as shown in Fig. 2(f). The sharp peak is located at 1.87 eV, which is consistent with the band gap of the monolayer MoS_2.

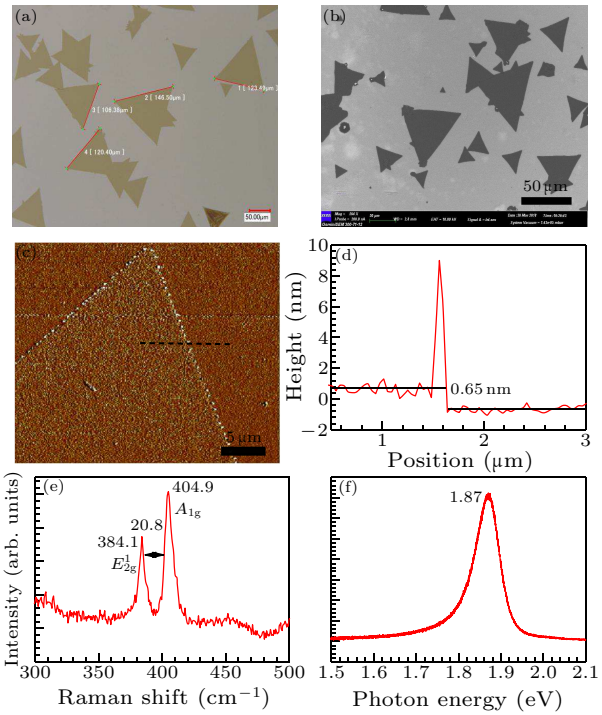

Fig. 2. (a) Optical image of MoS_2 triangular islands, (b) SEM image of MoS_2 triangular islands, (c) AFM image of the MoS_2 triangular islands, (d) its step height along the black line in (c), (e) Raman spectrum and (f) PL spectrum of MoS_2 triangular island.

In fact, the monolayer MoS_2 needs a process from nucleation to growth. Figure 3 shows the SEM images of MoS_2 thin films grown on SiO_2/Si substrates at different Mo precursor temperatures of 720℃, 740℃, 760℃ and 780℃. In all cases, the shape of most MoS_2 thin films is triangular and their sizes become gradually larger as the temperature increases from 720℃ to 760℃. Actually, the growth of the triangular MoS_2 requires sufficient sulfur atmosphere.[8,13,15,20] Cheng *et al.* reported that the MoS_2 thin film with a triangle shape is usually developed when the growth rate of Mo-zz is at least three times faster than that of S-zz in the initial hexagonal nuclei.[21] The relatively low growth temperatures (720℃, 740℃, 760℃) lead to an S-rich atmosphere (Mo:S < 1:2), so that the MoS_2 thin film grows into a triangle shape. As the Mo precursor temperature increases, more unsaturated Mo atoms

can be provided and have higher probability of meeting and bonding with free S atoms in the S-sufficient atmosphere, which is beneficial for the growth of large-size MoS_2 triangular islands. The size of the triangles is $\sim 30\,\mu m$ at 720℃ (Fig. 3(a)) and $\sim 50\,\mu m$ at 740℃ (Fig. 3(b)), while at 760℃ (Fig. 3(c)), the size reaches more than $120\,\mu m$. When the temperature is increased to 780℃ (Fig. 3(d)), the MoS_2 triangles start stacking and their shape is changed from a triangle to a truncated triangle. According to Ref. [20] to grow MoS_2 by the CVD method, MoO_3 should firstly be reduced to volatile MoO_{3-x} by S molecules: $MoO_3+(x/2)S \rightarrow MoO_{3-x}+(x/2)SO_2$. At a relatively high growth temperature, a great amount of MoO_{3-x} (Mo:S > 1:2) is produced according to the above equation, resulting in the reaction in a relatively S-deficient atmosphere. This increase of MoO_{3-x} not only causes the shape evolution but also explains the development of a merged state in the MoS_2 thin film. Figure 4 shows the PL spectrum of the truncated triangular MoS_2 thin film, and an obvious left shift of the peak relative to the monolayer can be seen, which is located at 1.83 eV, implying the increase of MoS_2 thickness. The above results suggest that the Mo source temperature plays a key role in CVD MoS_2 growth, since different temperatures provide different amounts of precursors. At lower temperatures of <760℃, the Mo precursor temperature can be appropriately raised to increase the amount of the Mo source, which is conducive to the formation of large-size MoS_2 triangular islands.

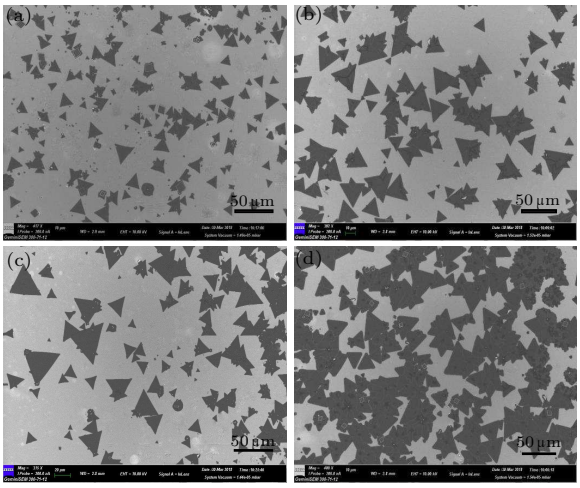

Fig. 3. SEM images of MoS_2 triangles synthesized on SiO_2/Si substrates with Mo precursor temperature at (a) 720℃, (b) 740℃, (c) 760℃, and (d) 780℃.

The above as-grown monolayers of MoS_2 are used to fabricate back-gated transistors to evaluate its electrical properties. Figure 5(a) shows the cross-sectional diagram of the MoS_2 field-effect transistors (FETs) and Fig. 5(b) is an AFM image of the drawn transistor on the MoS_2 triangular islands with a channel width/length of $W/L = 9\,\mu m/5\,\mu m$ (W is an average value). The source/drain (S/D) regions are completely covered by the contacted metals, and the 3-nm-thick thermal SiO_2 acts as the gate dielectric. Gate bias is applied to the p^+-Si substrate to modulate the device, and electrical measurements are conducted under a light-tight and electrically shielded condition at room temperature.

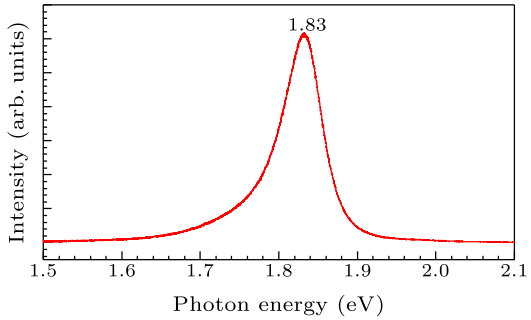

Fig. 4. PL spectrum of the truncated triangular MoS_2 thin film.

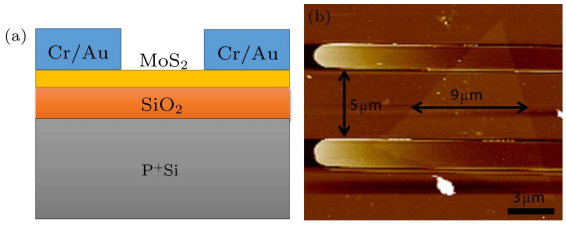

Fig. 5. (a) Structural diagram of the back-gated MoS_2 transistor and (b) AFM image of the transistor fabricated on the triangular MoS_2 island.

Figures 6(a) and 6(b) show the transfer characteristic (drain current (I_{dS}) versus gate voltage (V_G)) at $V_{dS} = 3\,V$ and $5\,V$ in linear and semi-logarithmic scales, respectively, for the transistor with monolayer MoS_2 as the channel grown at 760℃. The device exhibits a low-off current ($10^{-12}\,A$) with an on/off current ratio up to 10^6. Figures 6(c) and 6(d) exhibit the output characteristic curves of the MoS_2 transistor under small V_{dS} from -0.1 to $+0.1\,V$ and large V_{dS} up to $3\,V$ to demonstrate its linearity and driving capability, respectively. It can be seen that an approximate linear relationship between I_{dS} and V_{dS} is observed when V_{dS} changes from $-0.1\,V$ to $0.1\,V$ for V_G from $18\,V$ to $30\,V$, indicating a non-ideal ohmic contact between the metal and MoS_2. An unavoidable problem in the CVD MoS_2 is that the incomplete reacted MoO_3 may remain on the MoS_2 thin films when the CVD stops, which increases contact resistance and leads to a non-ideal ohmic contact. In addition, some deep traps between the as-grown MoS_2 and SiO_2 could be introduced, which could capture some electrons in the channel as V_{dS} increases and induces current collapse phenomena,[22] e.g. negative differential resistance effect, as shown in Fig. 6(d). The carrier mobility of the back-gated MoS_2 FETs was extracted using the formula $\mu = (\Delta I_{dS}/\Delta V_G) \times (L/WC_{ox}V_{dS})$, where C_{ox} is the gate capacitance per unit area, and $\Delta I_{dS}/\Delta V_G$ is the slope of the transfer curve in the linear region. The field-effect mobility of the as-grown MoS_2 transistor is calculated to be $1.92\,cm^2/Vs$, which is a low value due to the large S/D contact resistances, as mentioned above. In addition, the extracted subthreshold swing (SS) has a relatively small value of 194.6 mV/dec. The electrical properties of other transistors with mono-

layer MoS_2 grown at 720℃ or 740℃ are summarized in Table 1. Obviously, the transistor with monolayer MoS_2 grown at 760℃ has the best electrical performance. It is worth noting that the electrical properties of the fabricated MoS_2 transistors, e.g. saturation current and carrier mobility, are not better than those reported in previous reports.[23–26] Except for the large S/D contact resistances, other causes probably include poorer interface quality between the MoS_2 and gate dielectric, and increased gate leakage due to the deterioration of the SiO_2 gate dielectric during the MoS_2 growth. Therefore, the S/D contact and interfacial optimizations are important in the future, and a transfer of the as-grown MoS_2 is also needed to obtain better device performances.

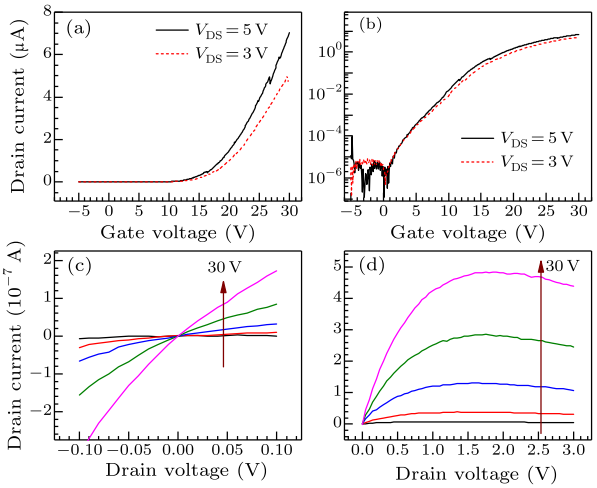

Fig. 6. Transfer characteristics of the as-grown MoS_2 transistor: (a) in linear scale and (b) in logarithmic scales (V_{dS} = 3 V and 5 V respectively). Output characteristics of the as-grown MoS_2 transistor: (c) small range of V_{dS} from −0.1 V to 0.1 V and (d) large range of V_{dS} from 0 V to 3 V (V_G from 18 V to 30 V with a step of 3 V).

Table 1. Performance of devices with different size monolayer MoS_2 as channel grown at different temperatures.

Temperature	Mobility (cm^2/Vs)	SS (mV/dec)	On/off ratio
720℃ (10 μm)	0.24	464.2	10^6
740℃ (15 μm)	0.57	272.5	10^6
760℃ (20 μm)	1.92	194.6	10^6

In summary, the effects of the Mo precursor temperature on the size and shape of MoS_2 thin film have been investigated for CVD MoS_2. It is found that as the Mo precursor temperature rises from 720℃ to 760℃, the size of the MoS_2 triangular islands gradually increases up to over 120 μm, to a maximum of 146 μm. When the temperature reaches 780℃, the shape and thickness of the MoS_2 thin film are changed. The involved mechanisms lie in the change of the atomic ratio of S atoms to Mo atoms with the Mo precursor temperature: Mo:S < 1:2 for the temperature range of 720℃–760℃ due to the S-rich atmosphere, resulting in the growth of triangular MoS_2 thin film whose size increases as the temperature increases owing to the increased Mo atoms and bonding probability with S atoms, and Mo:S > 1:2 for high temperatures of > 760℃, e.g. 780℃, due to the S-deficient atmosphere, leading to the stacking of the triangular MoS_2 islands into truncated triangles. AFM, SEM, Raman and PL spectra are used to characterize the MoS_2 thin film, and confirm its structure and monolayer thickness. Moreover, the as-grown MoS_2 triangular islands are used to fabricate back-gated transistors to evaluate their electrical properties. The transistors are n-channel enhancement-mode FETs, where the device with the monolayer MoS_2 grown at 760℃ exhibits the best electrical properties: a mobility of 1.92 cm^2/Vs and a subthreshold swing of 194.6 mV/dec, indicating the feasible approach of fabricating transistors on monolayer MoS_2 grown by the CVD method. Further optimization of growth processing and improvements of the S/D contact and MoS_2/dielectric interface are needed to obtain excellent electrical performances of the CVD-grown MoS_2 transistors.

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