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Physics-based analysis and simulation model of electromagnetic interference induced soft logic upset in CMOS inverter*

Yu-Qian Liu(刘彧千)[1,†], Chang-Chun Chai(柴常春)[1], Yu-Hang Zhang(张宇航)[2], Chun-Lei Shi(史春蕾)[1], Yang Liu(刘阳)[1], Qing-Yang Fan(樊庆扬)[1], and Yin-Tang Yang(杨银堂)[1]

[1] *Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*

[2] *Department of Micro-Nano Electronics, Shanghai Jiao Tong University, Shanghai* 200240, *China*

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The instantaneous reversible soft logic upset induced by the electromagnetic interference (EMI) severely affects the performances and reliabilities of complementary metal–oxide–semiconductor (CMOS) inverters. This kind of soft logic upset is investigated in theory and simulation. Physics-based analysis is performed, and the result shows that the upset is caused by the non-equilibrium carrier accumulation in channels, which can ultimately lead to an abnormal turn-on of specific metal–oxide–semiconductor field-effect transistor (MOSFET) in CMOS inverter. Then a soft logic upset simulation model is introduced. Using this model, analysis of upset characteristic reveals an increasing susceptibility under higher injection powers, which accords well with experimental results, and the influences of EMI frequency and device size are studied respectively using the same model. The research indicates that in a range from L waveband to C waveband, lower interference frequency and smaller device size are more likely to be affected by the soft logic upset.

Keywords: electromagnetic interference, soft logic upset, non-equilibrium carrier, upset model

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1. Introduction

The complexity of the electromagnetic environment today puts the performance and reliability of CMOS integrated circuits to the test. A typical instance is the electromagnetic interference (EMI) generated by high-power microwave (HPM) sources, which can couple into electronic systems easily through the front-door (such as antennas of receiver) and back-door (such as apertures on shell, interconnected wires and power cables) paths.[1–7] Different kinds of EMIs have dissimilar influences on the CMOS integrated circuits, from bit error (commonly seen in digital transmission) to catastrophic overheat structural damage.[8–11] The bit error is more noticeable for its higher unpredictability and lower triggering threshold than the permanent damage. Hence, the study on EMI induced bit error in CMOS integrated circuits is of great importance.

For CMOS inverters, device logic upset is a main reason to cause the circuit bit error. Considerable research efforts have been devoted to the parasitic latch-up effect evoked logic upset under EMI, we call it hard logic upset here.[12–17] By triggering a positive feedback in the parasitic PNPN structure, the latch-up effect can cause a non-reversible upset in CMOS inverter until a power-down. Nevertheless, investigations on soft logic upset — an instantaneous reversible upset with no apparent latch-up effect happening — focused only on experimental phenomena. Kim *et al.* revealed experimental results of 0.5 μm and 1.5 μm technology CMOS inverters injected by EMIs in a range from 0 dBm to 24 dBm, and using a proposed experimental parameter extraction method, critical soft logic upset was observed through the degeneration of static and dynamic characteristics.[18,19] Wang *et al.* also reported the experimental results inadvertently in investigating the latch-up threshold of commercial CMOS inverters, more specifically, the soft logic upset can exactly be found in the results under the latch-up threshold.[20] As for the explanation of physical mechanism, Iliadis *et al.* proposed a modified output current expression to illustrate the EMI induced soft and hard logic upsets in individual MOSFETs and cascaded inverters.[21,22] In simulation studies, Wang *et al.* established a simulation program with the integrated circuit emphasis (SPICE) model to predict two kinds of logic upsets (hard and soft) in CMOS inverters, which matched well with experimental results.[23] From the above, it can be noted that little attention has been paid to the specialized mechanism explanation for soft logic upset in CMOS inverters. Moreover, a physics-based simulation model is also crucial in understanding the soft logic upset.

In this work, physical mechanism analysis of EMI induced soft logic upset in CMOS inverters is presented specifically, and the upset is attributed to an incomplete recombination caused non-equilibrium accumulation. Moreover, a soft logic upset simulation model that consists of a device numer-

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†Corresponding author. E-mail: yuqianliuxd@163.com

ical simulation part, an output digital filter part and a simulation static parameter extraction part, is proposed. Using this model, investigations on the soft logic upset influenced by the EMI injection power, the interference frequency and the device size are conducted, and the results are well supported by the reported experiments.

2. Theoretical foundation and analysis

2.1. Device structure and setup

A typical three-dimensional n-well CMOS inverter structure studied in this work is shown in Fig. 1. The device is established based on 0.35-μm CMOS technology and the distance between two gates is 5 μm. The device has 10.5 μm of total lateral size and 4 μm of depth, 2 μm of the vertical length of n-well. Arsenic and Boron are chosen to create n-type and p-type doped regions. Two parasitic transistors Q_1 and Q_2 are exhibited in the schematic diagram, the impedances of substrates are represented by r_{well} and r_{sub} respectively. Under normal operation conditions, the supply voltage V_{dd} is 3.3 V with mid-point voltage V_{m} located at about 1.65 V. The initial temperature of the device is 300 K to meet the ambient temperature, and the top surface is set to be adiabatic. The logic flip function of CMOS inverter is realized through V_{in} and V_{out}. An EMI is injected into V_{in} directly to simulate the unprotected inputs in CMOS circuits. The injected plane wave is in sinusoidal form which is proved to be convictive in experiment.[24] The power of the EMI ranges from 3 dBm to 32 dBm, and the interference frequency is focused on 1 GHz to 5 GHz (L to C waveband). These conditions are appropriate to the inducing of the soft logic upset in CMOS inverters after adequate attempts.

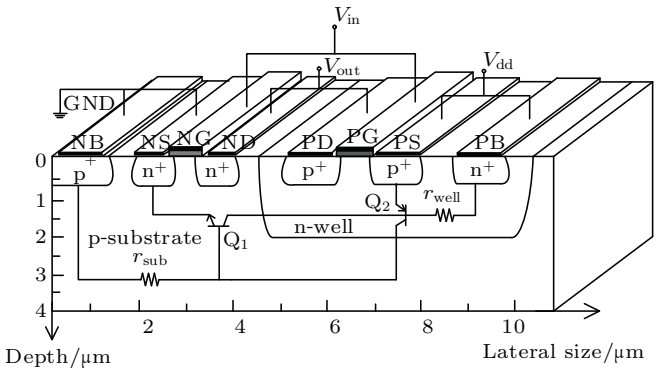

Fig. 1. Schematic diagram of n-well CMOS inverter structure.

2.2. Soft logic upset mechanism

The latch-up effect is considered to be one of the upset mechanisms in CMOS inverters.[12–17] However, when the EMI is not severe enough to trigger the latch-up, the interference on CMOS inverters will induce a real-time soft logic upset. To thoroughly understand the physical mechanism of this upset, we begin with the semiconductor continuity equation in CMOS inverter under the thermal equilibrium state

$$\frac{\partial n_0}{\partial t} = \frac{\partial p_0}{\partial t} = G_0 - R_0 = 0, \tag{1}$$

where n_0 and p_0 refer to the initial electron concentration and the initial hole concentration, G_0 is the generation rate, $R_0 = n_0 p_0 r$ is the recombination rate, and r is the probability of electron hole recombination. When the sinusoidal EMI signal V_{in} is injected, the external EMI produces an interference electric field immediately in both gates of the inverter. Since the field strength is not strong enough to cause an oxide breakdown, the generation rate under EMI remains invariable. So the continuity equation under EMI is given as

$$\frac{\partial n_{\text{EMI}}}{\partial t} = \frac{\partial p_{\text{EMI}}}{\partial t} = G' - R' = n_0 p_0 r - n_{\text{EMI}} p_{\text{EMI}} r', \tag{2}$$

in which n_{EMI} and p_{EMI} are the interfered electron concentration and the interfered hole concentration, respectively; r' is the influenced probability of recombination.

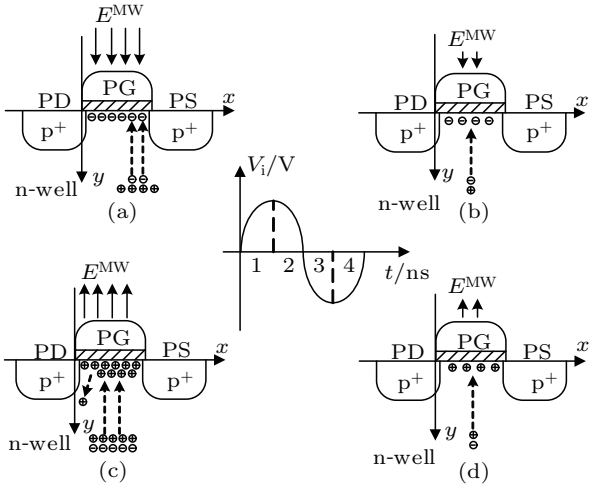

Fig. 2. Schematic diagram of the generation and transportation of non-equilibrium carriers in inverter's PMOS during a whole interference period.

In practical applications, CMOS inverter often works in the state that one of the MOSFETs is on and the other is off. So here we illustrate a condition that $V_{\text{in}} = 3.3$ V (input logic high) to help analyze the EMI process. In this circumstance, non-equilibrium carriers are evoked in both positive channel metal–oxide–semiconductor (PMOS) and negative channel metal–oxide–semiconductor (NMOS) substrates and then swept into the channels to influence the conductive character of the device. In the NMOS part of the inverter, the existence of the inherent inversion channel current cannot obviously change its conductivity when the non-equilibrium electrons arrive at the channel. In the PMOS part, an extra channel current is generated by the non-equilibrium holes and becomes the main reason to induce the soft logic upset. A schematic diagram of a whole interfering period at PMOS

when $V_{in} = 3.3$ V can be seen in Fig. 2. The injection sinusoidal EMI signal V_i is spilt into four parts according to its variation tendency. In the first part, shown in Fig. 2(a), $V_i > 0$ and $\partial V_i/\partial t > 0$, which means the growing interference field is along the y axis, pushing the non-equilibrium electrons to the channel. However, no lateral channel current arises since the source and drain of the PMOS are in p-type doping. During the second part in Fig. 2(b), $V_i > 0$ and $\partial V_i/\partial t < 0$, so the channel current remains negligible and the accumulation of non-equilibrium electrons decreases. The third part is illustrated in Fig. 2(c), the interference field changes its orientation and moves the non-equilibrium holes to the channel. During this part, the extra channel inversion layer current appears and increases with the strength of the interference field increasing, leading to a soft upset in the inverter. In the fourth part as seen in Fig. 2(d), the extra channel current falls down with the decrease of interference field, meanwhile the upset to the logic features mitigates.

Considering no direct injection of non-equilibrium carriers occurring during the soft logic upset (because no oxide breakdown happens), the generation of non-equilibrium carriers is attributed to the change of the electron–hole recombination probability r. As is well known, the generation and recombination happen constantly in a doped semiconductor. When the EMI appears, part of generated carriers are swept away (along or against the field direction) before their recombination, leading the electron hole recombination probability r to decrease. The recombination probability change in PMOS can be expressed as follows:

$$\frac{r}{r'_p} = \begin{cases} 1, & t \in \left[\dfrac{a}{2f}, \dfrac{a+1}{2f}\right), \\ 1+\sin(2\pi f t+\varphi), & t \in \left[\dfrac{a+1}{2f}, \dfrac{a+2}{2f}\right), \end{cases} \quad a = 0,2,4,6,\ldots, \tag{3}$$

where r'_p is the EMI affected recombination probability in PMOS substrate, f is the frequency of EMI signal, and φ is its initial phase, and t is the interference time. The EMI induced extra non-equilibrium holes $\Delta p = p_{EMI} - p_0$. Since the inverter is in thermal equilibrium, $\partial p_0/\partial t = 0$, we have $\partial \Delta p/\partial t = \partial p_{EMI}/\partial t$. Meanwhile, under the slowly and continuously varying EMI signal, $\partial p_{EMI}/\partial t = 0$. Additionally, the non-equilibrium carriers are formed in pairs, so $\partial \Delta p = \partial \Delta n$. Substituting these conditions into Eq. (2), the extra non-equilibrium holes Δp can be calculated from

$$\Delta p = \frac{1}{2}\left[\left(n_0^2 + p_0^2 + \frac{4n_0 p_0 r}{r'_p} - 2n_0 p_0\right)^{1/2} - (n_0 + p_0)\right], \tag{4}$$

and the accumulation of the non-equilibrium holes in PMOS channel will inevitably form an extra channel current. Based on the semiconductor current density equation, the PMOS extra channel current density can be shown as follows:

$$J_{extra-p}(x) = q\mu_p(\Delta p + p_0)\left(\frac{(V_{EMI} - V_{dd})}{d_{ox}} \cdot \frac{x}{T}\right) - qD_p \frac{\partial(\Delta p + p_0)}{\partial y}, \tag{5}$$

where q is the charge energy, μ_p is the hole mobility, d_{ox} and T respectively are the thickness of gate oxide layer and the channel depth, V_{EMI} is the virtual value of external interference voltage, and D_p is the hole diffusion coefficient. The diffusion current under EMI is along the y axis, which barely contributes to the extra channel current, so we have $qD_p(\partial p_{EMI}/\partial y) \approx 0$. Then the PMOS extra channel current can be expressed as

$$I_{extra-p} = \int_0^L H\left(P^{EMI}\right) d_{ch} q\mu_p(\Delta p + p_0) \times \left(\frac{(V_{EMI} - V_{dd})}{d_{ox}} \cdot \frac{x}{d_{ch}}\right) dx, \tag{6}$$

where L is the channel length. As the interference field increases, a peculiar situation occurs that the drift speed along the negative y axis is much higher than along the x axis, leading some non-equilibrium carriers to collide with each other in the surface of gate oxide and substrate. The $H(P^{EMI})$ is used here to explain this kind of extra current loss, where P^{EMI} is the power of the injection EMI signal.

Similarly, when $V_{dd} = 0$ V, the soft logic upset is mainly determined by the interference in the NMOS channel, the extra channel current $I_{extra-n}$ can be calculated from

$$I_{extra-n} = \int_0^L H\left(P^{EMI}\right) d_{ch} q\mu_n(\Delta n + n_0) \times \left(\frac{(V_{EMI})}{d_{ox}} \cdot \frac{x}{d_{ch}}\right) dx. \tag{7}$$

The minority carriers in the substrate of NMOS are electrons, so the $I_{extra-n}$ occurs in the first half of each disturbance cycle as exhibited in Fig. 2. Furthermore, the EMI induced output logic deviations can be calculated respectively based on the $I_{extra-p}$ and $I_{extra-n}$, and are expressed as

$$\Delta V_{high} = \frac{L}{W\mu_n C_{ox}(V_G - V_T)} \cdot I_{extra-p}, \tag{8}$$

$$\Delta V_{low} = 3.3 - \frac{L}{W\mu_n C_{ox}(V_G - V_T)} \cdot I_{extra-n}, \tag{9}$$

where ΔV_{high} and ΔV_{low} are the deviation of output high level and output low level, W is the channel width, V_G and V_T are the gate voltage and threshold voltage in normal operation condition, and C_{ox} is the inherent capacitance of the gate oxide layer.

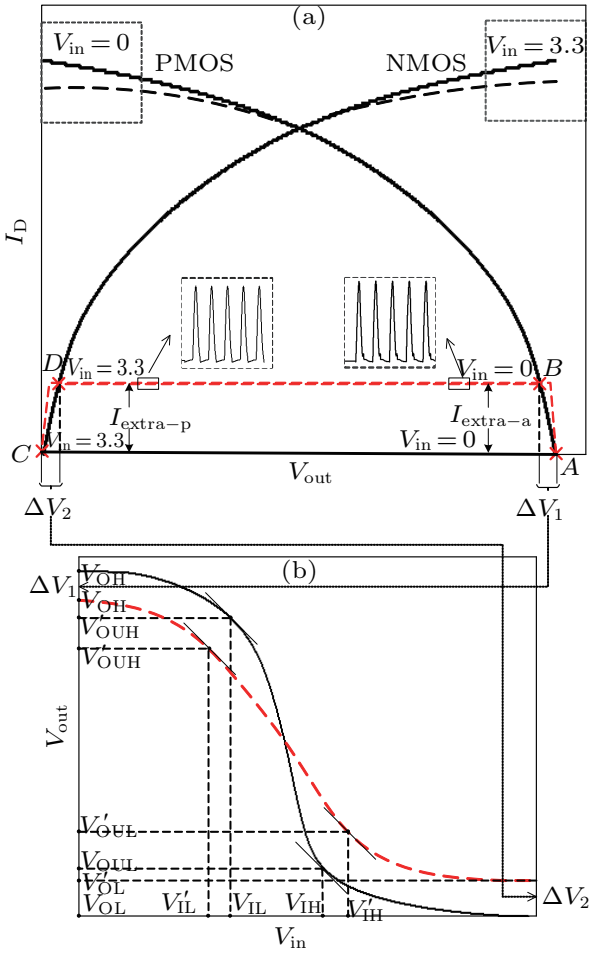

Fig. 3. (color online) Schematic diagram of soft logic upset principle through a deviation of the voltage transfer characteristic (VTC) curve.

The voltage transfer characteristic (VTC) curve under EMI induced soft logic upset is revealed in principle in Fig. 3. Figure 3(a) shows the I_D–V_{out} curves of NMOS and PMOS in the inverter. It is easy to notice that when $V_{in} = 0$ V, the EMI induced $I_{extra-n}$ changes the intersection point between the NMOS and PMOS load lines from A to B, and causes a V_{out} to shift by ΔV_1, which eventually leads to the decrease from V_{OH} to V'_{OH} in the VTC curve as seen in Fig. 3(b). Identically, the $I_{extra-p}$ induces a change from C to D, which evokes the ΔV_2 and the VTC curve deviating from V_{OL} to V'_{OL}. For the same reason, the $I_{extra-p}$ and $I_{extra-n}$ can influence the whole VTC curve of the CMOS inverter. One thing should be noticed is that the turned-on MOSFST shows some current loss in its saturation region (seen in two dotted regions in Fig. 3(a)). The reason of this phenomenon is that the strong interference field on the gate of the non-sensitive MOSFET (for example, the NMOS when $V_{in} = 3.3$ V) pushes some inverse carriers to the substrate, which is not the dominant cause of the soft logic upset. According to the deduction above, the soft logic upset can be more intuitively demonstrated by the decay of static characteristics. Moreover, the recession of the output range, gain and a noise margin can be noticed easily in the curve as well.

3. Simulation results and discussion

3.1. Soft logic upset dependence on injection power

Figure 4 indicates the numerical simulation output voltages of the CMOS inverter. The EMI signal V_{in}'s ranging from 3 dBm to 32 dBm in value are applied in the time range from 5 ns to 10 ns (to save simulation time, no cumulative effect is found in longer term simulation attempt). The EMI is superposed with the original input logic level which is low in Fig. 4(a) and high in Fig. 4(b). A time-dependent output deviation is observed which fits the soft logic upset features well. Moreover, when $V_{in} = 3.3$ V, the upset occurs in second half of each EMI cycle, which is in line with the analyzed results mentioned in Subsection 2.2, and the disturbed output voltages are also in sinusoid-like form and increase with the augment of the injection power. The same consequence is also shown in Fig. 4(a).

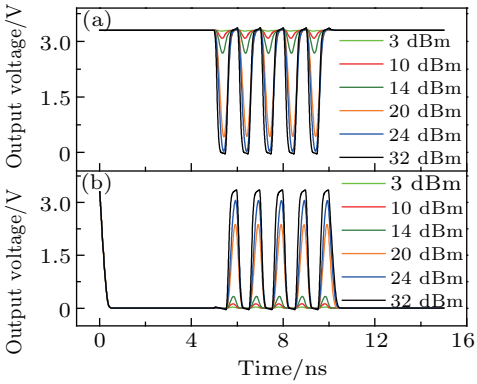

Fig. 4. (color online) Numerical simulation output voltages varying with time under 3 dBm to 32 dBm EMI $V_{in} = 3.3$ V (a) and 0.0 V (b).

The jumping interference output voltages in Fig. 4 are intuitional but hard to measure accurately. Wang *et al.* reported that a duplexer was used in EMI injection experiments.[20] The interference output voltages can be separated into upset output logic voltages and high frequency clutters. Referencing this idea, a digital filter module is introduced in simulation as shown in Fig. 5. The numerical simulation output voltage data (for example, one of the curves in Fig. 4) is imported in the input voltage A, which can be observed directly in oscilloscope 1. Oscilloscopes 2 and 3 show the high frequency clutter and the upset output logic voltage respectively by sending the input voltage A into the high-pass and low-pass filters. The data output retains the useful upset output logic voltage data in an array named Simout. Using this method, it is easy to visualize the EMI induced soft logic upset through an output logic deviation. Figure 6 shows the comparison between the processed simulation output logic voltages (seen in Fig. 6(b)) and experimental results (seen in Fig. 6(a)) reported in Ref. [20]. The input levels are both low, and the frequencies of EMI are 1 GHz identically. Fine conformity of their trends can be noticed between experiments and simulations, the difference in

specific value is caused by the actual experimental equipment loss and the difference between simulated and real manufactured inverters. Considering the original features of the digital filter, there is a filter delay of about 3 ns as shown in Fig. 6(b), which barely affects the tendency of the curves. Based on the simulation results, an experiment measurable parameter ΔV marked in Fig. 6(b) is used to estimate degree of soft logic upset in this work, which is expressed as

$$\Delta V = \left| V_{\text{out}}^{\text{EMI}} - V_{\text{out}} \right|, \tag{10}$$

where $V_{\text{out}}^{\text{EMI}}$ is the filtered output logic voltage under EMI and V_{out} is the normal output level.

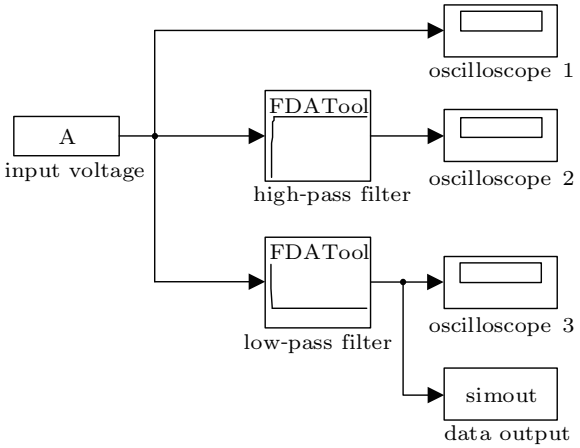

Fig. 5. Schematic diagram of digital filter module.

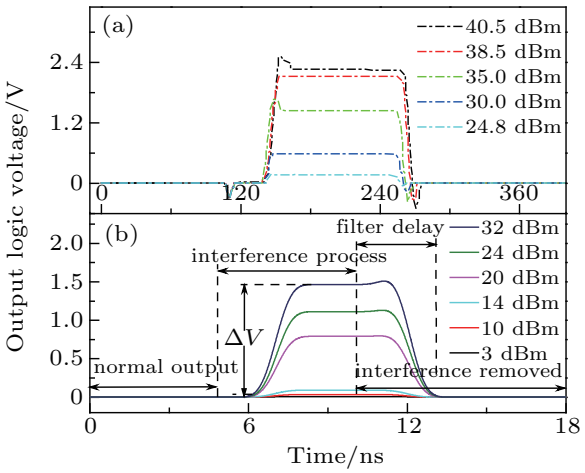

Fig. 6. (color online) Upset logic output voltages in (a) experiments reported in Ref. [20], (b) simulations after using the digital filter module.

Mechanism explanation in Subsection 2.2 reveals that the extra channel current induces the soft logic upset in CMOS inverter. To justify the proposed parameter ΔV, in Fig. 7 we plot the curves of ΔV and the interfered extra channel current density J_{extra} (including $J_{\text{extra-n}}$ and $J_{\text{extra-p}}$) versus injected interference power. A parallel rising tendency between ΔV and J_{extra} emerges with the increase of the EMI injection power, indicating that the parameter ΔV can reflect the channel carrier distribution changes in CMOS inverters reasonably.

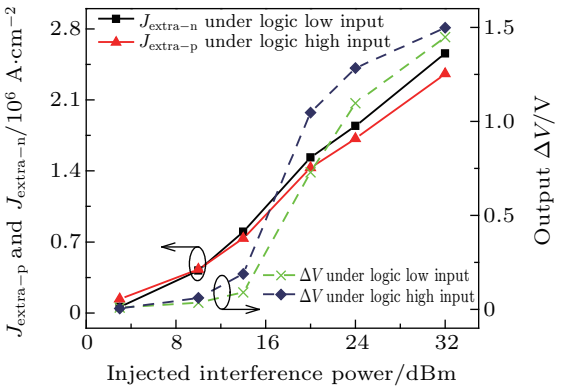

Fig. 7. (color online) Curves of ΔV and interference extra channel current density $J_{\text{extra-n}}$ and $J_{\text{extra-p}}$ versus injected interference power.

The experimentally measurable parameter ΔV describes the soft logic upset conveniently. However, to comprehensively measure the device situation under soft logic upset, an extraction of the voltage transfer characteristic is helpful. To achieve this, a carrier equivalent simulation method is used in this work. Based on above-mentioned study, 5 groups of data (N_{pn}, T) (Here, N_{pn} ($n = 1, 2, 3, 4, 5$) is the peak doping concentration and T is the thickness of the interference extra carrier layer.) are collected in numerical simulation results at the positions that make the channel 5 equal parts, the collecting time points are the ends of the first and third parts of one interference cycle. Then the equivalent interference carrier doping concentration C_{s} is given as

$$C_{\text{s}} = \frac{1}{10} \sum_{\text{n}=1}^{5} C_{\text{pn}} \cdot H(P^{\text{EMI}}), \tag{11}$$

where $H(P^{\text{EMI}}) \approx 1/2$ when injection power is lower than 30 dBm and $H(P^{\text{EMI}}) \approx 1/4$ when higher than 30 dBm according to previous simulations. Figure 8 reveals the variations of C_{s} and T with the increase of injected voltage. An approximately proportional relationship between C_{s} and interference voltage can be found, meanwhile the interference extra carrier layer thickness T is found to be almost stable at 10 nm in both MOSFETs. Then we remodel the device by using the data in Fig. 8, two man-made inversion channels are placed into the simulation structure. Using this carrier equivalent simulation method, complete VTC curves under augmented EMI can be obtained. The contrast between the EMI induced inverter VTC degradation in simulation and that in reported experimental results[19] can be seen in Fig. 9. Besides good consistency between simulations (seen in Fig. 9(a)) and experiments (seen in Fig. 9(b)), several signs of degradation in static performance of the inverter can be observed likewise. Besides the decrease of output logic voltage range $V_{\text{OH}} - V_{\text{OL}}$, the attenuation of gain ($g_{\text{m}} = \partial I_{\text{ds}}/\partial g_{\text{s}}$) and the degeneration of noise margin SNM_{H} and SNM_{L} ($SNM_{\text{H}} = V_{\text{OH}} - V_{\text{IH}}$ and $SNM_{\text{L}} = V_{\text{IL}} - V_{\text{OL}}$) are also observed. All these phenomena are supported by the

mechanism in Subsection 2.2. Furthermore, with the increase of the EMI power, the degradation of VTC curves becomes more severe. When the injection power reaches 20 dBm, the VTC curve comes to a complete recession, which means the disappearing of the flip feature in CMOS inverter. In addition, since the simulations are under ideal conditions and the device size and supply voltage in simulation are different from in experiment, the interference VTC curves cannot be exactly the same.

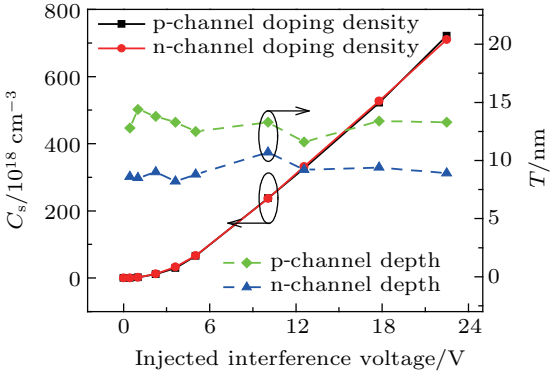

Fig. 8. (color online) Variations of equivalent interference carrier doping concentration C_s and average channel depth T with injection voltage increasing.

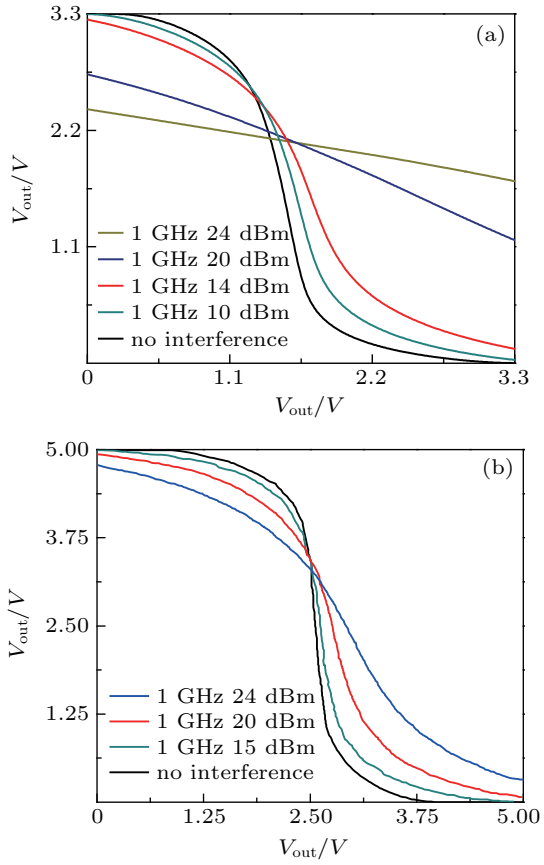

Fig. 9. (color online) Comparisons of EMI-induced inverter's VTC degradation between (a) simulation results and (b) experimental results reported in Ref. [19].

To verify the simulation model more comprehensively, experiments can be setup as shown in Fig. 10. The interference signal V_{EMI} is generated by a network analyzer (e.g., HP8753C), and then coupled with V_{in} through a bias-T. The normal input level V_{in}, along with the V_{dd} is produced by a semiconductor parameter analyzer (e.g., HP4145B). Then the coupled signal is directly injected to the test chip. The test chip should be designed and fabricated specially: the input and output of the inverter should have coplanar waveguides in ground-signal-ground (GSG) configuration. The VTC curve of the inverter is measured by the voltage monitor unit V_{m1} in the semiconductor parameter analyzer. Through two filters (as shown in Fig. 5), the disturbed output logic voltage V_L and the high-frequency interference voltage V_H can be monitored respectively in V_{m3} and V_{m2}.

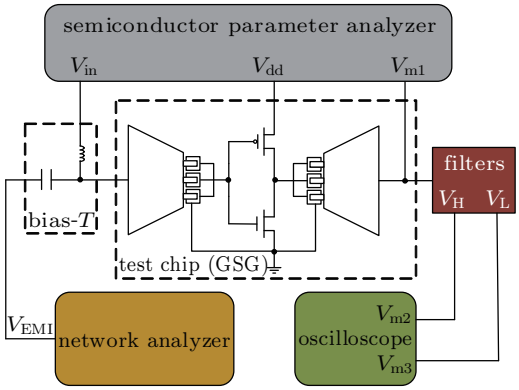

Fig. 10. (color online) General experiment setup on effect of EMI on single CMOS inverter.

3.2. Dependence on interference frequency

Considering the high complexity of the intentional electromagnetic environments, investigation on the influence of EMI frequency on the soft logic upset is valuable. Using the proposed parameter ΔV, we simulate L-to-C waveband EMI induced soft logic upset in CMOS inverter. Figure 11 illustrates the output ΔV varying with the injection power under different EMI frequencies, and the reported output logic voltages in experiment[20] is also given for comparison. An apparent trend can be found that under 1-GHz-to-5-GHz EMI, lower interference frequencies tend to induce severer degeneration as shown by larger output ΔV, which is supported by the reported experimental results in Ref. [20]. In addition, Kim *et al.* conducted EMI experiments[22] on single enhanced n-channel MOSFET, which can be considered as a part of the CMOS inverter, and the results revealed the same tendency as our simulations'. Moreover, in order to trace the physical understanding of the EMI frequency influence, device numerical simulation results of electron concentrations when $V_{in} = 0.0$ V are illustrated in Fig. 12. The condition of no EMI is plotted in Fig. 12(a) for comparison, figures 12(b) and 12(c) respectively illustrate the device internal electron concentrations under 1-GHz and 5-GHz EMI. The injection powers are both 24 dBm. Obvious electron inversion layers can be seen in these two

figures, which confirms the existence of the soft logic upset. Furthermore, more substrate non-equilibrium electrons are found in Fig. 12(b), which is consistent with the conclusion in Fig. 11.

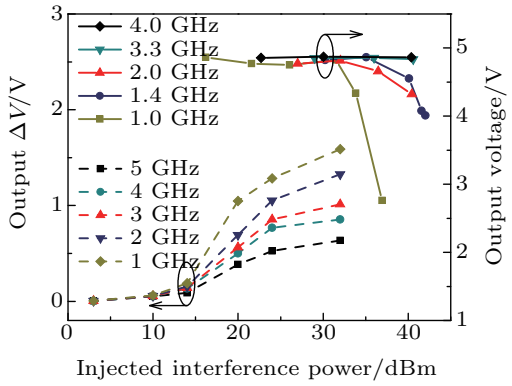

Fig. 11. (color online) Simulation results of (left) output ΔV and (right) experimental results of output voltage reported in Ref. [20] under EMI at frequencies ranging from 1 GHz to 5 GHz.

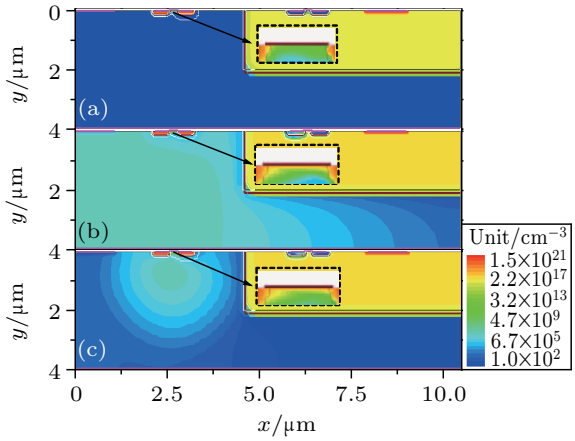

Fig. 12. (color online) Device simulation results of low level input electron concentrations under (a) no EMI, (b) 1-GHz and 24-dBm EMI, (c) 5-GHz and 24-dBm EMI. The inset shows the electron concentrations in NMOS channels.

Based on the mechanism explanation in Subsection 2.2, this frequency upset characteristic is attributed to the decrease of non-equilibrium carriers at higher frequencies. With the increase of the EMI frequency, the interference signal is no longer the slowing varying situation and the carriers change their directions too fast, thereby increasing the recombination possibility instead.

3.3. Dependence on device size

Investigation on the dependence between the device size and soft logic upset is conducted here. Half of size simulation device is established, compared with the primary CMOS inverter structure mentioned in Subsection 2.1. The shrinkage is based on the quasi-constant voltage reduction rule, which means that to maintain the normal operational function of the CMOS inverter, doping concentration in the device substrates should increase to 1.8×10^{17} cm^3 (6×10^{16} cm^3 in original size device) and the supply voltage should be adjusted to 2.5 V.

Figure 13 shows the comparison between the interference degrees in original inverter and half the size of inverter under 3-dBm-to-32-dBm EMI when $V_{in} = 0.0$ V. Owing to having different V_{dd} values, the interference degree is represented by $\Delta V/V_{dd}$. Obviously, half the size of CMOS inverter shows a more serious soft logic upset, whether the input is at a logic high level (see Fig. 13(a)) or at a low level (see Fig. 13(b)). To further confirm this conclusion, the electron concentration distributions of different device sizes are shown in Fig. 14. Figure 14(a) shows no EMI control group either, and figure 14(b) displays the original size simulation results under 24-dBm and 1-GHz EMI while figure 14(c) shows half the size of situation under the same interference. It can be indicated that the distribution trends of non-equilibrium electrons in inverters of different sizes are identical, which means that the mechanism of soft logic upset is not affected by device size. However, the value of non-equilibrium electron concentration is higher in half the size of device. This phenomenon is trigged by the fact that the inverters with smaller size are more inclined to accumulate the non-equilibrium carriers, which means that they are more likely to have soft logic upsets under EMI.

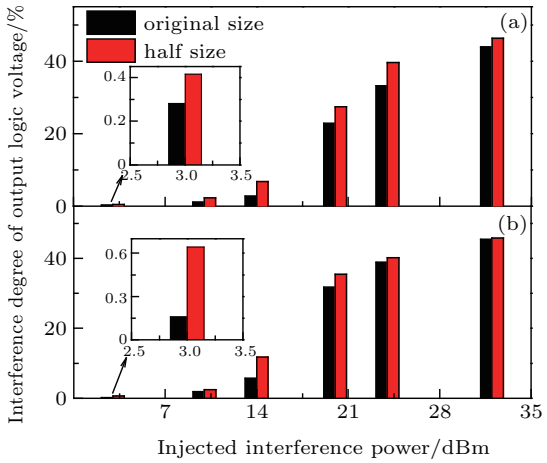

Fig. 13. (color online) 3-dBm-to-32-dBm EMI induced soft logic upsets in original and half the size of inverter at $V_{in} = 3.3$ V (a) and 0.0 V (b). The inset shows the results at an injection power of 3 dBm.

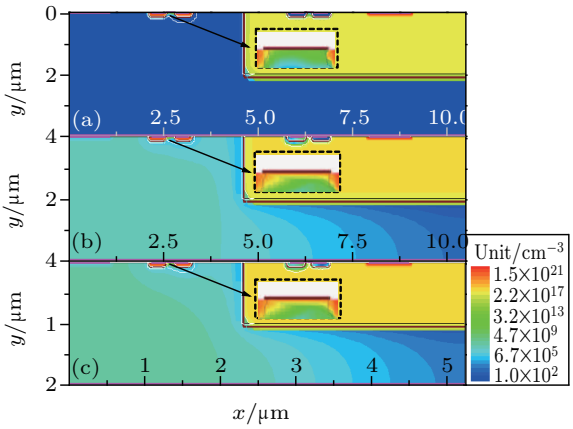

Fig. 14. (color online) Device simulation results of low level input electron concentrations at (a) original size and no EMI, (b) original size and 24-dBm EMI, (c) half size and 24-dBm EMI. The inset shows the electron concentrations in NMOS channels.

4. Conclusions

Theoretical analysis concentrating on the EMI induced soft logic upset in CMOS inverters is presented. The upset is directly caused by an abnormal turn on of the specific MOSFET in single inverter, and furthermore, the unusual inverse channel is formed by an incomplete recombination caused non-equilibrium accumulation under the effect of the interference field. Based on the semiconductor basic equations, the upset extra channel current I_{extra} is obtained, and then the logic output deviation and the static characteristics degradation are calculated using I_{extra}. These mechanism explanations provide an in-depth understanding of soft logic upset caused CMOS bit error.

In simulation, a soft logic upset simulation model is established and used in the study of EMI power characteristic. First, the device numerical simulation is built to reproduce the physical and electrical characteristics of the CMOS inverter under soft logic upset, and then a digital filter model is used to obtain the soft upset output logic level. And a static parameter extraction method in simulation is proposed to further understand the interference in device performance. The influences on EMI frequency and device size are studied using the same model, concluding that lower frequency of EMI and smaller size of inverter are more susceptible to the EMI induced soft logic upsets. The results are supported by the reported experimental results. The simulation model reduces the cost of experiments and provides a new idea for further studies.

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