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Total Ionizing Dose Effects of 55-nm Silicon-Oxide-Nitride-Oxide-Silicon Charge Trapping Memory in Pulse and DC Modes *

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The ^{60}Co-γ ray total ionizing dose radiation responses of 55-nm silicon-oxide-nitride-oxide-silicon (SONOS) memory cells in pulse mode (programmed/erased with pulse voltage) and dc mode (programmed/erased with direct voltage sweeping) are investigated. The threshold voltage and off-state current of memory cells before and after radiation are measured. The experimental results show that the memory cells in pulse mode have a better radiation-hard capability. The normalized memory window still remains at 60% for cells in dc mode and 76% for cells in pulse mode after 300 krad(Si) radiation. The charge loss process physical mechanisms of programmed SONOS devices during radiation are analyzed.

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With advantages of discrete charge storage, low power, low cost, high speed, and good retention/endurance performance, the charge-trapping memory, such as silicon-oxide-nitride-oxide-silicon (SONOS) technology has piqued increasing interests in the semiconductor industry to meet the formidable challenges of scaling-down.[1] The radiation-hard capability is crucial to charge-trapping memory aiming at harsh environment application like space explorations. There exist various previous publications on the impact of the charge-trapping memory's structures,[2,3] materials,[4,5] and technology node[6,7] on its responses with different radiation sources. Diversified results were shown in these previous reports on the total ionizing dose (TID) responses of charge trapping memory (CTM),[6,8] which may be due to the fact that these researches were carried out without considering the impact of the memory cell's operation modes. It is necessary to study the radiation tolerance differences of memory cells operating in pulse and dc modes.

The ultra-thin tunnel oxide layer of CTM cells can easily be degraded due to hole generation and trapping in the bulk oxide together with the interface state generation between silicon and tunnel oxide, for which the high electric field during program and erase operations is responsible.[9−11] The stored charge may escape from the storage layer by the trap-assisted tunneling (TAT) mechanism with the help of oxide traps and interface states. On the one hand, the data retention reliability is worsened;[12] on the other hand, those oxide traps and interface states have a significant influence over the radiation tolerance of memories.[13,14] The traps and interface states generation rates vary from operation/stress modes, such as pulse and dc.[15−17] Therefore, it is necessary to study the impacts of charge-trapping memory's operation modes on its radiation-hard performance.

In this work, we investigate the effects of TID irradiation on 55 nm SONOS memory cells operating in pulse and dc modes, focusing on the threshold voltage ($V_{\rm th}$), memory window (MW) shifts, and off-state leakage current ($I_{\rm off}$), followed by a detailed discussion on the underlying charge loss mechanism of the programmed SONOS device during irradiation.

The device under test (DUT) is a 2 × 2-bit NOR-type flash memory mini-array. Among the DUT, each memory cell consists of a 2T-stacked structure, which is a memory transistor (MT) in series with a select transistor (ST). The schematic diagram of the mini-array and the transmission electron microscope (TEM) cross section of a memory cell are presented in Fig. 1. The electron beam of TEM is incident into the SONOS memory cell perpendicular to the channel and the surface of the measured sample. As shown in Fig. 1, there are five terminals (WLS/G, WL, BL/D, SL and B) for every memory cell, in which G and D represent gate and drain terminals of the memory transistor, respectively. The memory transistor is an SONOS device, featured by a multi-dielectric gate insulator consisting of a tunnel oxide/storage nitride/blocking oxide (ONO) sandwich with charge storage in discrete traps in the silicon nitride layer.[19] The DUTs in this work are manufactured by us-

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ing an ultra-low-power 55-nm complementary-metal-oxide-semiconductor (CMOS) logic technology node with 3-extra masks and relevant process modules. The specific layers' thickness of the ONO stack cannot be shown clearly due to being commercial confidential. The select transistor is also an n-channel transistor. All I_d–V_g curves from the memory transistor are measured with the selected transistor remaining in the ON state.

The basic electric characterization is performed by an Agilent B1500A semiconductor device analyzer at room temperature. With terminal B floating, the memory cells are programmed/erased with the Fowler–Nordheim (FN) tunneling mechanism with operating conditions demonstrated in Table 1. Two different operating modes are utilized to evaluate various impacts of stress modes on the memory cell's TID effects.[12] The memory cell is programmed/erased with direct voltage sweep (7 V/−7 V) in dc mode and 7 V/−7 V for 2 ms/6 ms duration in pulse mode. The I_d–V_g curves are obtained by the READ operation under a drain bias of 0.6 V. Figure of merits in this study are defined as follows: V_{th} is the gate voltage while the drain current of the memory transistor is 1 μA ($I_d = 1$ μA) with $V_d = 0.6$ V, MW is determined by the V_{th} difference between programmed and erased cells, and I_{off} is defined as the drain voltage at zero gate bias (I_d@$V_g = 0$ V) with $V_d = 0.6$ V.

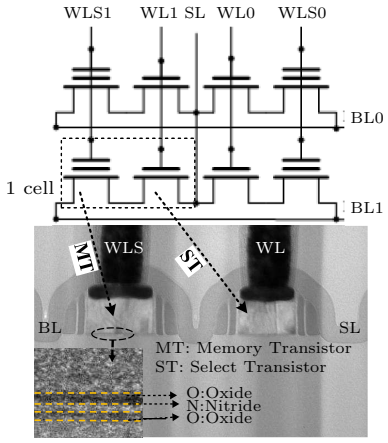

Fig. 1. Simplified schematic of the 2×2 mini-array and the corresponding TEM cross section of one-bit cell, consisting of a memory transistor (SONOS) and a select transistor. The blocking oxide/storage nitride/tunnel oxide (ONO) layers of the SONOS device are clearly shown in the lower TEM picture. The specific size information of each layer cannot be shown clearly due to being commercially confidential.

Table 1. Definition of operation conditions. VG and VD represent the gate and drain voltages of the memory transistor, respectively.

Operation	V_{WLS}/V_G	V_{WL}	V_{BL}/V_D	V_{SL}	Time
PGM	7 V	0 V	0 V	0 V	2 ms
ERS	−7 V	0 V	0 V	0 V	6 ms
READ	−3–3 V	2.5 V	0.6 V	0 V	

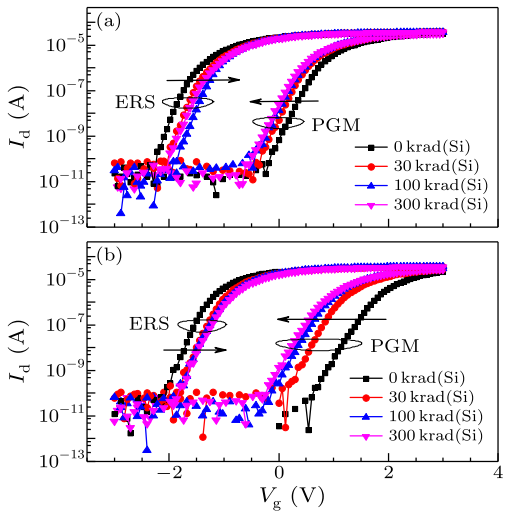

Fig. 2. The I_d–V_g curves of the memory cells under TID radiation: (a) P/E in pulse mode, and (b) P/E in dc mode before and after radiation.

The TID radiation experiments were conducted with the ^{60}Co gamma source in Peking Normal University with the dose rate as 50 rad(Si)/s, in which DUTs were placed during radiation. Time intervals for electrical measurements between irradiation exposures are within the limits stated in MIL-STD-883D Test Method 1019.4 (one hour after exposure to start electrical characterization and two hours to begin the next exposure). The total dose steps are 30 krad(Si), 100 krad(Si), and 300 krad(Si), respectively.

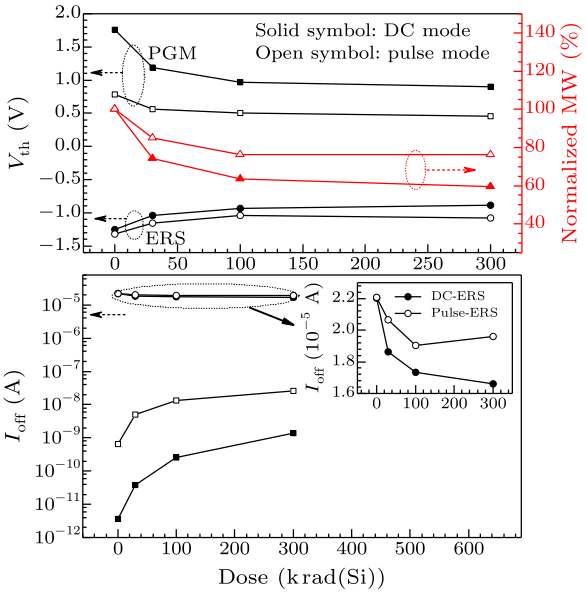

Fig. 3. (a) The value of V_{th} and normalized MW shifts of memory cells for both programmed state (PGM) and erased state (ERS) with pulse mode (open symbol) and dc mode (solid symbol) before and after radiation. (b) The logarithm plot of I_{off} versus radiation dose for PGM and ERS. The inset shows the linear plot of I_{off} versus radiation dose for ERS.

Figure 2 shows a set of I_d–V_g curves with different levels of radiation dose for memory cells in pulse mode (Fig. 2(a)) and dc mode (Fig. 2(b)). No bias is applied to the memory cells during radiation to avoid long time stress and disturbance. In both modes, the I_d–V_g curves of the programmed cell shift toward the negative direction while those of the erased cell shift toward the positive direction after radiation. The V_{th} shifts and the MW variation due to TID radiation for both programmed and erased states with pulse and dc modes are shown in Fig. 3(a) to make a direct comparison among the radiation-hard capability of memory cells.

It is worth noting that V_{th} of the programmed cell in dc mode is much larger than that in pulse mode before radiation. It is generally acknowledged that V_{th} of the memory transistor rises with the increase of the programming stress time due to more charge crossing the tunnel oxide and injecting into the charge storage layer.[1] The initial V_{th} difference is caused by a longer high-field stress time in dc mode during program operation. However, the high electric field stress can also incur a reliability issue that traps and interface states will be generated by the tunneling electron after gaining enough energy from the stressing electric field.[17,19] As a result, the reliability of the memory cell may be lowered.

As shown in Fig. 3(a), V_{th} of the programmed memory cells in dc mode drifts down from 1.76 V to 0.9 V after 300 krad(Si) radiation. By contrast, the programmed memory cells in pulse mode only observes a drift from 0.78 V to 0.46 V. Similarly, V_{th} of the erased memory cells in dc mode goes up from −1.25 V to −0.89 V, while V_{th} of the erased cells in pulse mode goes up from −1.32 V to −1.08 V. No matter for pulse or dc mode, the highest degradation rate (14.85% in pulse mode and 25.65% in dc mode) of MW happened before 30 krad(Si), while the lowest one (1.3% in pulse mode and 6.29% in dc mode) happened between 100 krad(Si) and 300 krad(Si), which can be attributed to the relatively easier initial loss of stored charges in the shallow energy traps and the charge redistribution.[8] Shallow energy traps in SONOS devices are good in terms of the program and erase speed, but bad for retention and anti-TID performance. The degradation in V_{th} leads to MW shrinking. The normalized MW for cells in pulse mode remains at 76%, while the cells in dc mode only remain at 60% after 300 krad(Si).

In addition to V_{th} shifts, the memory cells also experienced several orders magnitude of I_{off} increase for programmed cells and a slight I_{off} decrease for erased cells, as shown in Fig. 3(b). After 300 krad(Si) radiation, I_{off} is approximately 3 orders of magnitude higher than the corresponding pre-radiation one for the programmed memory transistor in dc mode, while only 2 orders higher than that in pulse mode. Here I_{off} of the erased memory transistor decreases from 22 μA to 16.6 μA in dc mode, and decreases from 22 μA to 19.6 μA in pulse mode. The experimental results show that the memory transistor in pulse mode has a better radiation-hard capability than that in dc mode. In general, flash memory array works in pulse mode.[6,8] For the performance evaluation of memory cells in an array, the TID testing results based on memory cells in pulse mode may be more reliable and practical than those in dc mode.

The electrical responses of the programmed memory transistors caused by radiation can be explained by physical processes as shown in Fig. 4.[20,21]

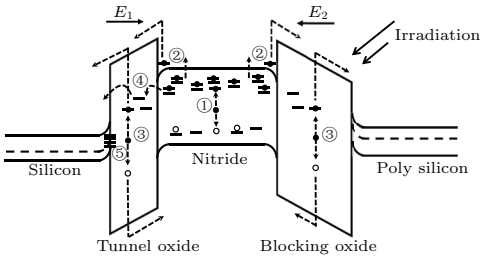

Fig. 4. Physical mechanisms involved in the programmed state of the SONOS device under TID irradiation: (1) electron-hole pairs are generated in the nitride layer; (2) electrons emission over the nitride/oxide barriers; (3) electron-hole pairs are generated in the tunnel oxide and blocking oxide; (4) traps existing in the tunnel oxide assist electrons conducting from the nitride layer to silicon; and (5) the interface states are generated at the silicon/tunnel oxide interface (channel region).

Process 1: Electron-hole pairs are generated in the nitride layer during radiation, in which the generated charge carriers recombine partially afterwards, and the build-in electric field (E_1/E_2) induced by trapped electrons acts to sweep remaining mobile electrons out of the nitride layer, and to contain remaining holes in the nitride. In addition, the nitride has a higher trapping probability for holes than electrons.[6,21] These reasons explain the buildup of positive charge in the nitride, while there still exists net negative charge due to electron storage.

Process 2: Trapped electrons, capable of absorbing energy from radiation and being emitted to the conduction band of the nitride, continue to absorb energy from radiation till they obtain sufficient energy to overcome the nitride/oxide barrier of 3.1 eV.

Process 3: The radiation-generated electron-hole pairs in the tunnel/blocking oxide recombine partially in the first picosecond. Then, being more mobile than remaining holes, remaining electrons are swept away toward substrate silicon/poly silicon due to built-in electric field (E_1/E_2). The holes are relatively immobile and remain near the region of generation or tend to shift toward the oxide/nitride interface.

Process 4: Absorbing energy from radiation and emitted to the traps in the tunnel oxide at first, then electrons in the nitride traps can hop through the oxide traps to the substrate silicon.

Process 5: The interface states, generated by high-electric field or radiation at the silicon/tunnel oxide interface can act as donors or acceptors to trap holes or electrons. The interface states generation also results in an increase in the subthreshold slope (SS).

These processes have caused $V_{\rm th}$ of the programmed memory transistor and MW to decrease with radiation dose. For an erased memory transistor with excess holes in the nitride layer, the direction of the built-up electric field (E_1/E_2) is from nitride to subsilicon/poly silicon. As a result, a higher trapping rate of holes for nitride and the electric field pointing out of nitride work against each other in process 1.[6] In addition, the radiation was responsible for charge loss in the nitride (processes 2 and 4) and the accumulation of positive charges in the surrounding oxide (process 3) also tend to cancel each other out resulting in a relatively small shift of $V_{\rm th}$.[21]

As mentioned above, traps and interface states will be generated during the program/erase operation. The $I_{\rm d}$–$V_{\rm g}$ curves of memory cells in both pulse and dc modes shift in a mostly parallel manner with the increase of the total dose, resulting in a slight change in the SS. The interface states generation is minimal, which explains that the radiation-hard capability difference between memory transistors in pulse and dc modes is mainly caused by tunnel oxide traps generation.[19] As to the PGM case, the loss of trapped electrons in the storage nitride becomes easier during radiation for the existing of tunnel oxide traps (process 4).[20,21] From this perspective, improving the quality of the tunnel oxide is beneficial for improving the radiation-hard capability of SONOS memory cells. As far as is known, the incorporation of nitrogen and fluorine into the tunnel oxide[22] can effectively reduce the generation of oxide traps and interface states. Moreover, the trap level distribution of nitride can be adjusted by changing the proportion of Si and N in the nitride material.[23] In this way, the deep level traps increase while the shallow ones decrease, which can also increase the radiation-hard capability of the SONOS memory cell.

In summary, the radiation-hard capability of 55-nm SONOS memory cells in pulse and dc modes has been investigated. It is found that the characteristics of memory transistors in dc mode suffered more degradation than that in pulse mode, for which more tunnel oxide traps that are generated in the memory transistor in dc mode are mainly responsible. Acting as intermediate tunneling sites, this makes it easier for stored charges escaping from the nitride traps during radiation. The conclusion can be drawn that the radiation-hard capability of memory cells in pulse mode is better than that in dc mode. From the circuit perspective, as it works in pulse mode, a simple dc mode for the TID evaluation of the SONOS memory cell would overestimate the performance degradation.

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