Ohmic Contact at Al/TiO_2/n-Ge Interface with TiO_2 Deposited at Extremely Low Temperature *

Yi Zhang(张译), Gen-Quan Han(韩根全)**, Yan Liu(刘艳),
Huan Liu(刘欢), Jin-Cheng Zhang(张进成), Yue Hao(郝跃)

Key Laboratory of Wide Band-Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071

(Received 12 October 2017)

TiO_2 deposited at extremely low temperature of 120°C by atomic layer deposition is inserted between metal and n-Ge to relieve the Fermi level pinning. X-ray photoelectron spectroscopy and cross-sectional transmission electron microscopy indicate that the lower deposition temperature tends to effectively eliminate the formation of GeO_x to reduce the tunneling resistance. Compared with TiO_2 deposited at higher temperature of 250°C, there are more oxygen vacancies in lower-temperature-deposited TiO_2, which will dope TiO_2 contributing to the lower tunneling resistance. Al/TiO_2/n-Ge metal-insulator-semiconductor diodes with 2 nm 120°C deposited TiO_2 achieves 2496 times of current density at −0.1 V compared with the device without the TiO_2 interface layer case, and is 8.85 times larger than that with 250°C deposited TiO_2. Thus inserting extremely low temperature deposited TiO_2 to depin the Fermi level for n-Ge may be a better choice.

PACS: 85.30.Hi, 85.30.De, 85.30.Kk, 85.30.Tv DOI: 10.1088/0256-307X/35/2/028501

Germanium (Ge) is considered as one of the most promising candidates to replace silicon for advanced nano-scaled CMOS applications because of its high carrier mobility. However, there are some problems such as significant drive current reduction for metal to n-Ge contact.[1,2] One reason for this has been the strong Fermi level pinning (FLP) induced by high electron Schottky barrier height (eSBH).[3,4]

It has been reported that the FLP at metal/n-Ge could be relieved by inserting a thin tunneling layer such as Al_2O_3,[5] GeO_2,[6] SiN,[7] ZnO[8] and TiO_2[9,10] between metal and semiconductor. Although the eSBH can be reduced with interface layers (ILs) such as Al_2O_3, GeO_2 and SiN, the devices will exhibit the large tunneling resistance because of large conduction band offset (CBO) between ILs and Ge. An important aspect to obtain the low contact resistance at metal/n-Ge interface is to choose a material with proper CBO to n-Ge, and thus ZnO and TiO_2, both have smaller CBO than Ge, are preferred. TiO_2 has shown promising performance, and thermal stability for TiO_2 inserted structure can be improved by post plasma nitridation treatments.[11] For the deposition of TiO_2, atomic layer deposition (ALD) is preferred for its better thickness controllability and uniformity. However, GeO_x will be formed inevitably during the thermal TiO_2 ALD process, which will severely degrade metal-insulator-semiconductor contact characteristics, and high resistance GeON may be formed after plasma nitridation. Thus ALD process for TiO_2 deposition needs to be optimized to eliminate the formation of a GeO_x layer.

In this work, TiO_2 is deposited by thermal ALD at 120℃ and 250℃. Chemical compositions of TiO_2/Ge, structures and electrical properties of Al/TiO_2/Ge contact are studied.

The starting wafers were commercially 4-inch n-Ge with an arsenic (As) dopant concentration of about $1 \times 10^{17}\,\mathrm{cm}^{-3}$. After cleaning using a 5% HF solution for 3 min and de-ionized water rinse for 1 min, the samples were immediately loaded into a PicosunTM R-200 advanced atomic layer deposition (ALD) chamber. Titanium tetrakis (dimethylamide) (TDMA-Ti) and H_2O were used as the titanium (Ti) and the oxygen sources, respectively. TiO_2 films were deposited at 120℃ and 250℃. Aluminum (Al) was deposited using the reactive ion sputtering at room temperature. Then, standard lithography was performed to pattern Al electrodes. To eliminate any current leakage between adjacent structures through the TiO_2 film, the samples were etched utilizing argon plasma to remove the exposed TiO_2 film. Finally, 200 nm Al was also deposited on the back side of the samples for the better contact.

X-ray photoelectron spectroscopy (XPS) was used to characterize the stoichiometry and quality of the layers. Electrical performance of the devices was characterized with a Keithley 4200 SCS.

The stoichiometry of GeO_2 was investigated by XPS measurement, and O 1*s* peaks and Ge 3*d* of the samples are illustrated in Figs. 1 and 2, respectively. The peaks were calibrated using adventitious C 1*s* of 284.6 eV. Figure 1(a) shows the O 1*s* peaks for samples deposited at different temperatures. Peaks at 530 eV

*Supported by the National Natural Science Foundation of China under Grant Nos 61534004, 61604112 and 61622405.
**Corresponding author. Email: hangenquan@ieee.org

are consistent with typical O 1s value of TiO_2, which represent binding oxygen atoms.[12] For the sample deposited at 120℃, an obvious shoulder left of the 530 eV peak is observed. From the deconvoluted fitting spectra in Fig. 1(b), it is clear to see that the shoulder is located at 531.5 eV, which represents non-lattice oxygen atoms or oxygen vacancies. The vacancies may distribute in the TiO_2 layer, which act as donors and make TiO_2 more electrically conductive.[12]

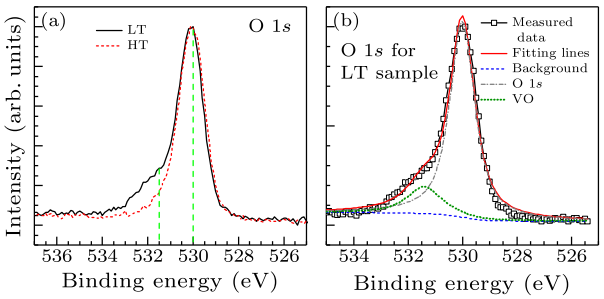

Fig. 1. XPS results of O 1s: (a) comparison of low-temperature and high-temperature deposited samples, and (b) the low-temperature sample with peaks fitting.

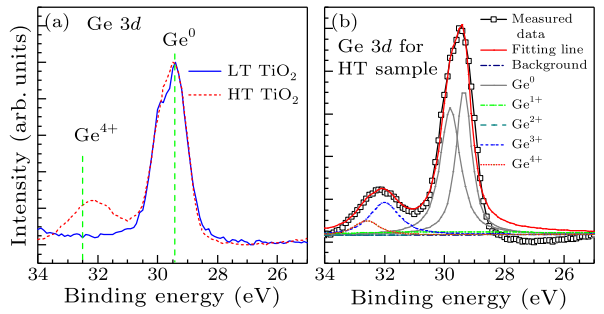

Fig. 2. XPS results of Ge 3d: (a) comparison of low-temperature and high-temperature deposited samples, and (b) the high-temperature sample with peaks fitting.

Figure 2(a) illustrates the Ge 3d spectra for the samples. A peak at 29.4 eV corresponding to the Ge–Ge bonds is observed.[13] Moreover, there is an obvious peak located at about 32 eV, indicating the oxides of Ge for the sample deposited at 250℃. Peak fitting of Ge 3d spectra for the sample deposited at 250℃ in Fig. 2(b) indicates that during the deposition process, Ge was oxidized, leading to the formation of Ge–O bonds. However, the composition of Ge^{4+} is much smaller than that of lower state ones. During the ALD deposition, two processes tend to form GeO_x, one is Ge directly reacting with oxygen source, and the other is the oxygen diffusing from TiO_2 to GeO_x due to dipole between TiO_2 and GeO_x. Both processes are sensitive to the deposition temperature. Higher temperature promotes the reaction of Ge and oxygen source and enhances the diffusion of oxygen from TiO_2 to GeO_x, and thus there is more GeO_x for the sample deposited at 250℃ compared with the sample deposited at 120℃. Deposition of TiO_2 at lower temperature can effectively suppress the GeO_x formation. Since the energy for forming GeO_2 is much larger than that of GeO, higher state GeO_x formation was limited. It was reported that a high oxidation state GeO_x layer between TiO_2 and Ge may improve it, thus improving Fermi level pinning, but in our higher temperature case, GeO_x is in the lower oxidation states. Thus this GeO_x layer will not effectively passivate the Ge surface.[14]

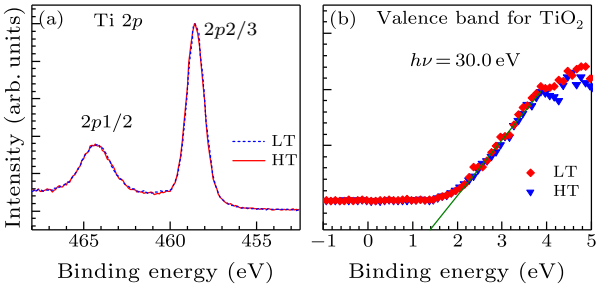

Fig. 3. XPS results of (a) Ti 2p and (b) valence band for TiO_2 of low-temperature and high-temperature samples.

Figure 3(a) shows the Ti 2p peaks for the samples with TiO_2 deposited at 120℃ and 250℃. The samples have two peaks located at 458.6 eV and 464.3 eV, which correspond to the Ti 2p3/2 and Ti 2p1/2 peaks, respectively. Figure 3(b) depicts the valence bands for the samples, and the phonon energy is 30 eV. There is no obvious difference between the two curves in the steepest range. Since valence band offset (VBO) of Ge/TiO_2 is the difference between Ge core level and valence band of TiO_2, we believe that VBO difference for both the samples may be smaller than the detection error.

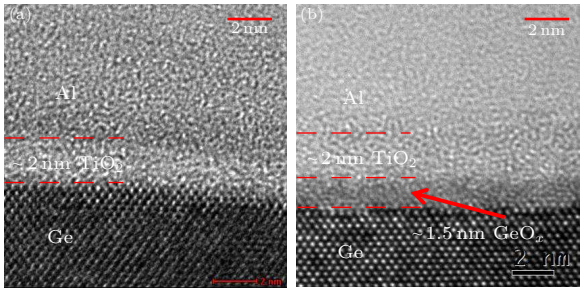

Fig. 4. HRTEM image of 30 cycles of (a) low-temperature and (b) high-temperature TiO_2 samples deposited on n-Ge.

To visualize the interface structures for both the samples and to confirm the thickness of interfacial layers, results of the high resolution transmission electron microscopy (HRTEM) of the samples are shown in Fig. 4, and clear Ge lattice can be observed. For the sample deposited at 250℃, there are distinctly two layers. Combining with the XPS results shown in Fig. 2, it is inferred that the layers are TiO_2 and GeO_x, and the thicknesses are 2 nm and 1.5 nm, respectively. For the lower-temperature-deposited sample, only one obvious layer between Al and Ge with thickness of

about 2 nm is observed based on the HRTEM contrast. Combining with the XPS results, it is inferred that the layer may be TiO_2. However, it should be noted that there may still exist a small content of low oxidation state GeO_x, since Ge is directly in contact with TiO_2, which is an oxide. Compared with the high-temperature sample, the GeO_x content is less, thus it may not be observed from the HRTEM results.

Both high-temperature and low-temperature deposited TiO_2 may be in the form of amorphous, as depicted from the HRTEM results. Aarik *et al.* reported that ALD deposited TiO_2 is amorphous with deposition temperature lower than 165℃,[15] which is consistent with the low-temperature TiO_2 HRTEM results. Though there are some conclusions that ALD deposited TiO_2 at high temperature such as 250℃ is in anatase phase,[16,17] there is an incubation layer for ALD deposited TiO_2 with thickness of more than 20 nm, and if the deposited TiO_2 is too thin, it may be in the form of amorphous,[18,19] which is why the 2 nm high-temperature TiO_2 sample in this work is amorphous. It was reported that the band gap for amorphous TiO_2 would vary from 3.3 to 3.5 eV.[20] Since there is no difference in VBO for low-temperature and high-temperature samples, the conduction band offset (CBO) difference of Ge/TiO_2 for low-temperature and high-temperature samples is less than 0.2 eV.

Combining the XPS and TEM results shown above, we obtain that lower deposition temperature may eliminate GeO_x formation. It should be noted that GeO_x is mainly formed during the ALD deposition process, i.e., at high temperature and not after deposition. Though part of the oxygen atoms diffused to the interface during the high temperature ALD process, oxygen source is abundant, and Ti atoms may be more reactive to grasp oxygen atoms from oxygen source and form higher valence state TiO_2. Though part of the oxygen diffused to form GeO_x, oxygen vacancies would be much less compared with the low-temperature sample.

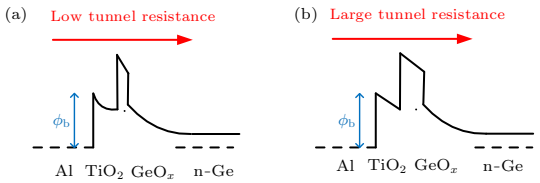

Fig. 5. Simplified energy band diagrams of Al/ALD TiO_2/n-Ge with TiO_2 deposited at (a) low temperature and (b) high temperature.

Figure 5 shows the simplified energy band diagrams of $Al/TiO_2/GeO_x$/n-Ge for low-temperature and high-temperature depositions. Such conclusions are considered: (1) difference in CBO at the TiO_2/Ge interface. CBO for the low-temperature sample is larger than that for the high-temperature sample, and the difference is less than 0.2 eV. (2) Difference in doping concentration of TiO_2. Low-temperature TiO_2 is rich in oxygen vacancies and is n-type doped, thus the barrier of low-temperature TiO_2 is thinner, and the tunneling resistance across TiO_2 is smaller. (3) Difference in fixed charges in TiO_2. There are more positive fixed charges in low-temperature TiO_2.[21] These positive charges increase the amount of potential dropped across the IL to reduce the n-Ge depletion charge, thus the barrier height reduced.[22] (4) Difference in the thickness of GeO_x formed during deposition process. This GeO_x layer would introduce large tunneling resistance, and the resistance is smaller for the low-temperature TiO_2 inserted sample.

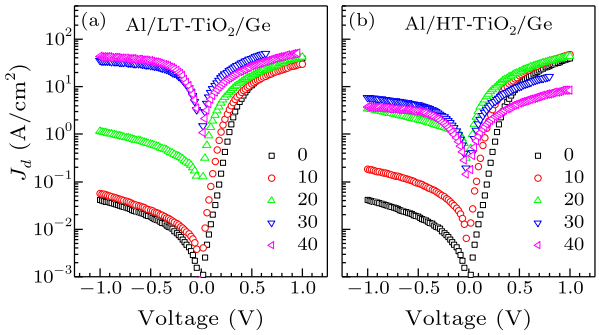

Fig. 6. The J–V characteristics of Al/ALD TiO_2/n-Ge with TiO_2 deposited at (a) low temperature and (b) high temperature with different ALD cycle numbers.

Figure 6 depicts the J–V curves for Al/TiO_2/n-Ge metal-insulator-semiconductor diodes with TiO_2 grown at low-temperature and high-temperature. Compared with diodes without the IL, diodes with 10 cycles TiO_2 samples exhibits improvement in the reverse current density J_R for both the samples, while the sample with the high-temperature IL has the larger J_R compared with the low-temperature sample. The same trend is observed for the 20-cycle samples. When increased to 30 cycles, J_R for the low-temperature sample increases much more than the high-temperature sample, and J_R for the low-temperature is larger than the high-temperature sample. The forward current density J_F for the high-temperature sample starts to decrease while this tendency does not come for the low-temperature sample until the 40-cycle one. For the 40-cycle samples, J_R for the low-temperature sample still shows the increase while for the high-temperature sample it drops. For both the samples with 40 cycles, J_F decreases, while the high-temperature sample shows larger series resistance. For the low-temperature-deposited TiO_2, the largest current density is achieved with 40-cycle TiO_2, and the current density increases by 2496 times compared with the device without the TiO_2 IL. The current density for the 40-cycle low-temperature-deposited sample is 8.85 times larger than the largest current density achieved by inserting 20 cycles of high-

temperature TiO_2.

It is more like an 'ideal' case that the samples are inserted with low-temperature TiO_2, since the GeO_x does not take much part in the mechanism of FLP because it is thin enough. Thus the J–V curves for low-temperature samples with different cycles are only affected by the characteristics of TiO_2, such as the thickness, the doping concentration of TiO_2, and the fixed charges in TiO_2. However, for the high-temperature samples the existence of GeO_x makes the metal-insulator-semiconductor mechanism complicated, since the GeO_x affects the depletion width in n-Ge and the tunneling resistance, and it affects more with thicker GeO_x, i.e., more ALD cycles.

In conclusion, deposition temperature for thermal ALD TiO_2 has a great influence on the electrical performance of Al/TiO_2/n-Ge metal-insulator-semiconductor contacts. It is found that after 30 cycles of high-temperature ALD deposition, there is about a 1.5 nm GeO_x layer between TiO_2 and Ge, and the GeO_x layer is in low valence state. However, there is no obvious GeO_x layer after the low-temperature deposition process, as confirmed by both TEM and XPS. Both the TiO_2 samples are amorphous, and the thickness of TiO_2 for both the cases is about 2 nm. However, there are oxygen vacancies in low-temperature-deposited TiO_2, which act as donors in TiO_2, while there is no obvious oxygen vacancy evidence for the high-temperature-deposited sample. There is no obvious difference in valence band offset, indicating that the conduction band offset difference is due to the difference of the low-temperature and high-temperature TiO_2 band gaps, and the CBO difference is less than 0.2 eV. Electrical characteristics indicate that both the cases can improve contact characteristics, but the samples inserted with 30- and 40-cycle low-temperature TiO_2 show the larger current density. The largest current density at -0.1 V is achieved by inserting the 40-cycle low-temperature TiO_2, and the current density increases by 2496 times compared with the device without the TiO_2 IL case. Though the high-temperature TiO_2 shows the less CBO with Ge, the GeO_x layer increases the series resistance and severely degrades the electrical characteristics of Al/ALD TiO_2 IL/n-Ge metal-insulator-semiconductor contacts. Thus inserting extremely low-temperature-deposited TiO_2 to depin FL for n-Ge may be a better choice.

References

[1] Xie R, Phung T H, He W, Yu M and Zhu C 2009 *IEEE Trans. Electron Devices* **56** 1330
[2] Kuzum D, Krishnamohan T, Nainani A, Sun Y, Pianetta P, Wong H and Saraswat K C 2011 *IEEE Trans. Electron Devices* **58** 59
[3] Dimoulas A, Tsipas P, Sotiropoulos A and Evangelou E 2006 *Appl. Phys. Lett.* **89** 252110
[4] Nishimura T, Kita K and Toriumi A 2007 *Appl. Phys. Lett.* **91** 123123
[5] Zhou Y, Ogawa M, Han X and Wang K 2008 *Appl. Phys. Lett.* **93** 202105
[6] Nishimura T, Kita K and Toriumi A 2008 *Appl. Phys. Express* **1** 051406
[7] Connelly D, Faulkner C, Clifton P and Grupp D 2006 *Appl. Phys. Lett.* **88** 012105
[8] Manik P, Mishra R, Kishore V, Ray P, Nainani A, Huang Yi, Abraham M, Ganguly U and Lodha S 2012 *Appl. Phys. Lett.* **101** 182105
[9] Lin J, Roy A, Nainani A, Sun Y and Saraswat K C 2011 *Appl. Phys. Lett.* **98** 092113
[10] Kim G, Kim J, Kim S, Jo J, Shin C, Park J, Saraswat K C and Yu H 2014 *IEEE Electron. Devices Lett.* **35** 1076
[11] Biswas D, Biswas J, Ghosh S, Wood B and Lodha S 2017 *Appl. Phys. Lett.* **110** 052104
[12] Wang G, Wang H, Ling Y, Tang Y, Yang X, Fitzmorris R, Wang C, Zhang J and Li Y 2011 *Nano Lett.* **11** 3026
[13] Zhang L, Li H, Guo Y, Tang K, Woicik J, Robertson J and McIntyre P 2015 *ACS Appl. Mater. Interfaces* **7** 20499
[14] Kita K, Wang S K, Yoshida M, Lee C H, Nagashio K, Nishimura T, Toriumi A 2009 *Electron Devices Meeting, IEEE International* (Baltimore, MD, USA 7–9 December 2009) p 693
[15] Aarik J, Aidla A, Kiisler A, Uustare T and Sammelselg V 1997 *Thin Solid Films* **305** 270
[16] Kim G, Kim S, Kim S, Park J, Seo Y, Cho B, Shin C, Shim J and Yu H 2016 *ACS Appl. Mater. Interfaces* **8** 35419
[17] Gupta S, Manik P, Mishra R, Nainani A, Abraham M and Lodha S 2013 *J. Appl. Phys.* **113** 234505
[18] Strobel A, Schnabel H, Reinhold U, Rauer S and Neidhardt A 2016 *J. Vac. Sci. Technol.* A **34** 01A118
[19] Puurunen R L, Sajavaara T, Santala E, Miikkulainen V, Saukkonen, Laitinen M and Leskelä M 2011 *J. Nanosci. Nanotechnol.* **11** 8101
[20] Figgemeiera E, Kylberga W, Constablea E, Scarisoreanub M, Alexandrescub R, Morjanb I, Birjegab R, Popovicib E, Fleacab C, Gavrila F L and Prodan G 2007 *Appl. Surf. Sci.* **254** 1037
[21] Nasim F, Ali A, Bhatti A S and Naseem S 2011 *J. Appl. Phys.* **110** 114517
[22] Hu J, Nainani A, Sun Y, Saraswat K C and Wong H 2011 *Appl. Phys. Lett.* **99** 252104