Concise Modeling of Amorphous Dual-Gate In-Ga-Zn-O Thin-Film Transistors for Integrated Circuit Designs *

Can Li(李璨), Cong-Wei Liao(廖聪维)**, Tian-Bao Yu(于天宝), Jian-Yuan Ke(柯建源), Sheng-Xiang Huang(黄生祥), Lian-Wen Deng(邓联文)

School of Physics and Electronics, Central South University, Changsha 410083

(Received 29 August 2017)

An analytical model for current–voltage behavior of amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) with dual-gate structures is developed. The unified expressions for synchronous and asynchronous operating modes are derived on the basis of channel charges, which are controlled by gate voltage. It is proven that the threshold voltage of asynchronous dual-gate IGZO TFTs is adjusted in proportion to the ratio of top insulating capacitance to the bottom insulating capacitance ($C_{\rm TI}/C_{\rm BI}$). Incorporating the proposed model with Verilog-A, a touch-sensing circuit using dual-gate structure is investigated by SPICE simulations. Comparison shows that the touch sensitivity is increased by the dual-gate IGZO TFT structure.

PACS: 73.40.Qv, 71.23.An, 85.60.Pg DOI: 10.1088/0256-307X/35/2/027302

Amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) show great potential for mass production of active matrix flat panel display (AMFPD),[1,2] owing to the high mobility, excellent uniformity, and low manufacturing cost.[3] In recent years, IGZO TFTs with dual-gate (DG) structure attract enormous attention, due to the improved electrical performance.[4,5] Baek *et al.* demonstrated that the threshold voltage of DG IGZO TFTs can be adjusted by changing base voltage.[6] Wang *et al.* showed a new AMOLED pixel circuit with DG IGZO TFTs.[7] However, few works have been involved for modeling of current–voltage characteristics of DG IGZO TFTs to date. Due to the lack of an analytical model, there are great difficulties to simulate DG IGZO TFT integrated circuits.

Recently, widespread attention has been paid to TFT integrated touch sensors for consuming electronics. Nakamura proposed an in-cell touch sensor array using LTPS TFTs, which showed a good measurement result.[8] However, the schematic seems slightly complicated, as many elements are required for sensing pixel circuit, such as a storing capacitance, a precharging, a reading-out TFT, and an amplifier circuit. Thus Cheu *et al.* proposed a simpler sensing pixel circuit where only four TFTs and one coupling capacitance were used.[9] In addition, Brown *et al.* proposed 1TFT-1capacitance touch sensing circuit with the LTPS TFT technology.[10] However, the research of touch sensor using IGZO TFTs is not enough, and specifically there are fewer studies on touch sensor using DG IGZO TFTs. Furthermore, as the requirements for the switching and driving transistors are different, the dimension and configuration for the DG IGZO TFTs should be carefully chosen.

Figure 1 shows the simplified cross sectional view of DG IGZO TFTs, and Table 1 lists the geometrical parameters. The active layer is controlled by two separated gates, i.e., bottom gate (BG) and top gate (TG).[11] In this study, floating gate effects are avoided because both the top and the bottom gate electrodes are connected with specific voltage source. As the two gates can be applied with the same or different controlling voltages, unified current–voltage expressions will be derived on the basis of channel charge–voltage relationship in the following.

Table 1. Geometrical parameters of dual-gate IGZO TFTs.

Parameter	Value
Top/bottom gate thickness (nm/nm)	100/100
Gate insulator thickness (nm)	200
IGZO layer thickness (nm)	30
Channel width/length (μm/μm)	60/10

The y direction is along the side of the IGZO film from the source to the drain electrodes. The channel length is L, and the thickness is $t_{\rm s}$ as shown in Fig. 1. Here $y = 0$ and $y = L$ indicate the regional boundary of channel to source and of channel to drain, $C_{\rm TI}$, $C_{\rm BI}$ and $C_{\rm dep}$ are the capacitance values per unit area for the top insulator, bottom insulator, and IGZO film, respectively.

The distribution of charges in the IGZO layer is dependent on the applied voltage on the gate electrodes. As shown in Fig. 1, the channel layer of DG TFTs is divided into the main and the sub channels. For the conventional single-gate (SG) IGZO TFTs with inverter staggered structure, which has been widely used for decades, the drain-to-source current can only flow through the main channel, which is solely controlled by the bottom gate. However, for DG IGZO TFTs, it is also possible that drain-to-source current flows through the sub channel in the case that the top-

*Supported by the National Key Research and Development Program of China under Grant No 2017YFA0204600, the National Natural Science Foundation of China under Grant No 61404002, and the Science and Technology Project of Hunan Province under Grant No 2015JC3041.

**Corresponding author. Email: hustliao@126.com

gate voltage ($V_{\rm TG}$) is larger than the threshold voltage of TG ($V_{\rm TT0}$). Furthermore, the charge distribution in the main channel will also be affected by the top gate if $V_{\rm TG} < V_{\rm TT0}$, and the threshold voltage will be adjusted accordingly. When $C_{\rm TI}$ and $C_{\rm dep}$ are in serial configuration, the charge in the main channel is influenced by the top gate through $C'_{\rm TI}$, which is approximately expressed as $C'_{\rm TI} = (C_{\rm TI}C_{\rm dep})/(C_{\rm TI}+C_{\rm dep})$.[12]

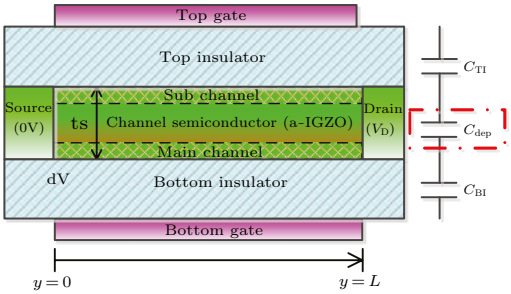

Fig. 1. Simplified cross-sectional view of dual-gate IGZO TFTs.

The drain-source current (i.e., $I_{\rm DS}$) of TFTs is in proportion to the electron velocity of the electron in the channel (i.e., $\mu_{\rm EF}(dV/dy)$, where $\mu_{\rm EF}$ is the effective field effect mobility). Therefore, the voltage drop is expressed as

$$dV = \frac{I_{\rm DS}dy}{W\mu_{\rm FE}|Q|}, \tag{1}$$

where dV is the voltage drop from y to $y+dy$, and W is the channel width. The value of Q represents the gate-induced charges, which can be expressed as[13]

$$Q = A[V_{\rm BG}-V_{\rm BT0}-V(y)] + B[V_{\rm TG}-V_{\rm TT0}-V(y)], \tag{2}$$

$$A = C_{\rm BI}\frac{{\rm sgn}V_{\rm BG}+1}{2} + \frac{C_{\rm BI}C_{\rm dep}}{C_{\rm BI}+C_{\rm dep}}\frac{1-{\rm sgn}V_{\rm BG}}{2}, \tag{3}$$

$$B = C_{\rm TI}\frac{{\rm sgn}V_{\rm TG}+1}{2} + \frac{C_{\rm TI}C_{\rm dep}}{C_{\rm TI}+C_{\rm dep}}\frac{1-{\rm sgn}V_{\rm TG}}{2}, \tag{4}$$

where $V_{\rm BT0}$ and $V_{\rm TT0}$ are the threshold voltages of the main and the sub channels, $V_{\rm BG}$ and $V_{\rm TG}$ are the voltages of BG and TG, respectively. The effective field mobility is dependent on gate voltage, and it is expressed as

$$\mu_{\rm FE} = \mu_{\rm BAND}(V_{\rm G}-V_{\rm FB})^{\gamma}, \tag{5}$$

where $V_{\rm FB}$ is the flat band voltage, $\mu_{\rm BAND}$ is the flat band mobility, $V_{\rm G}$ is the gate voltage, and γ is a material- and temperature-dependent parameter.[14]

Synchronous dual-gate mode means that the top gate electrode and the bottom gate electrode are connected (i.e., $V_{\rm BG} = V_{\rm TG} = V_{\rm G}$).

Substituting Eq. (2) into Eq. (1), and integrating Eq. (1) from $y = 0$ to $y = L$, the on-current is simplified to

$$I_{\rm DS} = \frac{W}{L}\mu_{\rm FE}(C_{\rm BI}+C_{\rm TI})\Big\{\Big[V_{\rm G} - \frac{(C_{\rm BI}V_{\rm BT0}+C_{\rm TI}V_{\rm TT0})}{C_{\rm BI}+C_{\rm TI}}\Big]V_{\rm DS} - \frac{1}{2}V_{\rm DS}^2\Big\}. \tag{6}$$

Here the effective gate capacitance of unit gate insulator area ($C_{\rm DI}$) is the total capacitance of top and bottom gate insulating layers ($C_{\rm BI}$ and $C_{\rm DI}$),

$$C_{\rm DI} = C_{\rm BI} + C_{\rm TI}, \tag{7}$$

and the effective threshold voltage ($V_{\rm DTH}$) is expressed as

$$V_{\rm DTH} = \frac{C_{\rm BI}V_{\rm BT0}+C_{\rm TI}V_{\rm TT0}}{C_{\rm BI}+C_{\rm TI}}. \tag{8}$$

Thus in the case of $V_{\rm DS} > V_{\rm G} - V_{\rm DTH}$, the drain-to-source current for saturation region is

$$I_{\rm DS} = \frac{W}{2L}\mu_{\rm FE}C_{\rm DI}(V_{\rm G}-V_{\rm DTH})^2(1+\lambda\cdot V_{\rm DS}), \tag{9}$$

where λ is the kink effect coefficient. For sub-threshold region, $I_{\rm sub}$ is determined by diffusion of gate-to-channel field and it is expressed as[15]

$$I_{\rm DS} = I_{\rm DG}\frac{W}{L}[1-e^{-(\ln 10)\frac{\theta_1 V_{\rm DS}}{{\rm SS}_{\rm DG}}}]e^{(\ln 10)\frac{\theta_2(V_{\rm G}-V_{\rm FB})}{{\rm SS}_{\rm DG}}}, \tag{10}$$

$${\rm SS}_{\rm DG} = \frac{k_{\rm B}T}{q}(\ln 10)\Big(1+\frac{C_{\rm dep}}{C_{\rm DI}}\Big), \tag{11}$$

where $I_{\rm DG}$ is the drain-source current at $V_{\rm G} = V_{\rm DTH}$, $SS_{\rm DG}$ is the sub-threshold swing of synchronous DG IGZO TFTs, θ_1 and θ_2 are the fitting parameters.

The leakage drain-source current is expressed as

$$I_{\rm DS} = G_{\rm DG}V_{\rm DS}\frac{W}{L}, \tag{12}$$

where $G_{\rm DG}$ is the conductivity coefficient for leakage region. To sum up, using the smoothing function $f(x,y) = [(x^m y^m)/(x^m+y^m)]^{1/m}$ and $\tanh(x)$,[16] the unified model for drain-to-source current of synchronous dual-gate IGZO TFTs can be expressed as

$$\begin{aligned} I_{\rm DS} = {} & \frac{W}{L}\mu_{\rm FE}C_{\rm DI}\frac{(V_{\rm G}-V_{\rm DTH})}{2}\Big([2V_{\rm DS}(V_{\rm G}-V_{\rm DTH}) \\ & - V_{\rm DS}^2]^m\Big\{\Big[2V_{\rm DS} - \frac{V_{\rm DS}^2}{(V_{\rm G}-V_{\rm DTH})}\Big]^m \\ & \cdot(1+\lambda V_{\rm DS})^{-m} + (V_{\rm G}-V_{\rm DTH})^m\Big\}^{-1}\Big)^{1/m} \\ & \cdot\Big[\frac{1+\tanh[\beta(V_{\rm G}-V_{\rm DTH})]}{2}\Big] \\ & + \Big\{I_{\rm DG}\frac{W}{L}[1-e^{-(\ln 10)\frac{\theta_1 V_{\rm DS}}{{\rm SS}_{\rm DG}}}] \\ & \ln[1+e^{\ln(10)\frac{\theta_2(V_{\rm G}-V_{\rm FB})}{{\rm SS}_{\rm DG}}}] + G_{\rm DG}V_{\rm DS}\frac{W}{L}\Big\} \\ & \cdot\Big[\frac{1-\tanh[\beta(V_{\rm G}-V_{\rm DTH})]}{2}\Big], \end{aligned} \tag{13}$$

where m is the smoothing parameter and β is the fitting parameter. Based on the derived current–voltage model, the output and transfer characteristic can be obtained by Hspice simulator incorporating the Verilog-A code. Comparisons between the calculation and the measurement are carried out as shown in Fig. 2.[17] As good agreements are obtained, the above derived analytical model is highly reliable.

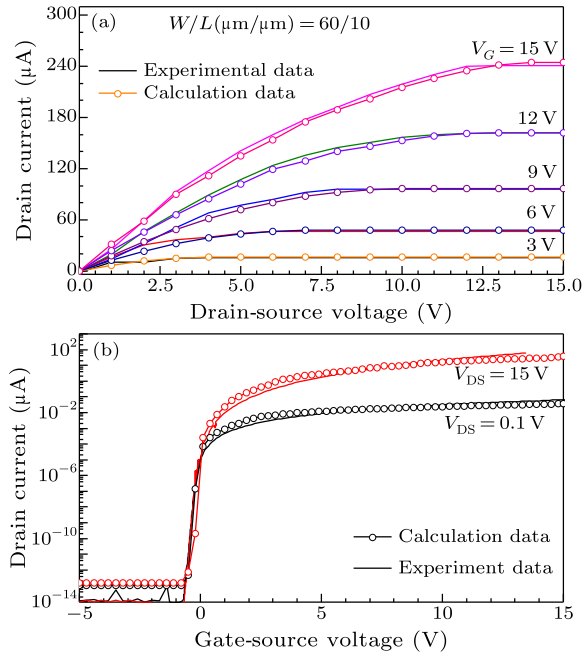

Fig. 2. Comparison of calculation and measurement electrical characteristic for synchronous dual-gate IGZO TFTs: (a) with output characteristic and (b) with transfer characteristic.

On the other hand, asynchronous dual-gate mode means that the top-gate electrode and the bottom-gate electrodes are biased independently. The IGZO channel is mainly controlled by the bottom gate, and the top gate is only used to adjust the threshold voltage linearly.

As listed in Table 1, the thickness of the IGZO layer is much smaller than the bottom- and top-gate insulators. Thus it is reasonable to assume $C_{dep} \gg C_{BI}$ or C_{TI}. Then the drain-to-source current behavior for the above threshold region is written as

$$I_{DS} = \frac{W}{L}\mu_{FE}\Big\{C_{BI}\Big[V_{BG} - V_{BT0} + \frac{C_{TI}}{C_{BI}}(V_{TG} - V_{TT0})\Big]V_{DS} - \frac{1}{2}(C_{BI} + C_{TI})V_{DS}^2\Big\}, \quad (14)$$

where the threshold voltage of asynchronous DG IGZO TFTs is defined as

$$V_{BTH} = V_{BT0} - \frac{C_{TI}}{C_{BI}}(V_{TG} - V_{TT0}). \quad (15)$$

In other words, the threshold voltage is linearly decreasing with the increases of the TG voltage, and the coefficient is C_{TI}/C_{BI}.

Therefore, in the case of $V_{DS} \geq (V_{BG} - V_{BTH})(C_{BI}/C_{DI})$, the saturation current of the device is expressed as

$$I_{DS} = \frac{W}{2L}\mu_{FE}\frac{C_{BI}^2}{C_{BI} + C_{TI}}(V_{BG} - V_{BTH})^2(1 + \lambda V_{DS}), \quad (16)$$

and the sub-threshold current is expressed as

$$I_{DS} = I_{BG}\frac{W}{L}e^{(\ln 10)\frac{\theta_2[V_{BG} - V_{FB} + \frac{C_{TI}}{C_{BI}}(V_{TG} - V_{TH0})]}{SS_{BG}}} \cdot [1 - e^{-(\ln 10)\frac{\theta_1 V_{DS}}{SS_{BG}}}], \quad (17)$$

$$SS_{BG} = \frac{k_B T}{q}(\ln 10)\Big(1 + \frac{C_{dep}}{C_{BI}}\Big), \quad (18)$$

where I_{BG} is the drain-source current at $V_{BG} = V_{BTH}$, and SS_{BG} is the sub-threshold swing of asynchronous DG IGZO TFTs.

Therefore, also using the smoothing function $f(x, y) = [(x^m y^m)/(x^m + y^m)]^{1/m}$, the unified model for drain-to-source current of asynchronous DG IGZO TFTs can be expressed as

$$\begin{aligned} I_{DS} = {} & \frac{W}{L}\mu_{FE}C_{BI}\frac{(V_{BG} - V_{BTH})}{2} \\ & \cdot \Big(\Big[2\frac{C_{BI}}{C_{BI} + C_{DI}}V_{DS}(V_{BG} - V_{BTH}) - V_{DS}^2\Big]^m \Big\{\Big[2V_{DS} - \frac{V_{DS}^2}{C_{BI}(V_{BG} - V_{BTH})}\Big]^m \\ & \cdot (1 + \lambda V_{DS})^{-m} + \frac{C_{BI}}{C_{BI} + C_{DI}}(V_{BG} - V_{BTH})^m\Big\}^{-1}\Big)^{\frac{1}{m}}\Big[\frac{1}{2} + \frac{\tanh[\beta(V_{BG} - V_{BTH})]}{2}\Big] \\ & + \Big(I_{BG}\frac{W}{L}[1 - e^{-(\ln 10)\frac{\theta_1 V_{DS}}{SS_{BG}}}] \\ & \cdot \ln\Big\{1 + e^{(\ln 10)\frac{\theta_2[V_{BG} - V_{FB} + \frac{C_{TI}}{C_{BI}}(V_{TG} - V_{TH0})]}{SS_{BG}}}\Big\} \\ & + G_{BG}V_{DS}\frac{W}{L}\Big)\Big(\frac{1 - \tanh[\beta(V_{BG} - V_{BTH})]}{2}\Big). \end{aligned} \quad (19)$$

Figure 3 shows the calculated transfer characteristic by Hspice simulations incorporating Verilog-A based on the derived model.[18] It is observed that the threshold voltage positively shifts with decreasing the TG voltage for constant sub-threshold swing and off-region current. The increase of threshold voltage is attributed to the depletion of charges in the IGZO film for the negative top-gate voltage. Due to the adjustable threshold voltage, multiple functions can be realized by asynchronous DG IGZO TFTs with increasing flexibility in circuit design.

The touch sensing efficiency with SG and DG TFTs is compared.[19] Figure 4(a) shows the touch pixel circuit based on photodiode (PD). The pixel consists of one driving TFT (M1), one capacitance (C1), the switching TFT (M2) and the load capacitance (C2), and the parameters for the investigated pixel are listed in Table 2. As the leakage current is

in proportion to the light intensity, the output voltage is increased by the finger-touching events with the decrease of the leakage current through PD.

For the conventional structure, M1 is with the single-gate structure. We propose to replace M1 with a dual-gate structure for a higher driving ability. The value of V_{DD}/V_B is 6 V, V_{SS} and V_{SSR} are -3 V, and -6 V, respectively. It is required that the value of V_{SS} is smaller than the threshold voltage of M1. The voltage V_{TT} received by the top-gate electrode is increased from -6 V to V_{TG} in the sensing period.

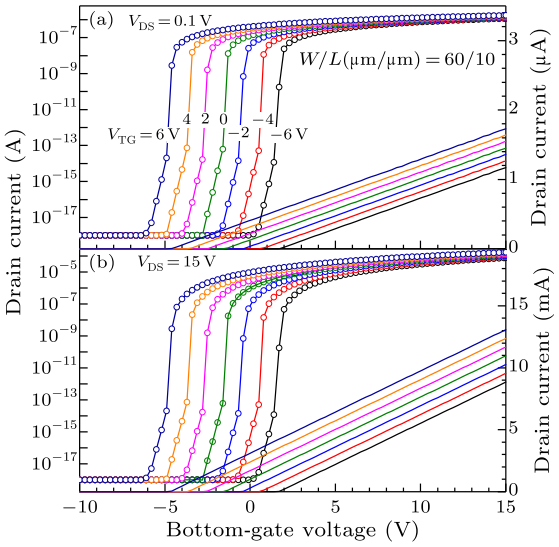

Fig. 3. The calculated transfer characteristic of asynchronous dual-gate IGZO TFTs with various V_{TG}.

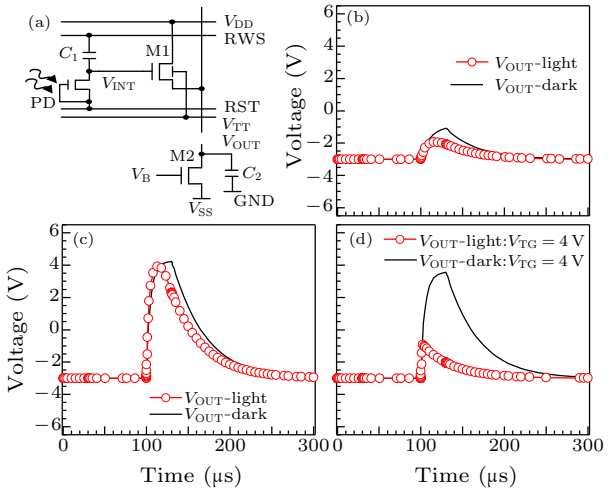

Fig. 4. The touch sensor schematic (a), and transient response of touch sensor with single-gate (b), synchronous dual-gate (c), and asynchronous dual-gate (d) IGZO TFTs.

Table 2. The parameters for touch pixel circuit.

Parameter	Value
Channel width/length of M1 (μm/μm)	60/10
Channel width/length of M2 (μm/μm)	12/4
C_1 (pF)	0.2
C_2 (pF)	25

Figure 4 shows the output of touch-sensing circuit with different M1 structures. For the asynchronous dual-gate mode, the difference of V_{OUT} between dark and light states is 5 V, which is larger than the single-gate and synchronous dual-gate structures. This is attributed to the increase of V_{OUT} for the asynchronous dual-gate mode under the dark condition, as the gate capacitance of M1 is as small as that of the single-gate mode, and the threshold voltage of M1 is comparable with the synchronous dual-gate mode. This is also closely related to the decrease of V_{OUT} for the asynchronous dual-gate mode under the light condition, due to the fast discharging of the gate electrode of M1 whose capacitance is small.

In summary, a compact model for drain-to-source current of dual-gate IGZO TFTs is investigated. By integration of the expression of channel charges, which is controlled by gate voltage, unified models for current-to-voltage DG IGZO TFTs with synchronous and asynchronous modes are derived. It is proved that the threshold voltage of asynchronous dual-gate IGZO TFTs is adjusted by top-gate voltage with the coefficient of C_{TI}/C_{BI}. By implementing the proposed model with Verilog-A, a touch-sensing circuit using dual-gate structure is investigated. It is found that the touch sensitivity is increased by dual-gate IGZO TFTs. The proposed electrical model for dual-gate IGZO TFTs is promising for promoting realization of system designs on display/touch panels.

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