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Interfacial and Electrical Properties of GaAs Metal-Oxide-Semiconductor Capacitor with ZrAlON as the Interfacial Passivation Layer *

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The ZrTiON gate-dielectric GaAs metal-oxide-semiconductor (MOS) capacitors with or without ZrAlON as the interfacial passivation layer (IPL) are fabricated and their properties are investigated. The experimental results show that the GaAs MOS capacitor with the ZrAlON IPL exhibits better interfacial and electrical properties, including lower interface-state density ($1.14 \times 10^{12}\ cm^{-2}eV^{-1}$), smaller gate leakage current ($6.82 \times 10^{-5}\ A/cm^2$ at $V_{fb}+1$ V), smaller capacitance equivalent thickness (1.5 nm), and larger k value (26). The involved mechanisms lie in the fact that the ZrAlON IPL can effectively block the diffusion of Ti and O towards the GaAs surface, thus suppressing the formation of interfacial Ga-/As-oxides and As-As dimers, which leads to improved interfacial and electrical properties for the devices.

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In recent years, as the Si-based complementary metal-oxide-semiconductor (CMOS) technology is approaching its fundamental scaling limit, GaAs-based MOS devices have received more and more attention in sub-10 nm logic metal-oxide semiconductor field-effect transistor (MOSFET) because of its high electron mobility, relatively large band gap and high injection velocity.[1–3] In addition, integrating the high-k gate dielectric into the GaAs-based MOS devices has been widely investigated due to the increasing gate leakage current with the device scaling.[4] However, the high-k/GaAs interface usually has many defects, e.g., Ga-/As-oxides and As-As dimers, which will result in the Fermi level pinning on the GaAs surface.[1,5,6] Thus it is extremely important to passivate the interface by using an interfacial passivation layer (IPL) before depositing the high-k gate dielectric. Usually, aluminum-oxide (Al_2O_3) is regarded as a desirable gate dielectric because of its large bandgap (~9 eV), high breakdown field (~5–10 MV/cm), high thermal stability and remaining amorphous under typical processing conditions.[7] Also, good interfacial and electrical properties have been obtained by using Al_2O_3 as IPL or the gate dielectric for GaAs-based MOS capacitors.[8–12] However, the k value of Al_2O_3 is not large enough (~8), which limits further device scaling.[2] On the other hand, zirconium-oxide (ZrO_2) has a large k value (~24) and sufficient band offsets versus GaAs (~1.4 eV for conduction band, ~3.0 eV for valence band),[13] but easily crystallizes during the thermal processing due to its lower crystallization temperature (~400–500℃),[14] which will result in large gate leakage current.[14–16] Thus it is expected that Al-doped ZrO_2 could possess the advantages of both Al_2O_3 and ZrO_2, i.e., high k value, large bandgap, high crystallization temperature and good interfacial properties with GaAs substrate. Moreover, it has been demonstrated that incorporating nitrogen into the oxide can increase the k value, passivate the oxygen vacancies and form strong N-related bonds at/near the dielectric/semiconductor interface to further enhance the thermal stability and reliability of the devices.[2,17–19] Therefore, in this work, Al-doped ZrON (ZrAlON) will be used as the IPL to fabricate the GaAs MOS capacitors with ZrTiON as high-k gate dielectric, and its interfacial and electrical properties are investigated. The experimental results show that the GaAs MOS capacitor with the ZrTiON/ZrAlON gate stack exhibits good interface quality and excellent electrical properties as compared with its counterpart without the IPL.

The Si-doped GaAs wafers (0.5×10^{18}–$1.0 \times 10^{18}\ cm^{-3}$) were in sequence dipped in the organic solvent, diluted HCl and $(NH_4)_2S$ solution for surface cleaning and sulfur passivation. Then the wafers were divided into two groups: (1) a ~2-nm ZrAlN was firstly deposited as the IPL by co-sputtering Zr (RF) and Al (DC) targets, followed by depositing a ~8-nm ZrTiN as the high-k layer by co-sputtering Zr (RF) and Ti (DC) targets, denoted as ZrAlON sample; (2) a control sample with only ~10-nm ZrTiN as high-k gate dielectric. All the sputtering was carried out in an Ar/N_2 (24 sccm/12 sccm) ambient atmosphere at room temperature. Post-deposition annealing (PDA) was performed at 600℃ for 60 s in N_2 (500 sccm)+O_2 (50 sccm) to convert the nitride into the oxynitride. Finally, Al gate electrode was formed with an area of $7.85 \times 10^{-5}\ cm^2$, followed by forming-gas (5% H_2+95% N_2) annealing at 300℃ for 20 min.

The capacitance–voltage (C–V) and gate leakage current versus gate voltage (J_g–V_g) measurements were performed by an HP 4284A precision LCR meter and an HP 4156 A semiconductor parameter analyzer, respectively. Physical thickness of the gate dielectric was measured by multi-wavelength ellipsometry. All electrical measurements were carried out under light-tight and electrically shielded conditions at room temperature.

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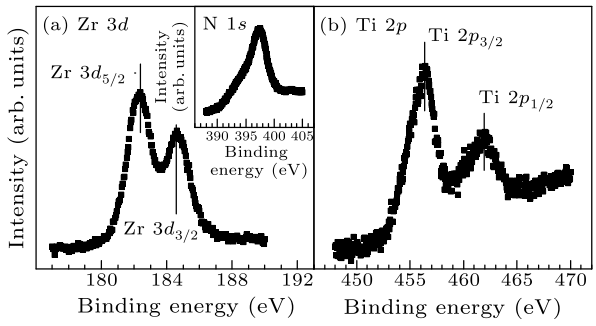

Fig. 1. XPS spectra of (a) Zr 3*d* and (b) Ti 2*p* for the samples. The inset in (a) is N 1*s* spectrum.

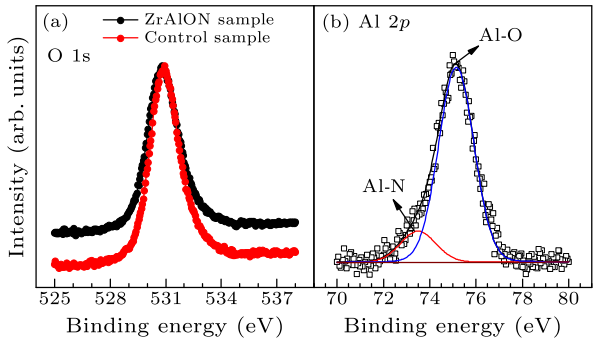

Fig. 2. XPS spectra of (a) O 1*s* for the two samples and (b) Al 2*p* for the ZrAlON sample.

To investigate the composition of the ZrTiON/ZrAlON gate stack and the interfacial chemical states at the high-k/GaAs interface, XPS analyses were carried out for the two samples. For this purpose, the thickness of the gate dielectric layer was thinned to ∼3 nm from the GaAs surface by using an *in situ* Ar^+ ion beam. In Fig. 1, the Zr 3*d* spectrum exhibits two peaks of 3*d*3/2 and 3*d*5/2 at 184.6 eV and 181.3 eV (Fig. 1(a)), respectively, and the Ti 2*p* spectrum also has two peaks at 461.9 eV and 456.4 eV (Fig. 1(b)), respectively, assigned to Ti 2*p*1/2 and Ti 2*p*3/2, showing the existence of Zr and Ti in the gate dielectric. Also, the presence of N can be demonstrated by the N 1*s* peak in the inset of Fig. 1(a). Combining with the O 1*s* peaks presented in Fig. 2(a), the formation of ZrTiON gate dielectric can be confirmed. Further, the Al 2*p* spectrum (Fig. 2(b)) can be well fitted with two peaks at 75.1 eV and 73.5 eV, which are attributed to Al-O and Al-N bonds, respectively. This indicates the composition of aluminum-oxynitride on the GaAs surface and thus confirms the formation of the ZrAlON IPL between the high-k dielectric and the GaAs substrate, combined with the Zr 3*d* spectrum in Fig. 1(a). Also, from the XPS results, the atom ratio of Zr/Ti (or Zr/Al) can be obtained to be $Zr_{0.58}Ti_{0.42}ON$ for the high-k layer and $Zr_{0.68}Al_{0.32}ON$ for the IPL. In Fig. 2(a), it can be seen that the intensity of the O 1*s* peak is obviously weaker for the ZrAlON sample than the control sample,[20] and further, from the XPS measurement, the ratio of the O atom number to the total number of atoms near the GaAs surface can be found to be 26.57% for the ZrAlON sample and 32.05% for the control sample, suggesting that the O content near the GaAs surface is lower for the former than the latter. In addition, in Fig. 3 for the As 3*d* spectrum, a Ti-O peak can be found at 37.0 eV, which belongs to the Ti 3*p*3/2, further confirming the presence of Ti in the gate dielectric.[2] The peak-area ratio of Ti 3*p*3/2 to As 3*d* can be calculated to be 18.67% and 60.28% for the ZrAlON and control samples,[21] respectively, and obviously, the Ti content near the GaAs surface is much lower for the former than the latter. These results indicate that the ZrAlON IPL can effectively block the Ti/O in-diffusion towards the GaAs substrate, thus reducing the defects near/at the GaAs surface and leading to good interfacial and electrical properties as presented in the following.

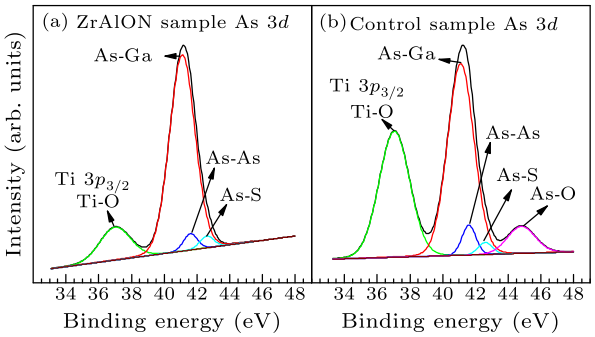

Fig. 3. XPS spectra of As 3*d* for the two samples.

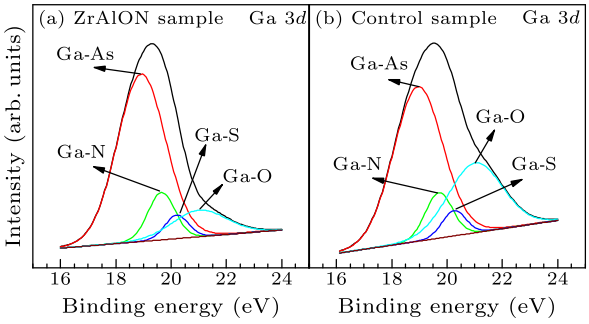

Fig. 4. XPS spectra of Ga 3*d* for the two samples.

The As 3*d* and Ga 3*d* spectra are shown in Figs. 3 and 4, respectively, and As-S, Ga-S and Ga-N peaks can be observed from the two figures, showing the sulfur passivation by $(NH_4)_2S$ dipping and the nitridation during the sputtering in ambient Ar/N_2. These are beneficial to suppress the formation of the Ga/As-oxides to some extent.[20] For the control sample in Fig. 3(b), an evident As-O peak can be found at 44.8 eV, showing the existence of the As-oxide at the GaAs surface, which, however, disappears for the ZrAlON sample, as shown in Fig. 3(a), implying that the ZrAlON IPL can effectively suppress the formation of As-oxide at the GaAs surface. Moreover, an As-As peak can be found in the As 3*d* spectra for the two samples, and the peak-area ratio of As-As/As 3*d*[21] can be calculated to be 4.22% for the ZrAlON sample and 6.48% for the control sample, showing that the content of the As-As bond is also less for the former than the latter. Furthermore, as shown in

Fig. 4(b) for the control sample, a much stronger Ga-O peak than As-O peak can be observed at 21.1 eV, indicating that Ga-oxide concentration is higher than As-oxide at the GaAs surface. This comes from the surface oxidation of the GaAs substrate or the decomposition of As oxide into Ga oxide and elemental As (As_2O_3+GaAs→Ga_2O_3+As) during the PDA at 600℃.[20] However, the intensity of the Ga-O peak for the ZrAlON sample is significantly reduced, as shown in Fig. 4(a), implying that the formation of the Ga-oxide is suppressed to a large extent. It has been reported that the Ga/As oxides and excess As atoms are closely related to the defective bonding states at/near the interface, which will degrade the interfacial and electrical properties of the devices.[18,22,23] Thus it can be suggested from the XPS results that the ZrAlON IPL can effectively suppress the formation of the Ga/As-oxides and As-As dimer at the GaAs surface, due to its strong blocking role against Ti/O in-diffusion, as discussed above, which will decrease the density of the defective interface bonds and will greatly improve the interfacial qualities of the devices, thus leading to excellent electrical properties, as presented in the following.

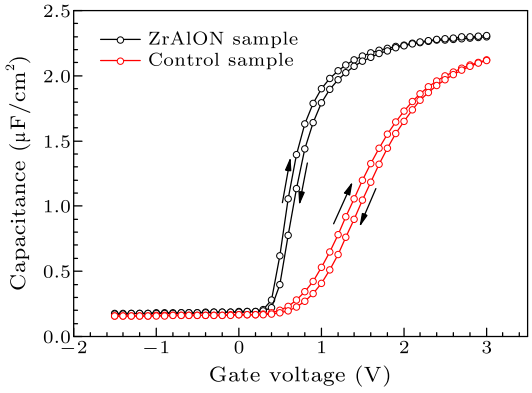

Fig. 5. HF (1-MHz) C–V curves of GaAs MOS capacitors for the two samples.

Figure 5 shows the typical HF (1 MHz) C–V curves of the samples, swept in two directions (from inversion to accumulation and back). As can be seen in Fig. 5, the C–V curve of the control sample shows a large 'stretch-out', small slope in the transition region and the unsaturated accumulation region, which should be attributed to a greater interface-state density caused by a larger amount of the weak Ga-O, As-O and As-As bonds at the GaAs surface, as shown by the above XPS results, thus leading to the Fermi-level pinning.[18,20,24,25] However, for the ZrAlON sample, an excellent C–V behavior is obtained with negligible 'stretch-out', steep slope in the transition region and the saturated accumulation capacitance, indicating good interfacial properties and unpinning Fermi-level. The less Ga/As-oxides at the GaAs surface for the ZrAlON sample than the control sample also leads to its larger accumulation capacitance than the latter, due to the reduced low-k interlayer.[2] In addition, the smaller hysteresis voltage for the ZrAlON sample (80 mV) than the control sample (110 mV) implies a lower density of slow states at/near the interface due to the reduced out-diffusion of Ga and As.[26] Therefore, based on the C–V curves for the two samples, it can be obtained that using the ZrAlON IPL can effectively improve the interfacial and electrical properties for the ZrTiON high-k gate dielectric GaAs MOS capacitors.

The flatband voltage ($V_{\rm fb}$), gate-oxide capacitance per unit area ($C_{\rm ox}$), equivalent k value of the gate dielectric ($k = C_{\rm ox} \cdot T_{\rm ox}/\varepsilon_0$, where $T_{\rm ox}$ is the total physical thickness of the gate dielectric, and ε_0 is the vacuum permittivity), capacitance equivalent thickness ($CET = \varepsilon_0 k_{\rm SiO_2}/C_{\rm ox}$, where $k_{\rm SiO_2}$ is the relative permittivity of SiO_2) can be extracted from the HF C–V curves and the interface-state density ($D_{\rm it}$) can be determined by Terman's method.[27] The value of $V_{\rm fb}$ for the ZrAlON sample is 0.65 V, smaller than that of the control sample (1.45 V), which can be explained by its reduced negative oxide charges associated with the acceptor-like interface and near interface traps, ascribed to the blocking role of the ZrAlON IPL against the out-diffusion of the Ga and As atoms,[2] as mentioned above. The larger k value for the ZrAlON sample (26) than the control sample (24) profits from the suppressed growth of low-k interfacial layer (Ga/As-oxides) on the GaAs surface, which correspondingly gives smaller CET for the former (1.5 nm) than the latter (1.63 nm). Importantly, the extracted $D_{\rm it}$ near the midgap for the ZrAlON sample is $1.14\times10^{12}\,{\rm cm^{-2}eV^{-1}}$ which is much lower than that of the control sample ($1.49\times10^{13}\,{\rm cm^{-2}eV^{-1}}$), closely associated with its greatly reduced Ga/As-oxides and excess As atoms at the GaAs surface, as confirmed by the XPS results above.[18,22,23]

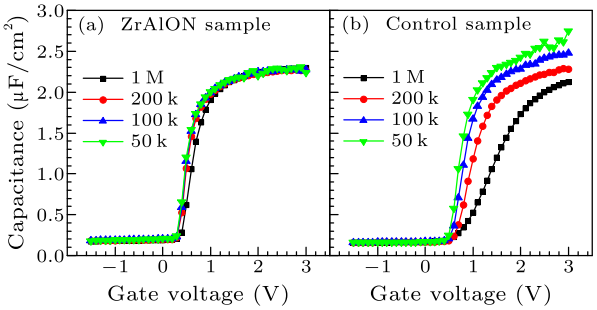

Fig. 6. Frequency dispersions of C–V curves at room temperature for the two samples.

Further, the multi-frequency C–V curves for the two samples are shown in Fig. 6. It can be seen that the control sample exhibits a large frequency dispersion in the depletion and accumulation regions, which, fortunately, is greatly reduced for the ZrAlON sample, especially in the accumulation region. This is attributed to the suppression of an inhomogeneous layer (low-k interlayer) near the gate dielectric/GaAs interface and small interface-state density,[22,28] due to the good passivation effect of the ZrAlON IPL on the GaAs surface.

The gate leakage properties ($J_{\rm g}$ versus $V_{\rm g}$) of the

two samples are shown in Fig. 7(a). It can clearly be seen that the ZrAlON sample exhibits a lower gate leakage current than the control sample, e.g., $6.82 \times 10^{-5}\,\mathrm{A/cm^2}$ and $1.53 \times 10^{-3}\,\mathrm{A/cm^2}$ at $V_\mathrm{g} = V_\mathrm{fb} + 1\,\mathrm{V}$ for the ZrAlON and control samples, respectively. The larger J_g may come from the interfacial trap-assisted tunneling and Ga-/As-oxide induced reduction of the high-k/GaAs conduction-band offset.[24] Thus the small leakage current for the ZrAlON sample is closely related to its less Ga/As-oxide and As-As dimer at the GaAs surface, as shown by the XPS results. Furthermore, a high-field stress at 7 MV/cm $(=(V_\mathrm{g} - V_\mathrm{fb})/T_\mathrm{ox})$ for 3600 s is used to examine the reliability of the devices and the results are shown in Fig. 7(b). After stressing, J_g increases for the two samples, which is probably from the newly-generated interface and near-interface trap-assisted tunneling of electrons from the substrate to the gate.[2] Obviously, the ZrAlON sample exhibits a smaller increase of J_g than the control sample after stressing, indicating its improved interface quality and better device reliability compared with the control sample.

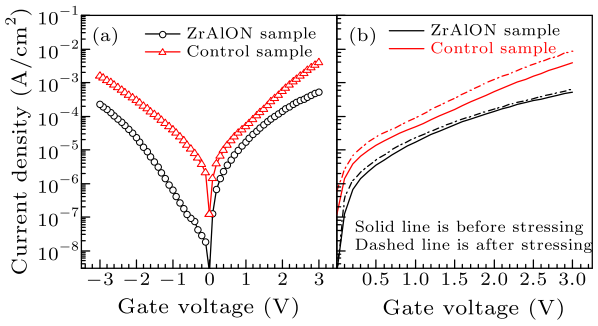

Fig. 7. (a) The J_g–V_g characteristics for the two samples. (b) Comparison of J_g before and after a high-field stress.

In summary, GaAs MOS capacitors with/without ZrAlON IPL have been fabricated by using ZrTiON as high-k gate dielectric and their interfacial and electrical properties are compared. The experimental data and XPS results show that using ZrAlON as IPL can effectively block Ti/O in-diffusion towards the substrate surface and can suppress the formation of Ga/As-oxides and As-As dimers at the interface, thus leading to improved interface quality and excellent electrical properties, including lower interface-state density $(1.14 \times 10^{12}\,\mathrm{cm^{-2}eV^{-1}})$, smaller capacitance equivalent thickness (1.5 nm), higher k value (26) and lower gate leakage current density $(6.82 \times 10^{-5}\,\mathrm{A/cm^2}$ at $V_\mathrm{fb} + 1\,\mathrm{V})$, compared with the sample without the IPL. Therefore, it can be suggested that ZrAlON should be a promising IPL for fabricating high-performance GaAs MOS devices with high-k gate dielectric.

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